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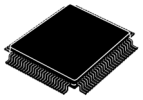
Freescale Semiconductor
Data Sheet: Advance Information

Document Number: MPC5604BC
Rev. 11, 12/2012

MPC5604B/C


208 MAPBGA
(17 x 17 x 1.7 mm)


144 LQFP
(20 x 20 x 1.4 mm)


100 LQFP
(14 x 14 x 1.4 mm)


64 LQFP
(10 x 10 x 1.4 mm)

MPC5604B/C Microcontroller Data Sheet

Features

- Single issue, 32-bit CPU core complex (e200z0)
  - Compliant with the Power Architecture® embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 512 KB on-chip code flash supported with the flash controller and ECC
- 64 (4 × 16) KB on-chip data flash memory with ECC
- Up to 48 KB on-chip SRAM with ECC
- Memory protection unit (MPU) with 8 region descriptors and 32-byte region granularity
- Interrupt controller (INTC) with 148 interrupt vectors, including 16 external interrupt sources and 18 external interrupt/wakeup sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash memory, or RAM from multiple bus masters
- Boot assist module (BAM) supports internal flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS-lite)
- 10-bit analog-to-digital converter (ADC)
- 3 serial peripheral interface (DSPI) modules
- Up to 4 serial communication interface (LINFlex) modules
- Up to 6 enhanced full CAN (FlexCAN) modules with configurable buffers
- 1 inter IC communication interface (I^2C) module
- Up to 123 configurable general purpose pins supporting input and output operations (package dependent)
- Real Time Counter (RTC) with clock source from 128 kHz or 16 MHz internal RC oscillator supporting autonomous wakeup with 1 ms resolution with max timeout of 2 seconds
- Up to 6 periodic interrupt timers (PIT) with 32-bit counter resolution
- 1 System Module Timer (STM)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The MPC5604B/C is a family of next generation microcontrollers built on the Power Architecture® embedded category.

The MPC5604B/C family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. MPC5604B/C device comparison[1]

Feature	Device															
	MPC5602BxLH	**MPC5602BxLL**	**MPC5602BxLQ**	**MPC5602CxLH**	**MPC5602CxLL**	**MPC5603BxLH**	**MPC5603BxLL**	**MPC5603BxLQ**	**MPC5603CxLH**	**MPC5603CxLL**	**MPC5604BxLH**	**MPC5604BxLL**	**MPC5604BxLQ**	**MPC5604CxLH**	**MPC5604CxLL**	**MPC5604BxMG**
CPU	e200z0h															
Execution speed[2]	Static – up to 64 MHz															
Code Flash	256 KB					384 KB					512 KB					
Data Flash	64 KB (4 × 16 KB)															
RAM	24 KB			32 KB		28 KB			40 KB		32 KB			48 KB		
MPU	8-entry															
ADC (10-bit)	12 ch	28 ch	36 ch	8 ch	28 ch	12 ch	28 ch	36 ch	8 ch	28 ch	12 ch	28 ch	36 ch	8 ch	28 ch	36 ch
CTU	Yes															
Total timer I/O[3] eMIOS	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit
• PWM + MC + IC/OC[4]	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	10 ch
• PWM + IC/OC[4]	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	40 ch
• IC/OC[4]	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	6 ch
SCI (LINFlex)	3[5]			4												
SPI (DSPI)	2	3		2	3	2	3		2	3	2	3		2	3	
CAN (FlexCAN)	2[6]			5	6	3[7]			5	6	3[7]			5	6	
I^2C	1															
32 kHz oscillator	Yes															
GPIO[8]	45	79	123	45	79	45	79	123	45	79	45	79	123	45	79	123
Debug	JTAG															Nexus2+
Package	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	208 MAPBGA[9]

1 Feature set dependent on selected peripheral multiplexing—table shows example implementation
2 Based on 125 °C ambient operating temperature
3 See the eMIOS section of the device reference manual for information on the channel configuration and functions.
4 IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter
5 SCI0, SCI1 and SCI2 are available. SCI3 is not available.
6 CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
7 CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
8 I/O count based on multiplexing with peripherals
9 208 MAPBGA available only as development package for Nexus2+

Table 2. MPC5604B/C device comparison[1]

Feature	Device										
	SPC560B 40L1	**SPC560B 40L3**	**SPC560B 40L5**	**SPC560C 40L1**	**SPC560C 40L3**	**SPC560B 50L1**	**SPC560B 50L3**	**SPC560B 50L5**	**SPC560C 50L1**	**SPC560C 50L3**	**SPC560B 50B2**
CPU	e200z0h										
Execution speed[2]	Static – up to 64 MHz										
Code Flash	256 KB					512 KB					
Data Flash	64 KB (4 × 16 KB)										
RAM	24 KB			32 KB		32 KB			48 KB		
MPU	8-entry										
ADC (10-bit)	12 ch	28 ch	36 ch	8 ch	28 ch	12 ch	28 ch	36 ch	8 ch	28 ch	36 ch
CTU	Yes										
Total timer I/O[3] eMIOS	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit
• PWM + MC + IC/OC[4]	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	10 ch
• PWM + IC/OC[4]	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	40 ch
• IC/OC[4]	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	6 ch
SCI (LINFlex)	3[5]			4							
SPI (DSPI)	2	3		2	3	2	3		2	3	
CAN (FlexCAN)	2[6]			5	6	3[7]			5	6	
I^2C	1										
32 kHz oscillator	Yes										
GPIO[8]	45	79	123	45	79	45	79	123	45	79	123
Debug	JTAG										Nexus2+
Package	LQFP64[9]	LQFP100	LQFP144	LQFP64[9]	LQFP100	LQFP64[9]	LQFP100	LQFP144	LQFP64[9]	LQFP100	LBGA208[10]

1 Feature set dependent on selected peripheral multiplexing—table shows example implementation

2 Based on 125 °C ambient operating temperature

3 See the eMIOS section of the device reference manual for information on the channel configuration and functions.

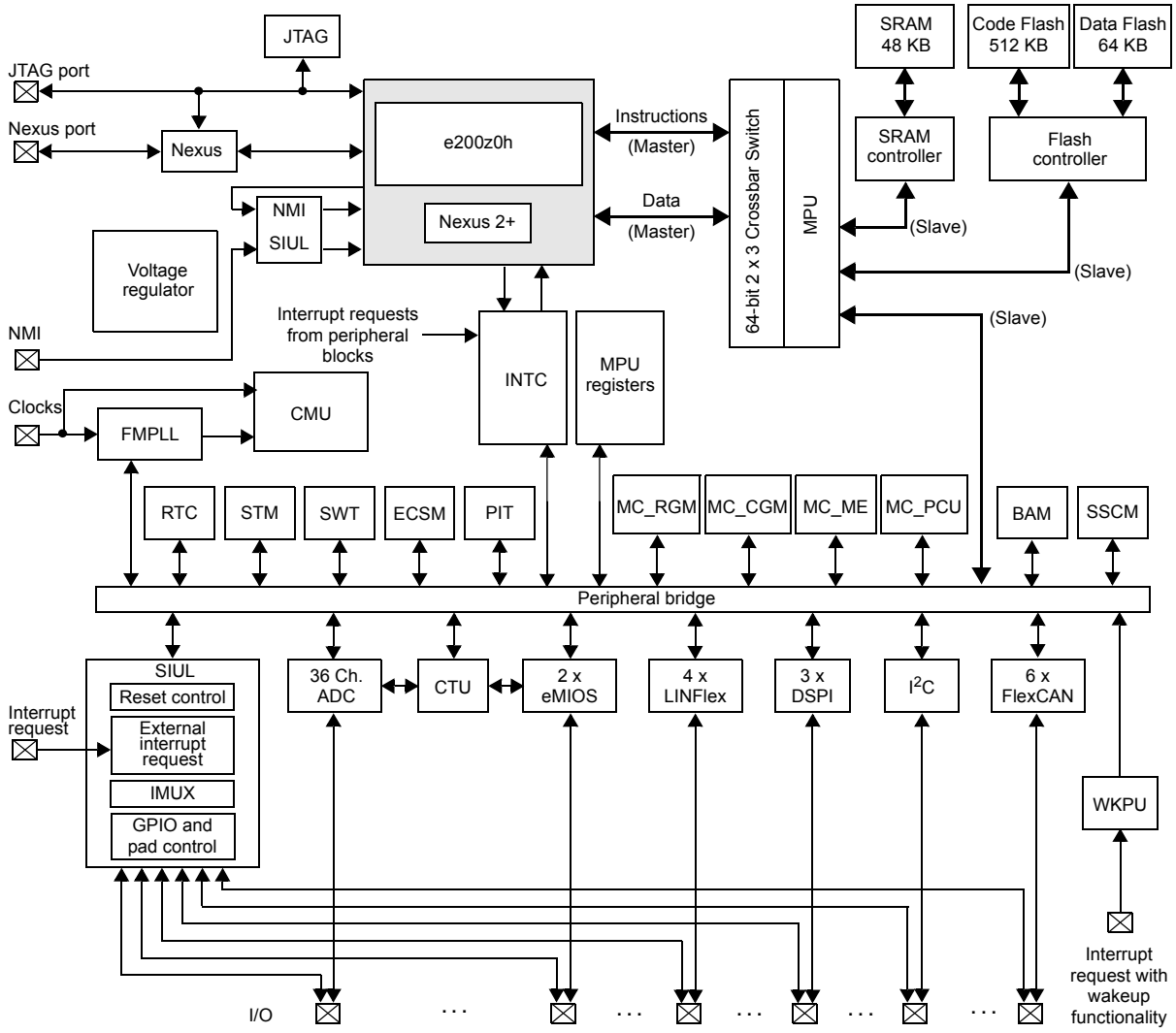
4 IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter

5 SCI0, SCI1 and SCI2 are available. SCI3 is not available.

[6] CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
[7] CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
[8] I/O count based on multiplexing with peripherals
[9] All LQFP64information is indicative and must be confirmed during silicon validation.
[10] LBGA208 available only as development package for Nexus2+

2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5604B/C device series.



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
FlexCAN	Controller Area Network
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
eMIOS	Enhanced Modular Input Output System
FMPLL	Frequency-Modulated Phase-Locked Loop
I^2C	Inter-integrated Circuit Bus
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
ECSM	Error Correction Status Module
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
MPU	Memory Protection Unit
Nexus	Nexus Development Interface (NDI) Level
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit

Figure 1. MPC5604B/C block diagram

Table 3 summarizes the functions of all blocks present in the MPC5604B/C series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Table 3. MPC5604B/C series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device

Table 3. MPC5604B/C series block summary (continued)

Block	Function
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Nexus development interface (NDI)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
System integration unit (SIU)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts and the 208 MAPBGA ballmap are provided in the following figures. For pin signal descriptions, please refer to the device reference manual.

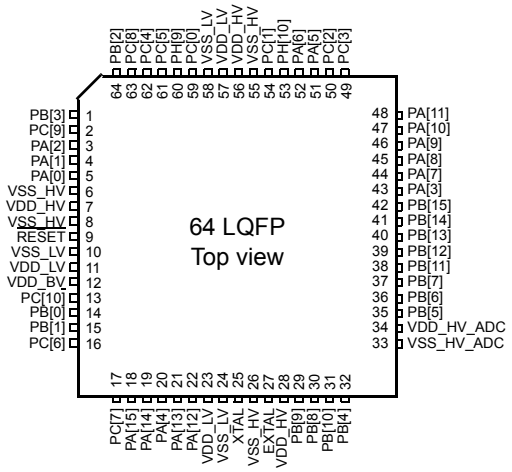


Figure 2. MPC560xB LQFP 64-pin configuration

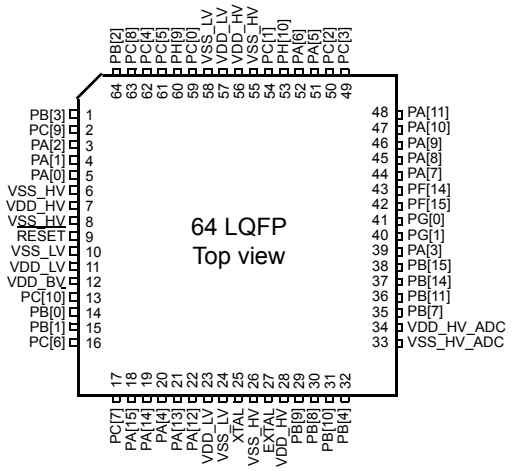
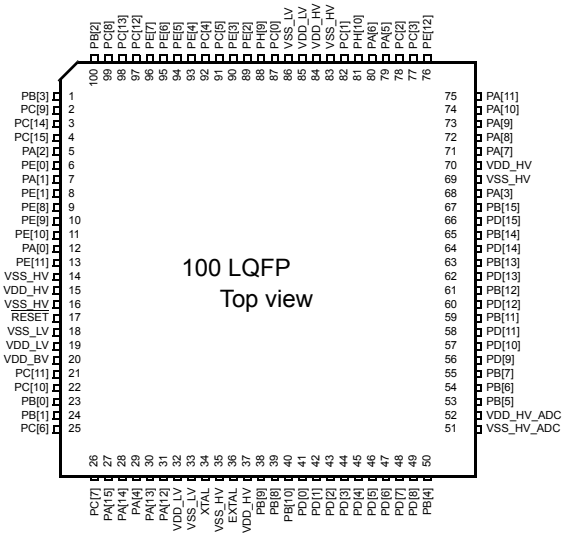
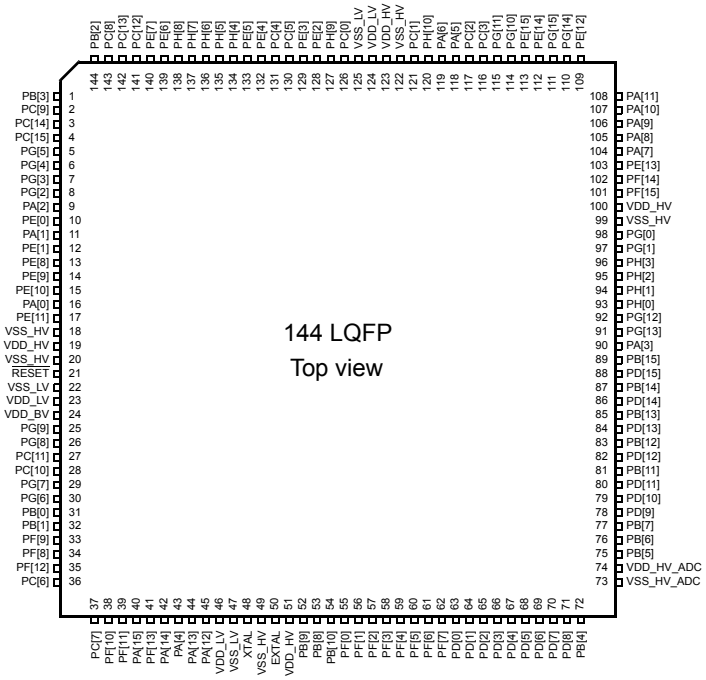


Figure 3. MPC560xC LQFP 64-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Figure 4. LQFP 100-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Figure 5. LQFP 144-pin configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	NC	NC	PH[8]	PH[4]	PC[5]	PC[0]	NC	NC	PC[2]	NC	PE[15]	NC	NC	NC	A
B	PC[9]	PB[2]	NC	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	NC	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	NC	PA[5]	NC	PE[14]	PE[12]	PA[9]	PA[8]	C
D	NC	NC	PC[15]	NC	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	NC	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV	NC	NC	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			NC	NC	NC	NC	J
K	EVTI	NC	VDD_BV	VDD_LV			VSS_HV	VSS_HV	VSS_HV	VSS_HV			NC	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	NC	NC	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	NC	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	NC	PC[7]	NC	NC	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	NC	OSC32K_XTAL	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	NC	OSC32K_EXTAL	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: 208 MAPBGA available only as development package for Nexus 2+.

NC = Not connected

Figure 6. 208 MAPBGA configuration

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Nexus output pads (MDO[*n*], MCKO, EVTO, MSEO) are forced to output.

3.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Three dedicated VDD_LV/VSS_LV supply pairs are used for 1.2 V regulator stabilization.

Table 4. Voltage supply pin descriptions

Port pin	Function	Pin number			
		64 LQFP[1]	100 LQFP	144 LQFP	208 MAPBGA[2]
VDD_HV	Digital supply voltage	7, 28, 56	15, 37, 70, 84	19, 51, 100, 123	C2, D9, E16, G13, H3, N9, R5
VSS_HV	Digital ground	6, 8, 26, 55	14, 16, 35, 69, 83	18, 20, 49, 99, 122	G7, G8, G9, G10, H1, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10
VDD_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.[3]	11, 23, 57	19, 32, 85	23, 46, 124	D8, K4, P7
VSS_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.[3]	10, 24, 58	18, 33, 86	22, 47, 125	C8, J2, N7
VDD_BV	Internal regulator supply voltage	12	20	24	K3
VSS_HV_ADC	Reference ground and analog ground for the ADC	33	51	73	R15
VDD_HV_ADC	Reference voltage and analog supply for the ADC	34	52	74	P14

1 Pin numbers apply to both the MPC560xB and MPC560xC packages.

2 208 MAPBGA available only as development package for Nexus2+

3 A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[1]

M = Medium[1 2]

F = Fast[1 2]

I = Input only with analog feature[1]

J = Input/Output ('S' pad) with analog feature

X = Oscillator

1. See the I/O pad electrical characteristics in the device datasheet for details.
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see PCR.SRC in section Pad Configuration Registers (PCR0–PCR122) in the device reference manual).

3.5 System pins

The system pins are listed in Table 5.

Table 5. System pin descriptions

System pin	Function	I/O direction	Pad type	RESET configuration	Pin number			
					64 LQFP[1]	100 LQFP	144 LQFP	208 MAPBGA[2]
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17	21	J1
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.[3]	I/O	X	Tristate	27	36	50	N8
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.[3]	I	X	Tristate	25	34	48	P8

1 Pin numbers apply to both the MPC560xB and MPC560xC packages.

2 208 MAPBGA available only as development package for Nexus2+

3 See the relevant section of the datasheet

3.6 Functional ports

The functional port pins are listed in Table 6.

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKPU[19][4]	SIUL eMIOS_0 CGL — WKPU	I/O I/O O — I	M	Tristate	5	5	12	16	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI[5] WKPU[2][4]	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	4	7	11	F3

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	39	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	52	80	119	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	46	73	106	C15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PA[10]	PCR[10]	AF0 AF1 AF2 AF3	GPIO[10] E0UC[10] SDA —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	47	47	74	107	B16
PA[11]	PCR[11]	AF0 AF1 AF2 AF3	GPIO[11] E0UC[11] SCL —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	48	48	75	108	B15
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 —	GPIO[12] — — — SIN_0	SIUL — — — DSPI0	I/O — — — I	S	Tristate	22	22	31	45	T7
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	M	Tristate	21	21	30	44	R7
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 — EIRQ[4]	SIUL DSPI_0 DSPI_0 — SIUL	I/O I/O I/O — I	M	Tristate	19	19	28	42	P6
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 — WKPU[10][4]	SIUL DSPI_0 DSPI_0 — WKPU	I/O I/O I/O — I	M	Tristate	18	18	27	40	R6
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — —	SIUL FlexCAN_0 — —	I/O O — —	M	Tristate	14	14	23	31	N3
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — — WKPU[4][4] CAN0RX	SIUL — — — WKPU FlexCAN_0	I/O — — — I I	S	Tristate	15	15	24	32	N1
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA —	SIUL LINFlex_0 I2C_0 —	I/O O I/O —	M	Tristate	64	64	100	144	B2

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — SCL — WKPU[11][4] LIN0RX	SIUL — I2C_0 — WKPU LINFlex_0	I/O — I/O — I I	S	Tristate	1	1	1	1	C3
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — GPI[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	32	50	72	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — GPI[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	—	53	75	R16
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — GPI[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	—	54	76	P15
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — GPI[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	35	55	77	P16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ANS[0] OSC32K_XTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	30	30	39	53	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ANS[1] OSC32K_EXTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	29	29	38	52	T9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKPU[8][4]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	31	40	54	P9
PB[11][8]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	36	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	—	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	—	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	37	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	38	67	89	L13
PC[0][9]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	59	87	126	A8
PC[1][9]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO[10] —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	54	82	121	C9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX[11] — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M	Tristate	50	50	78	117	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX[11] EIRQ[6]	SIUL DSPI_1 ADC — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O — I I I	S	Tristate	49	49	77	116	B11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 CAN3RX[11]	SIUL — — — DSPI_1 FlexCAN_3	I/O — — — I I	M	Tristate	62	62	92	131	B7
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX[11] — EIRQ[7]	SIUL DSPI1 FlexCAN_3 — SIUL	I/O O O — I	M	Tristate	61	61	91	130	A7
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	16	25	36	R2
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12][4]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	17	26	37	P3
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	63	63	99	143	A1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKPU[13][4]	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	2	2	B1
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX[11] MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	13	13	22	28	M3
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX[11] WKPU[5][4]	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	—	—	21	27	M4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	—	—	97	141	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	—	—	98	142	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	—	—	4	4	D3
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — GPI[4]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	41	63	P12

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 —	GPIO[49] — — — GPI[5]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	42	64	T12
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — GPI[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	43	65	R12
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — GPI[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	44	66	P13
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — GPI[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	45	67	R13
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — GPI[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	46	68	T13
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — GPI[10]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	47	69	T14
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — GPI[11]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	48	70	R14
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — GPI[12]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	49	71	T15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — GPI[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	56	78	N15
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — GPI[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	57	79	N14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — GPI[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	58	80	N16
PD[12][8]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ANS[4]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	60	82	M15
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ANS[5]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	—	62	84	M14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ANS[6]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	64	86	L15
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ANS[7]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	66	88	L14
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX[11] WKPU[6][4]	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	—	—	6	10	F1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX[11] —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M	Tristate	—	—	8	12	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 —	GPIO[66] E0UC[18] — — SIN_1	SIUL eMIOS_0 — — DSPI_1	I/O I/O — — I	M	Tristate	—	—	89	128	D7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	—	90	129	C7
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	—	93	132	D6
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	—	94	133	C6
PE[6]	PCR[70]	AF0 AF1 AF2 AF3	GPIO[70] E0UC[22] CS3_0 MA[1]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	—	95	139	B5
PE[7]	PCR[71]	AF0 AF1 AF2 AF3	GPIO[71] E0UC[23] CS2_0 MA[0]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	—	96	140	C4
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX[12] E0UC[22] CAN3TX[11]	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	—	—	9	13	G2
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7][4] CAN2RX[12] CAN3RX[11]	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	—	—	10	14	G1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 — EIRQ[10]	SIUL LINFlex_3 DSPI_1 — SIUL	I/O O O — I	S	Tristate	—	—	11	15	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] — CS4_1 — LIN3RX WKPU[14][4]	SIUL — DSPI_1 — LINFlex_3 WKPU	I/O — O — I I	S	Tristate	—	—	13	17	H2
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — E1UC[19][13] — SIN_2 EIRQ[11]	SIUL — eMIOS_1 — DSPI_2 SIUL	I/O — I/O — I I	S	Tristate	—	—	76	109	C14
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	S	Tristate	—	—	—	103	D15
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	—	112	C13
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] —	SIUL DSPI_2 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	—	—	113	A13
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ANS[8]	SIUL eMIOS_0 DSPI_1 — ADC	I/O I/O O — I	J	Tristate	—	—	—	55	N10
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ANS[9]	SIUL eMIOS_0 DSPI_1 — I	I/O I/O O — I	J	Tristate	—	—	—	56	P10