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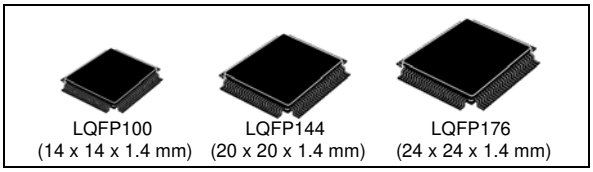
SPC560B54x, SPC560B60x, SPC560B64x

32-bit MCU family built on the Power Architecture® for automotive body electronics applications

Datasheet - production data



Features

- High performance 64 MHz e200z0h CPU
  - 32-bit Power Architecture® technology CPU
  - Up to 60 DMIPs operation
  - Variable length encoding (VLE)
- Memory
  - Up to 1.5 MB on-chip Code Flash with ECC
  - 64 KB on-chip Data Flash with ECC
  - Up to 96 KB on-chip SRAM with ECC
  - 8-entry MPU
- Interrupts
  - 16 priority levels
  - Non-maskable interrupt (NMI)
  - Up to 51 external interrupts lines including 27 wake-up lines
- 16-channel eDMA (linked to PITs, DSPI, ADCs, eMIOS, LINFlex and I^2C)
- GPIOs: 77 (LQFP100), 121 (LQFP144) and 149 (LQFP176)
- Timer units
  - 8-channel 32-bit periodic interrupt timer
  - 4-channel 32-bit system timer
  - System watchdog timer
  - Real-time clock timer
- eMIOS, 16-bit counter timed I/O units
  - Up to 64 channels with PWM/MC/IC/OC
  - Up to 10 counter basis
  - ADC diagnostic trigger via CTU
- One 10-bit and one 12-bit ADC with up to 53 channels
  - Extendable to 81 channels
  - Individual conversion registers
- Cross triggering unit (CTU)
- Dedicated diagnostic module for lighting
  - Advanced PWM generation
  - Time-triggered diagnostics
  - PWM-synchronized ADC measurements
- On-chip CAN/UART bootstrap loader
- Communications interfaces
  - Up to 6 FlexCAN (2.0B active) with 64 message buffers each
  - Up to 10 LINFlex/UART channels
  - Up to 6 buffered DSPI channels
  - I^2C interface
- Clock generation
  - 4 to 16 MHz fast external crystal oscillator
  - 32 kHz slow external crystal oscillator
  - 16 MHz fast internal RC oscillator
  - 128 kHz slow internal RC oscillator for low-power modes
  - Software-controlled FMPLL
  - Clock monitoring unit
- Low-power capabilities
  - Several low-power mode configurations
  - Ultra-low-power standby with RTC and communication
  - Fast wakeup schemes
- Exhaustive debugging capability
  - Nexus 2+ interface on LBGA208 package
  - Nexus 1 on all packages
- Voltage supply
  - Single 5 V or 3.3 V supply
  - On-chip voltage regulator
  - External ballast resistor support
- LQFP100, LQFP144, and LQFP176 packages; LBGA208 package for Nexus2+
- Operating temperature range -40 to 125 °C

Table 1. Device summary

Package	768 KByte Code Flash	1 MByte Code Flash	1.5 MByte Code Flash
LQFP176	—	SPC560B60L7	SPC560B64L7
LQFP144	SPC560B54L5	SPC560B60L5	SPC560B64L5
LQFP100	SPC560B54L3	SPC560B60L3	SPC560B64L3

This is information on a product in full production. www.st.com

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

1.2 Description

This family of 32-bit system-on-chip (SoC) microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (Auxiliary Processor Unit), providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 2. SPC560B54/6x family comparison(1)

Feature	SPC560B54		SPC560B60			SPC560B64			
CPU	e200z0h								
Execution speed(2)	Up to 64 MHz								
Code flash memory	768 KB		1 MB			1.5 MB			
Data flash memory	64 (4 × 16) KB								
SRAM	64 KB		80 KB			96 KB			
MPU	8-entry								
eDMA	16 ch								
10-bit ADC	Yes								
dedicated(3)	7 ch	15 ch	7 ch	15 ch	29 ch	7 ch	15 ch	29 ch	29 ch
shared with 12-bit ADC	19 ch								
12-bit ADC	Yes								
dedicated(4)	5 ch								
shared with 10-bit ADC	19 ch								
Total timer I/O(5) eMIOS	37 ch, 16-bit	64 ch, 16-bit	37 ch, 16-bit	64 ch, 16-bit	64 ch, 16-bit	37 ch, 16-bit	64 ch,16-bit	64 ch, 16-bit	64 ch, 16-bit
Counter / OPWM / ICOC(6)	10 ch								
O(I)PWM / OPWFMB / OPWMCB / ICOC(7)	7 ch								
O(I)PWM / ICOC(8)	7 ch	14 ch	7 ch	14 ch	14 ch	7 ch	14 ch	14 ch	14 ch

Table 2. SPC560B54/6x family comparison[1] (continued)

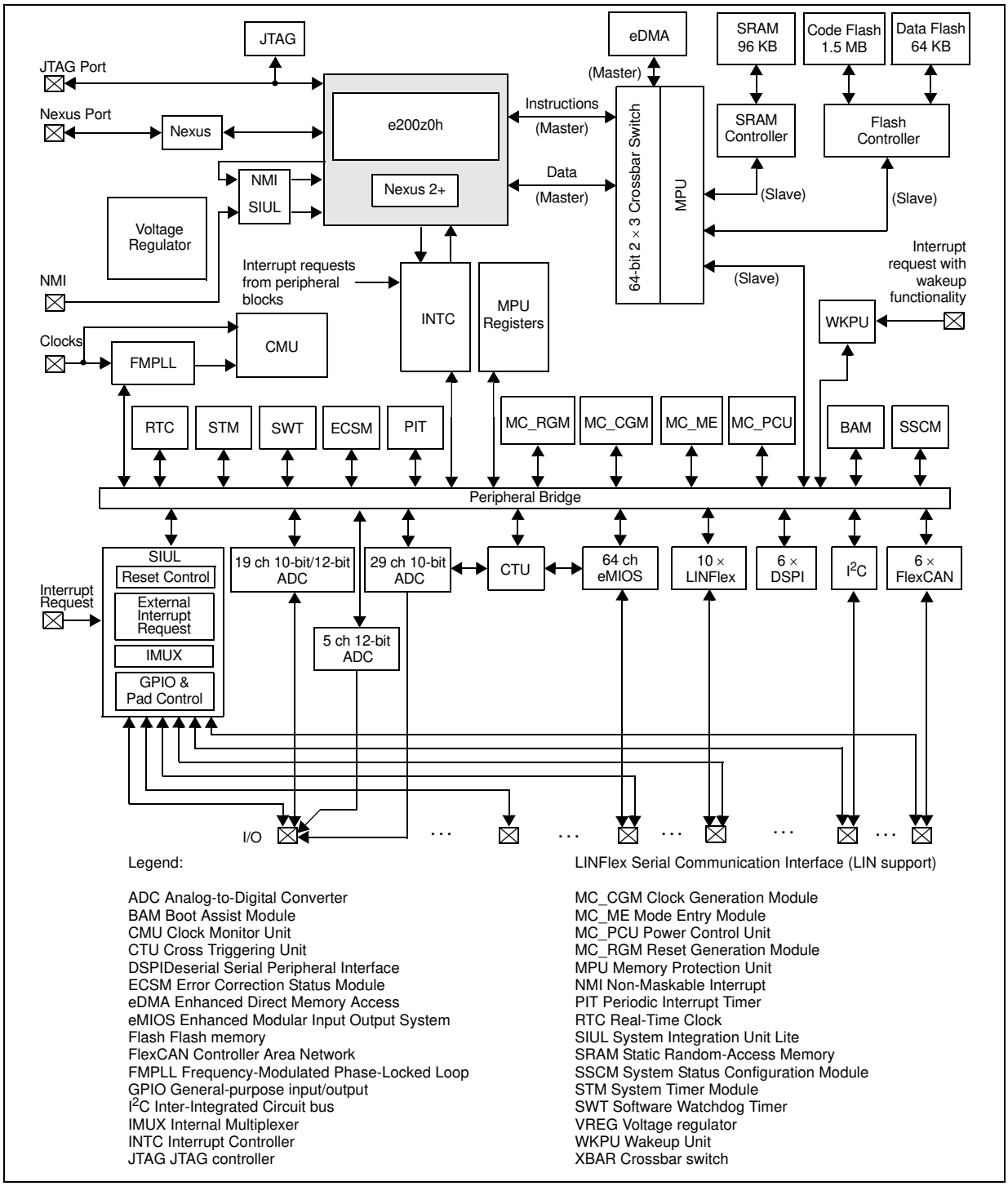
Feature	SPC560B54		SPC560B60			SPC560B64			
OPWM / ICOC[9]	13 ch	33 ch	13 ch	33 ch	33 ch	13 ch	33 ch	33 ch	33 ch
SCI (LINFlex)	4	8	4	8	10	4	8	10	10
SPI (DSPI)	3	5	3	5	6	3	5	6	6
CAN (FlexCAN)	6								
I2C	1								
32 KHz oscillator	Yes								
GPIO[10]	77	121	77	121	149	77	121	149	149
Debug	JTAG								N2+
Package	LQFP 100	LQFP 144	LQFP 100	LQFP 144	LQFP 176	LQFP 100	LQFP 144	LQFP 176	LBGA208[11]

1. Feature set dependent on selected peripheral multiplexing; table shows example.
2. Based on 125 °C ambient operating temperature.
3. Not shared with 12-bit ADC, but possibly shared with other alternate functions.
4. Not shared with 10-bit ADC, but possibly shared with other alternate functions.
5. See the eMIOS section of the chip reference manual for information on the channel configuration and functions.
6. Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.
7. Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.
8. Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.
9. Each channel supports a range of modes including PWM generation, Input Capture, and Output Compare.
10. Maximum I/O count based on multiplexing with peripherals.
11. LBGA208 available only as development package for Nexus2+.

2 Block diagram

Figure 1 shows a top-level block diagram of the SPC560B54/6x.

Figure 1. SPC560B54/6x block diagram



Legend:

ADC Analog-to-Digital Converter
BAM Boot Assist Module
CMU Clock Monitor Unit
CTU Cross Triggering Unit
DSPIDeserial Serial Peripheral Interface
ECSM Error Correction Status Module
eDMA Enhanced Direct Memory Access
eMIOS Enhanced Modular Input Output System
Flash Flash memory
FlexCAN Controller Area Network
FMPLL Frequency-Modulated Phase-Locked Loop
GPIO General-purpose input/output
I2C Inter-Integrated Circuit bus
IMUX Internal Multiplexer
INTC Interrupt Controller
JTAG JTAG controller
LINFlex Serial Communication Interface (LIN support)
MC_CGM Clock Generation Module
MC_ME Mode Entry Module
MC_PCU Power Control Unit
MC_RGM Reset Generation Module
MPU Memory Protection Unit
NMI Non-Maskable Interrupt
PIT Periodic Interrupt Timer
RTC Real-Time Clock
SIUL System Integration Unit Lite
SRAM Static Random-Access Memory
SSCM System Status Configuration Module
STM System Timer Module
SWT Software Watchdog Timer
VREG Voltage regulator
WKPU Wakeup Unit
XBAR Crossbar switch

Table 3 summarizes the functions of the blocks present on the SPC560B54/6x.

Table 3. SPC560B54/6x series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Inter-integrated circuit (I^2C) bus	Two-wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device

Table 3. SPC560B54/6x series block summary (continued)

Block	Function
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 27 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts and the ballmap are provided in the following figures. For pin signal descriptions, please see *Table 6*.

Figure 2 shows the SPC560B54/6x in the LQFP176 package.

Figure 2. LQFP176 pin configuration

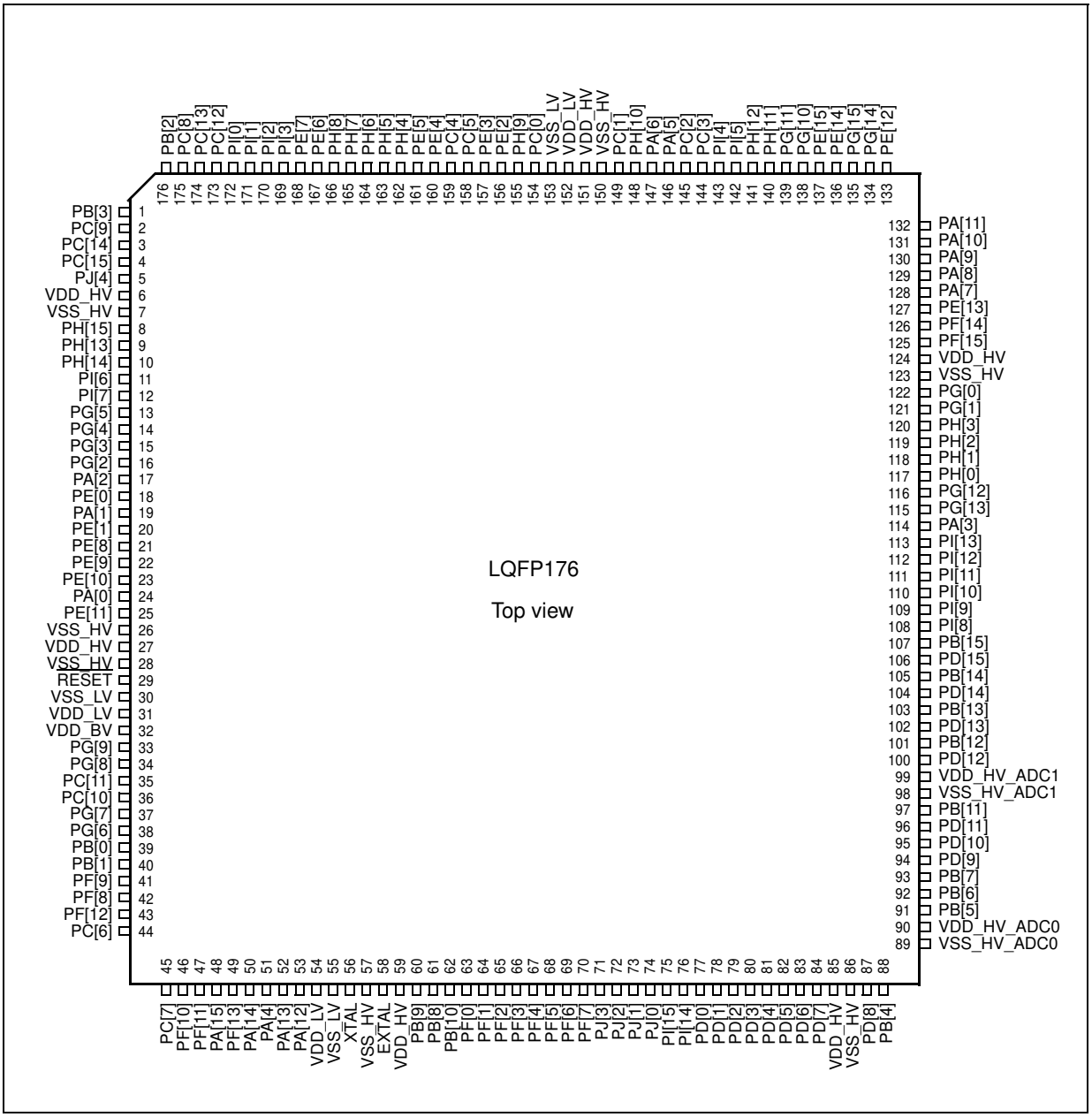


Figure 3 shows the SPC560B54/6x in the LQFP144 package.

Figure 3. LQFP144 pin configuration

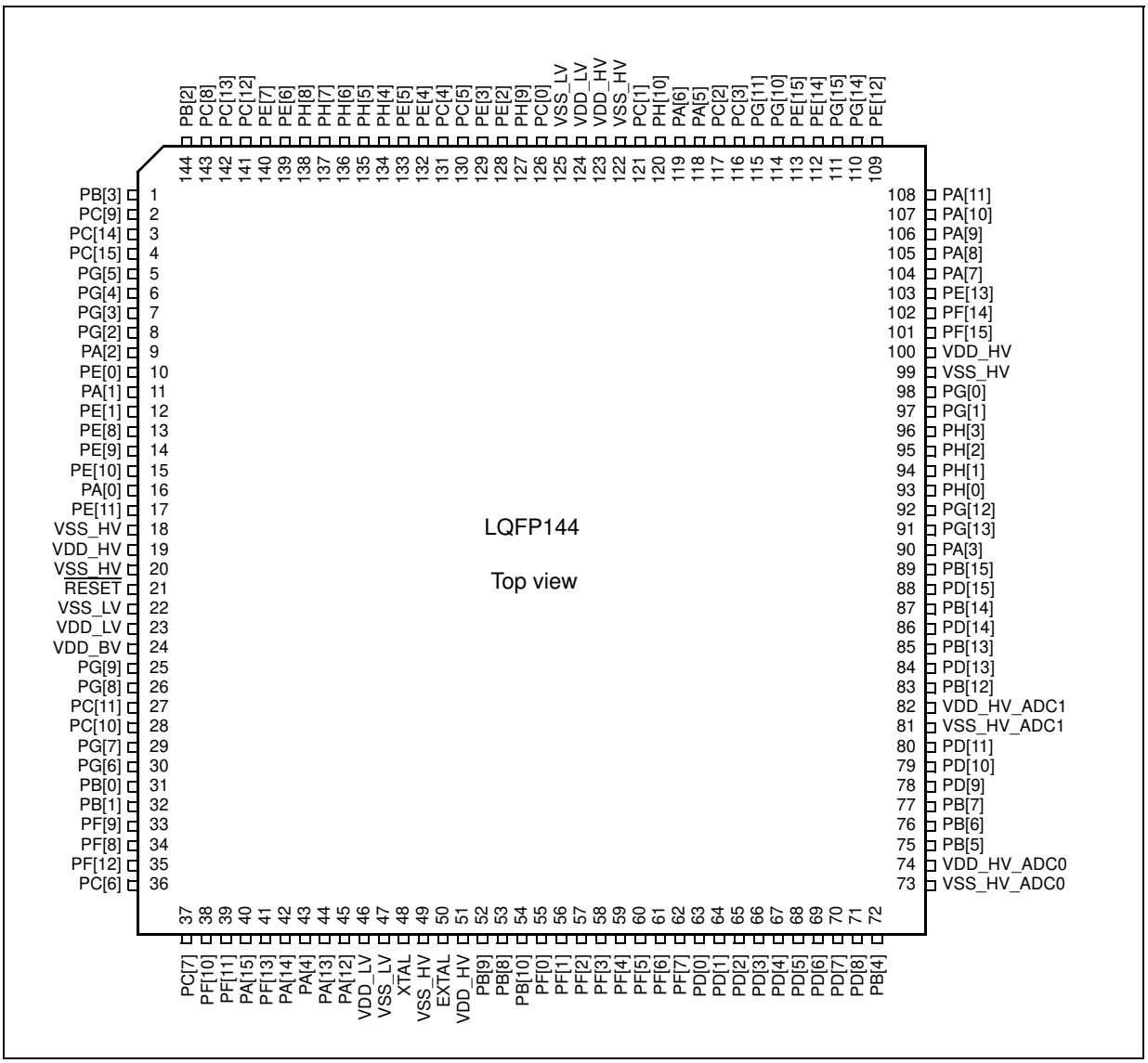


Figure 4 shows the SPC560B54/6x in the LQFP100 package.

Figure 4. LQFP100 pin configuration

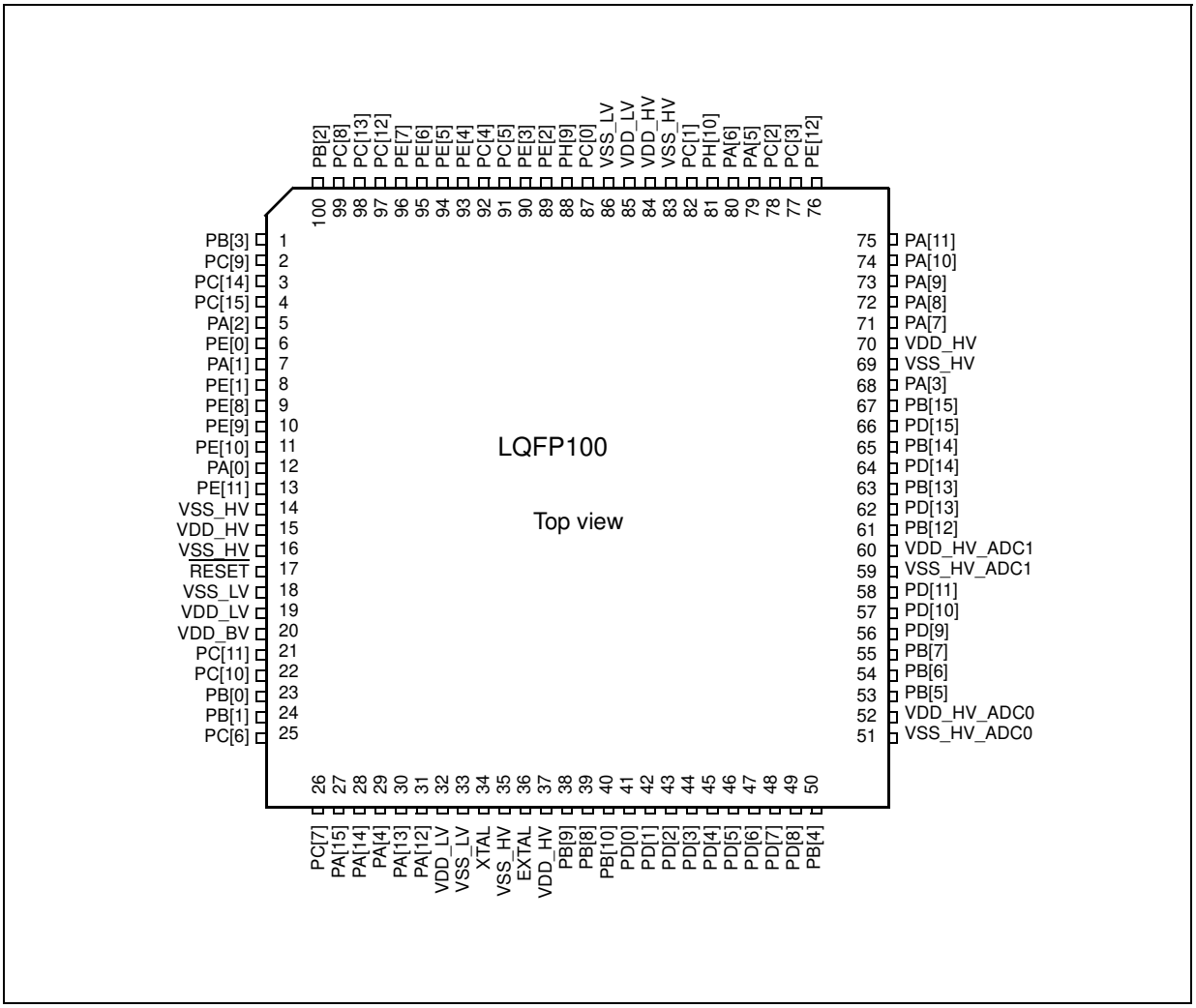


Figure 5 shows the SPC560B54/6x in the LBGA208 package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	PH[15]	PJ[4]	PH[8]	PH[4]	PC[5]	PC[0]	PI[0]	PI[1]	PC[2]	PI[4]	PE[15]	PH[11]	NC	NC	A
B	PC[9]	PB[2]	PH[13]	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	PI[2]	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	PI[3]	PA[5]	PI[5]	PE[14]	PE[12]	PA[9]	PA[8]	C
D	PH[14]	PI[6]	PC[15]	PI[7]	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	PH[12]	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV	PI[12]	PI[13]	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			PI[8]	PI[9]	PI[10]	PI[11]	J
K	EVTI	NC	VDD_BV	VDD_LV			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_ADC1	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	VDD_HV	PJ[0]	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	VSS_HV_ADC1	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	PJ[3]	PC[7]	PJ[2]	PJ[1]	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC0	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	PI[14]	XTAL32	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC0	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	PI[15]	EXTAL32	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

NOTE: The LBGA208 is available only as development package for Nexus 2+.

NC = Not connected

Figure 5. LBGA208 configuration

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8], PC[0] and PH[9:10] are in input weak pull-up when out of reset.
- RESET pad is driven low by the device till 40 FIRC clock cycles after phase2 completion. Minimum phase3 duration is 40 FIRC cycles.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

3.3 Pad configuration during standby mode exit

Pad configuration (input buffer enable, pull enable) for low-power wakeup pads is controlled by both the SIUL and WKPU modules. During standby exit, all low power pads PA[0,1,2,4,15], PB[1,3,8,9,10][a], PC[7,9,11], PD[0,1], PE[0,9,11], PF[9,11,13][b], PG[3,5,7,9][b], PI[1,3][c] are configured according to their respective configuration done in the WKPU module. All other pads will have the same configuration as expected after a reset.

The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption.

To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kOhms should be added between the TDO pin and VDD. Only if the TDO pin is used as an application pin and a pull-up cannot be used should a pull-down resistor with the same value be used instead between the TDO pin and GND.

3.4 Voltage supply pins

Voltage supply pins are used to provide power to the device. Three dedicated VDD_LV/VSS_LV supply pairs are used for 1.2 V regulator stabilization.

Table 4. Voltage supply pin descriptions

Port pin	Function	Pin number			
		LQFP100	LQFP144	LQFP176	LBGA208
VDD_HV	Digital supply voltage	15, 37, 70, 84	19, 51, 100, 123	6, 27, 59, 85, 124, 151	C2, D9, E16, G13, H3, N4, N9, R5
VSS_HV	Digital ground	14, 16, 35, 69, 83	18, 20, 49, 99, 122	7, 26, 28, 57, 86, 123, 150	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10
VDD_LV	1.2 V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.(1)	19, 32, 85	23, 46, 124	31, 54, 152	D8, K4, P7
VSS_LV	1.2 V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.(1)	18, 33, 86	22, 47, 125	30, 55, 153	C8, J2, N7

a. PB[8, 9] ports have wakeup functionality in all modes except STANDBY.

b. PF[9,11,13], PG[3,5,7,9], PI[1,3] are not available in the 100-pin LQFP.

c. PI[1,3] are not available in the 144-pin LQFP.

Table 4. Voltage supply pin descriptions (continued)

Port pin	Function	Pin number			
		LQFP100	LQFP144	LQFP176	LBGA208
VDD_BV	Internal regulator supply voltage	20	24	32	K3
VSS_HV_ADC0	Reference ground and analog ground for the A/D converter 0 (10-bit)	51	73	89	R15
VDD_HV_ADC0	Reference voltage and analog supply for the A/D converter 0 (10-bit)	52	74	90	P14
VSS_HV_ADC1	Reference ground and analog ground for the A/D converter 1 (12-bit)	59	81	98	N12
VDD_HV_ADC1	Reference voltage and analog supply for the A/D converter 1 (12-bit)	60	82	99	K13

1. A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet).

3.5 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[d]

M = Medium[d] [e]

F = Fast[d] [e]

I = Input only with analog feature[d]

J = Input/Output ('S' pad) with analog feature

X = Oscillator

3.6 System pins

The system pins are listed in *Table 5*.

d. See the I/O pad electrical characteristics in the chip datasheet for details.

e. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. The only exception is PC[1] which is in medium configuration by default (see the PCR.SRC description in the chip reference manual, Pad Configuration Registers (PCR0–PCR148)).

Table 5. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number			
					LQFP 100	LQFP 144	LQFP 176	LBGA 208(1)
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input weak pull-up after RGM PHASE2 and 40 FIRC cycles	17	21	29	J1
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	X	Tristate	36	50	58	N8
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	Tristate	34	48	56	P8

1. LBGA208 available only as development package for Nexus2+.

3.7 Functional port pins

The functional port pins are listed in *Table 6*.

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
Port A											
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19][5]	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU	I/O I/O O I/O I	M	Tristate	12	16	24	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI[6] — WKPU[2][5]	SIUL eMIOS_0 WKPU — WKPU	I/O I/O I — I	S	Tristate	7	11	19	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKPU[3][5]	SIUL eMIOS_0 — ADC_0 WKPU	I/O I/O — O I	S	Tristate	5	9	17	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	90	114	K15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKPU[9][5]	SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKPU	I/O I/O — I/O I I	S	Tristate	29	43	51	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] LIN4TX —	SIUL eMIOS_0 LINFlex_4 —	I/O I/O O —	M	Tristate	79	118	146	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX	SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4	I/O I/O — O I I	S	Tristate	80	119	147	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlex_3 — SIUL ADC_1	I/O I/O O — I I	J	Tristate	71	104	128	D16

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[7] —	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — SIUL BAM LINFlex_3	I/O I/O I/O — I I I	S	Input, weak pull-up	72	105	129	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[7]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — O I	S	Pull-down	73	106	130	C15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] SDA LIN2TX ADC1_S[2]	SIUL eMIOS_0 I^2C_0 LINFlex_2 ADC_1	I/O I/O I/O O I	J	Tristate	74	107	131	B16
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] SCL — EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C_0 — SIUL LINFlex_2 ADC_1	I/O I/O I/O — I I I	J	Tristate	75	108	132	B15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI_1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	31	45	53	T7
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M	Tristate	30	44	52	R7
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	28	42	50	P6
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10][5]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	27	40	48	R6
Port B											
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlex_0	I/O O I/O O	M	Tristate	23	31	39	N3

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — — —	GPIO[17] — E0UC[31] — WKPU[4][5] CAN0RX LIN0RX	SIUL — eMIOS_0 — WKPU FlexCAN_0 LINFlex_0	I/O — I/O — I I I	S	Tristate	24	32	40	N1
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlex_0 I^2C_0 eMIOS_0	I/O O I/O I/O	M	Tristate	100	144	176	B2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKPU[11][5] LIN0RX	SIUL eMIOS_0 I^2C_0 — WKPU LINFlex_0	I/O I/O I/O — I I	S	Tristate	1	1	1	C3
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[0] ADC1_P[0] GPIO[20]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	50	72	88	T16

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[1] ADC1_P[1] GPIO[21]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	53	75	91	R16
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[2] ADC1_P[2] GPIO[22]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	54	76	92	P15
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[3] ADC1_P[3] GPIO[23]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	55	77	93	P16