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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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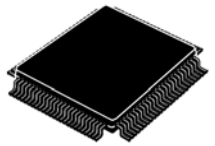
SPC560D30x
SPC560D40x

32-bit MCU family built on the Power Architecture® for automotive body electronics applications

Datasheet – preliminary data

Features

- High-performance up to 48 MHz e200z0h CPU
  - 32-bit Power Architecture® technology CPU
  - Variable length encoding (VLE)
- Memory
  - Up to 256 KB Code Flash with ECC
  - Up to 64 (4x16) KB Data Flash with ECC
  - Up to 16 KB SRAM with ECC
- Interrupts
  - 16 priority levels
  - Non-maskable interrupt (NMI)
  - Up to 38 external interrupts incl. 18 wakeup lines
- 16-channel eDMA
- GPIOs: 45 (LQFP64), 79 (LQFP100)
- Timer units
  - 4-channel 32-bit periodic interrupt timers
  - 4-channel 32-bit system timer module
  - System watchdog timer
  - 32 bit real-time clock timer
- 16-bit counter time-triggered I/Os
  - Up to 28 channels with PWM/MC/IC/OC
  - 5 independent counters
  - 27 ch. with ADC trigger capability
- 12-bit analog-to-digital converter (ADC) with up to 33 channels
  - Up to 61 channels via external multiplexing
  - Individual conversion registers
  - Cross triggering unit (CTU)
- Dedicated diagnostic module for lighting
  - Advanced PWM generation
  - Time-triggered diagnostics
  - PWM-synchronized ADC measurements



LQFP100 (14 x 14 x 1.4 mm)

LQFP64 (10 x 10 x 1.4 mm)

- Communications interfaces
  - 1 FlexCAN interface (2.0B active) with 32 message buffers
  - 3 LINFlex/UART, 1 with DMA capability
  - 2 DSPI
- Clock generation
  - 4 to 16 MHz fast external crystal oscillator
  - 16 MHz fast internal RC oscillator
  - 128 kHz slow internal RC oscillator
  - Software-controlled FMPLL
  - Clock monitoring unit
- Exhaustive debugging capability
  - Nexus1 on all packages
  - Nexus2+ available on emulation device (SPC560B64B2-ENG)
- On-chip CAN/UART bootstrap loader
- Low power capabilities
  - Several low power mode configurations
  - Ultra-low power standby with RTC,SRAM and CAN monitoring
  - Fast wakeup schemes
- Single 5 V or 3.3 V supply
- Operates in ambient temperature range of -40 to 125 °C

Table 1. Device summary

Package	Part number	
	128 Kbyte code Flash	256 Kbyte code Flash
LQFP100	SPC560D30L3	SPC560D40L3
LQFP64	SPC560D30L1	SPC560D40L1

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1 Introduction

1.1 Document overview

This document describes the device features and highlights the important electrical and physical characteristics.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology and designed specifically for embedded applications.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (auxiliary processing unit), providing improved code density. It operates at speeds of up to 48 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with the user's implementations.

The device platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory.

Table 2. Pictus 512K device comparison

Feature	Device			
	SPC560D30L1	**SPC560D30L3**	**SPC560D40L1**	**SPC560D40L3**
CPU	e200z0h			
Execution speed	Static – up to 48 MHz			
Code flash memory	128 KB		256 KB	
Data flash memory	64 KB (4 × 16 KB)			
SRAM	12 KB		16 KB	
eDMA	16 ch			
ADC (12-bit)	16 ch	33 ch	16 ch	33 ch
CTU	16 ch			
Total timer I/O[1] eMIOS	14 ch, 16-bit	28 ch, 16-bit	14 ch, 16-bit	28 ch, 16-bit
– Type X[2]	2 ch	5 ch	2 ch	5 ch
– Type Y[3]	—	9 ch	—	9 ch
– Type G[4]	7 ch	7 ch	7 ch	7 ch

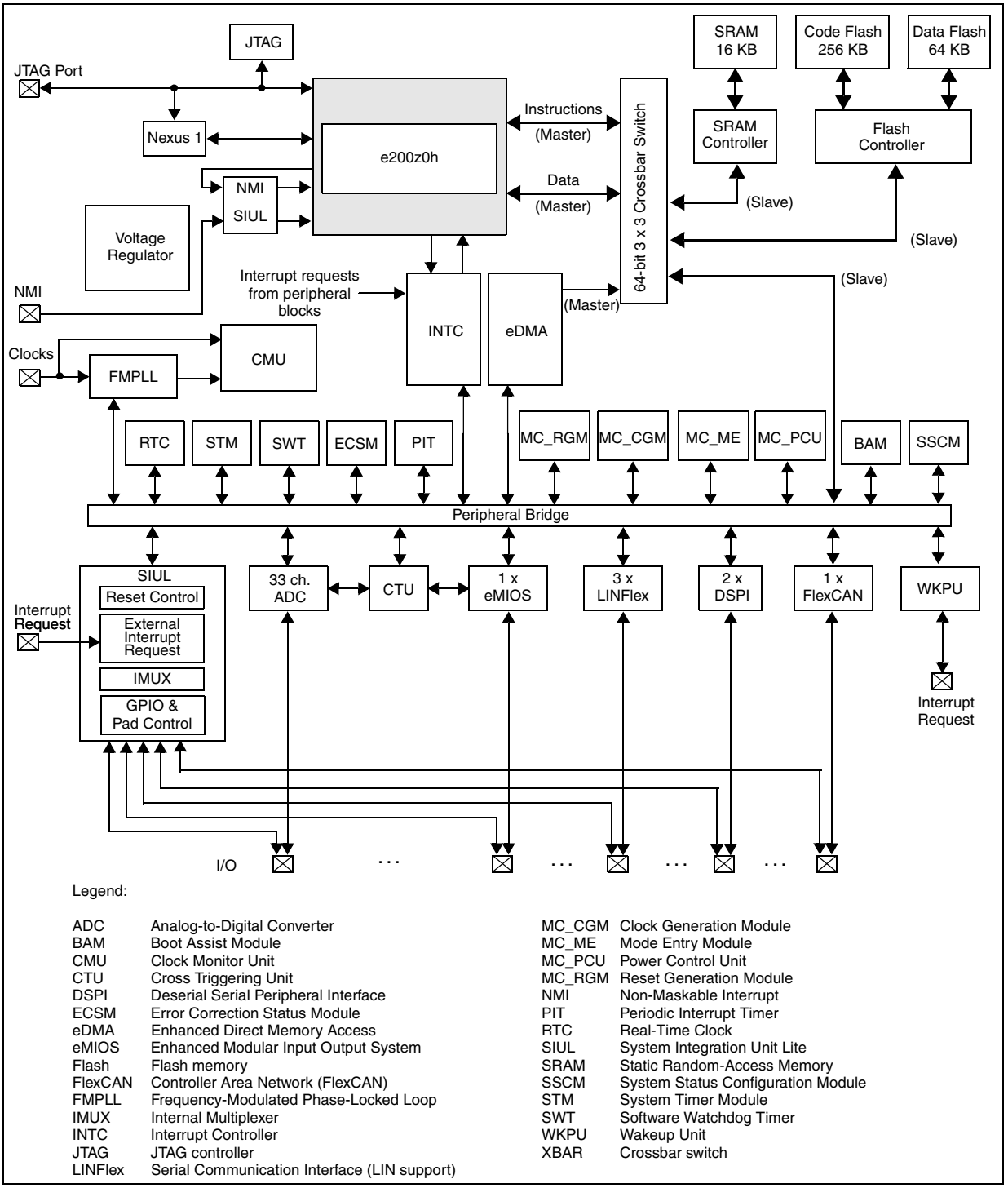
Table 2. Pictus 512K device comparison (continued)

Feature	Device			
	SPC560D30L1	SPC560D30L3	SPC560D40L1	SPC560D40L3
– Type H[5]	4 ch	7 ch	4 ch	7 ch
SCI (LINFlex)	3			
SPI (DSPI)	2			
CAN (FlexCAN)	1			
GPIO[6]	45	79	45	79
Debug	JTAG			
Package	LQFP64	LQFP100	LQFP64	LQFP100

1. Refer to eMIOS chapter of device reference manual for information on the channel configuration and functions.
2. Type X = MC + MCB + OPWMT + OPWMB + OPWFMB + SAIC + SAOC
3. Type Y = OPWMT + OPWMB + SAIC + SAOC
4. Type G = MCB + IPWM + IPM + DAOC + OPWMT + OPWMB + OPWFMB + OPWMCB + SAIC + SAOC
5. Type H = IPWM + IPM + DAOC + OPWMT + OPWMB + SAIC + SAOC
6. I/O count based on multiplexing with peripherals

2 Block diagram

Figure 1 shows a top-level block diagram of the Pictus 512K device series.



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
ECSM	Error Correction Status Module
eDMA	Enhanced Direct Memory Access
eMIOS	Enhanced Modular Input Output System
Flash	Flash memory
FlexCAN	Controller Area Network (FlexCAN)
FMPLL	Frequency-Modulated Phase-Locked Loop
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit
XBAR	Crossbar switch

Figure 1. Pictus 512K series block diagram

Table 3 summarizes the functions of all blocks present in the Pictus 512K series of microcontrollers. Please note that the presence and number of blocks varies by device and package.

Table 3. Pictus 512K series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to-digital converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection

Table 3. Pictus 512K series block summary (continued)

Block	Function
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Real-time counter (RTC)	Provides a free-running counter and interrupt generation capability that can be used for timekeeping applications
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to *Table 6*.

Figure 2 shows the Pictus 512K in the LQFP100 package.

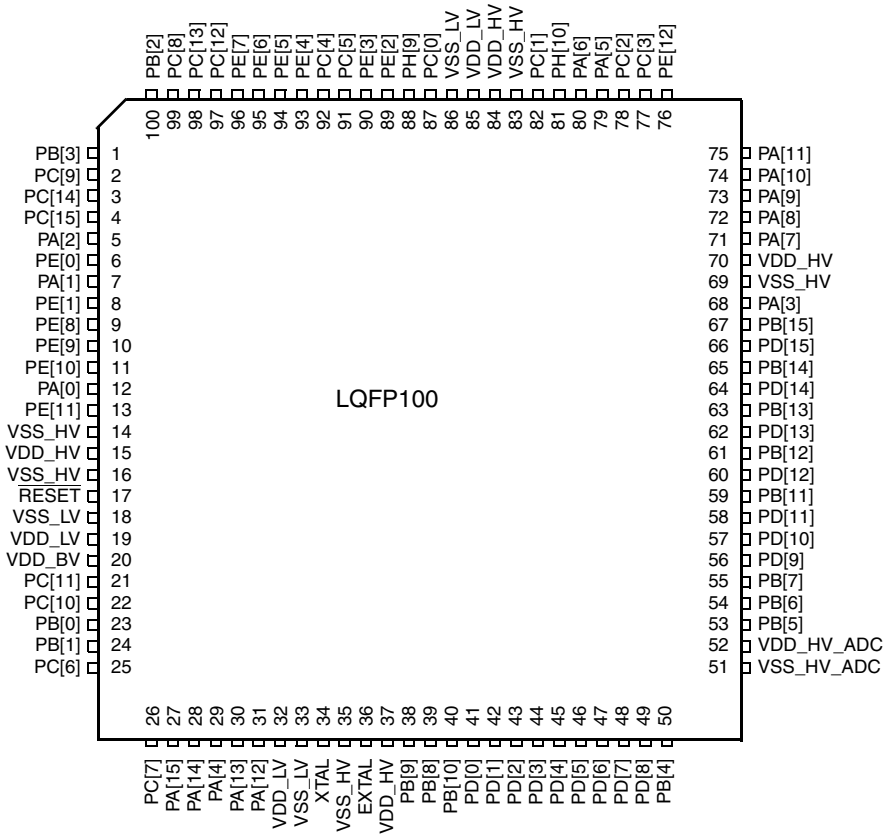


Figure 2. LQFP100 pin configuration (top view)

Figure 3 shows the Pictus 512K in the LQFP64 package.

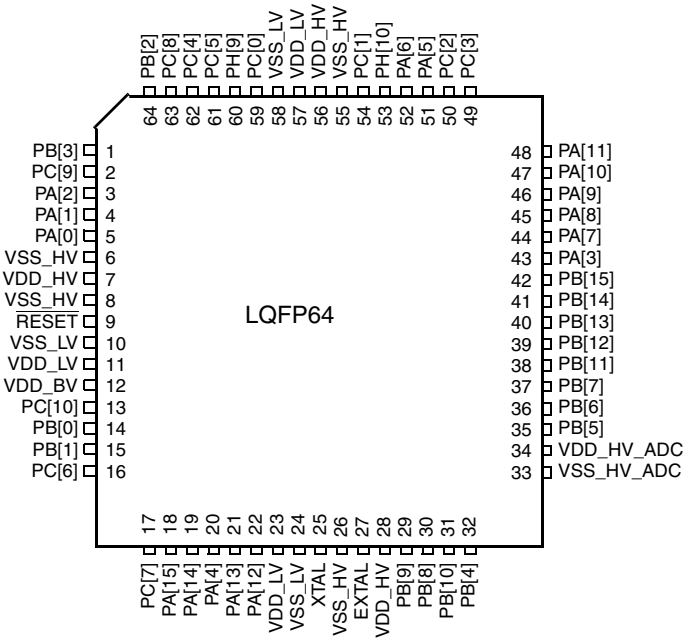


Figure 3. LQFP64 pin configuration (top view)

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up while TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.

3.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

Table 4. Voltage supply pin descriptions

Port pin	Function	Pin number	
		LQFP64	LQFP100
VDD_HV	Digital supply voltage	7, 28, 34, 56	15, 37, 52, 70, 84
VSS_HV	Digital ground	6, 8, 26, 33, 55	14, 16, 35, 51, 69, 83
VDD_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.(1)	11, 23, 57	19, 32, 85
VSS_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.(1)	10, 24, 58	18, 33, 86
VDD_BV	Internal regulator supply voltage	12	20

1. A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[a]

M = Medium[a] [b]

F = Fast[a] [b]

I = Input only with analog feature[a]

J = Input/Output ('S' pad) with analog feature

X = Oscillator

3.5 System pins

The system pins are listed in *Table 5*.

Table 5. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number	
					LQFP64	LQFP100
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17

a. See the I/O pad electrical characteristics in the device datasheet for details.

b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see the PCR[SRC] description in the device reference manual).

Table 5. System pin descriptions (continued)

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number	
					LQFP64	LQFP100
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.(1)	I/O	X	Tristate	27	36
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.(1)	I	X	Tristate	25	34

1. Refer to the relevant section of the device datasheet.

3.6 Functional ports

The functional port pins are listed in *Table 6*.

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction (2)	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
Port A									
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19](3)	SIUL eMIOS_0 CGL eMIOS_0 WKPU	I/O I/O O I/O I	M	Tristate	5	12
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI(4) WKPU[2](3)	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	7
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKPU[3](3)	SIUL eMIOS_0 — ADC WKPU	I/O I/O — O I	S	Tristate	3	5

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] — CS4_0 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 — DSPI_0 SIUL ADC	I/O I/O — I/O I I	S	Tristate	43	68
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — CS0_1 WKPU[9][3]	SIUL eMIOS_0 — DSPI_1 WKPU	I/O I/O — I/O I	S	Tristate	20	29
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	79
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1]	SIUL eMIOS_0 — DSPI_1 SIUL	I/O I/O — I/O I	S	Tristate	52	80
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] — — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 — — SIUL ADC	I/O I/O — — I I	S	Tristate	44	71
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[5]	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0]	SIUL eMIOS_0 eMIOS_0 — SIUL BAM	I/O I/O — — I I	S	Input, weak pull-up	45	72
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[5]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — I/O I	S	Pull-down	46	73

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] — LIN2TX ADC1_S[2]	SIUL eMIOS_0 — LINFlex_2 ADC	I/O I/O — O I	S	Tristate	47	74
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] — — EIRQ[16] ADC1_S[3] LIN2RX	SIUL eMIOS_0 — — SIUL ADC LINFlex_2	I/O I/O — — I I I	S	Tristate	48	75
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — — — EIRQ[17] SIN_0	SIUL — — — SIUL DSPI_0	I/O — — — I I	S	Tristate	22	31
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — CS3_1	SIUL DSPI_0 — DSPI_1	I/O O — I/O	M	Tristate	21	30
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	19	28
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10][3]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	18	27
Port B									
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — LIN2TX	SIUL FlexCAN_0 — LINFlex_2	I/O O — O	M	Tristate	14	23

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — LIN0RX WKPU[4][3] CAN0RX	SIUL — — LINFlex_0 WKPU FlexCAN_0	I/O — — I I I	S	Tristate	15	24
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX — —	SIUL LINFlex_0 — —	I/O O — —	M	Tristate	64	100
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — — — WKPU[11][3] LIN0RX	SIUL — — — WKPU LINFlex_0	I/O — — — I I	S	Tristate	1	1
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — ADC1_P[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	50
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — ADC1_P[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	53
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — ADC1_P[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	54
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — ADC1_P[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	55

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ADC1_S[4] WKPU[25][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	30	39
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ADC1_S[5] WKPU[26][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	29	38
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ADC1_S[6] WKPU[8][3]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	40
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC1_S[12]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC1_X[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC1_X[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC1_X[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC1_X[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67
Port C									
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F	Tristate	54	82
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 — — EIRQ[5]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	M	Tristate	50	78
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 —	GPIO[35] CS0_1 MA[0] — EIRQ[6]	SIUL DSPI_1 ADC — SIUL	I/O I/O O — I	S	Tristate	49	77
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 EIRQ[18]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	M	Tristate	62	92
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	M	Tristate	61	91
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	25

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12][3]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	26
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlex_2 eMIOS_0 —	I/O O I/O —	S	Tristate	63	99
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13][3]	SIUL — eMIOS_0 — LINFlex_2 WKPU	I/O — I/O — I I	S	Tristate	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] — — MA[1]	SIUL — — ADC	I/O — — O	M	Tristate	13	22
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 —	GPIO[43] — — MA[2] WKPU[5][3]	SIUL — — ADC WKPU	I/O — — O I	S	Tristate	—	21
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — EIRQ[19]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	97
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	98
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] — — EIRQ[8]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	—	3

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4
Port D									
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — —	GPIO[48] — — — WKPU[27][3] ADC1_P[4]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	41
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — —	GPIO[49] — — — WKPU[28][3] ADC1_P[5]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	42
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — ADC1_P[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	43
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — ADC1_P[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	44
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — ADC1_P[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	45
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — ADC1_P[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	46

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — ADC1_P[10]	SIUL — — — ADC	I — — — I	I	Tristate	—	47
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — ADC1_P[11]	SIUL — — — ADC	I — — — I	I	Tristate	—	48
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — ADC1_P[12]	SIUL — — — ADC	I — — — I	I	Tristate	—	49
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — ADC1_P[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	56
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — ADC1_P[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	57
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — ADC1_P[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	58
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC1_S[8]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	60
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC1_S[9]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	62

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ADC1_S[10]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	64
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ADC1_S[11]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	66
Port E									
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 —	GPIO[64] E0UC[16] — — WKPU[6][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	—	6
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	8
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 — —	GPIO[66] E0UC[18] — — EIRQ[21] SIN_1	SIUL eMIOS_0 — — SIUL DSPI_1	I/O I/O — — I I	M	Tristate	—	89
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	90
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	93
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	94