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SPC560P44L3, SPC560P44L5
SPC560P50L3, SPC560P50L5

32-bit Power Architecture® based MCU with 576 KB Flash memory and 40 KB SRAM for automotive chassis and safety applications

Datasheet − production data

Features

- 64 MHz, single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with Power Architecture® embedded category
  - Variable Length Encoding (VLE)
- Memory organization
  - Up to 512 KB on-chip code flash memory with ECC and erase/program controller
  - Additional 64 (4 × 16) KB on-chip data flash memory with ECC for EEPROM emulation
  - Up to 40 KB on-chip SRAM with ECC
- Fail safe protection
  - Programmable watchdog timer
  - Non-maskable interrupt
  - Fault collection unit
- Nexus L2+ interface
- Interrupts
  - 16-channel eDMA controller
  - 16 priority level controller
- General purpose I/Os individually programmable as input, output or special function
- 2 general purpose eTimer units
  - 6 timers each with up/down count capabilities
  - 16-bit resolution, cascadable counters
  - Quadrature decode with rotation direction flag
  - Double buffer input capture and output compare
- Communications interfaces
  - 2 LINFlex channels (LIN 2.1)
  - 4 DSPI channels with automatic chip select generation
  - 1 FlexCAN interface (2.0B Active) with 32 message objects

LQFP144 (20 x 20 x 1.4 mm)   LQFP100 (14 x 14 x 1.4 mm)

  - 1 safety port based on FlexCAN with 32 message objects and up to 7.5 Mbit/s capability; usable as second CAN when not used as safety port
  - 1 FlexRay™ module (V2.1) with selectable dual or single channel support, 32 message objects and up to 10 Mbit/s (512 KB device only)
- Two 10-bit analog-to-digital converters (ADC)
  - 2 × 11 input channels, + 4 shared channels
  - Conversion time < 1 µs including sampling time at full precision
  - Programmable ADC Cross Triggering Unit (CTU)
  - 4 analog watchdogs with interrupt capability
- On-chip CAN/UART bootstrap loader with Boot Assist Module (BAM)
- 1 FlexPWM unit: 8 complementary or independent outputs with ADC synchronization signals
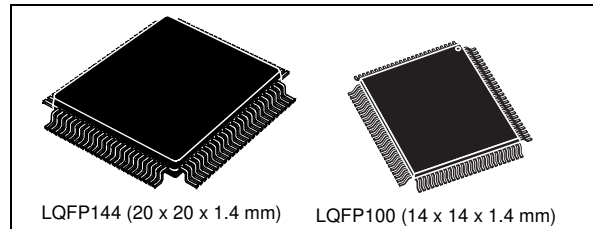
Table 1.   Device summary

Package	Part number	
	448 KB Flash	**576 KB Flash**
LQFP144	SPC560P44L5	SPC560P50L5
LQFP100	SPC560P44L3	SPC560P50L3

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1   Introduction

1.1   Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC560P44/50 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2   Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3   Device comparison

Table 2 provides a summary of different members of the SPC560P44Lx, SPC560P50Lx family and their features—relative to full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2.   SPC560P44Lx, SPC560P50Lx device comparison

Feature	SPC560P44	SPC560P50
Code flash memory (with ECC)	384 KB	512 KB
Data flash memory / EE option (with ECC)	64 KB	
SRAM (with ECC)	36 KB	40 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	2	
INTC (interrupt controller) channels	147	
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)	

Table 2. SPC560P44Lx, SPC560P50Lx device comparison (continued)

Feature		SPC560P44	SPC560P50
eDMA (enhanced direct memory access) channels		16	
FlexRay		Yes[1]	
FlexCAN (controller area network)		2[2],[3]	
Safety port		Yes (via second FlexCAN module)	
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	
eTimer		2 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capturing on X-channels)	
ADC (analog-to-digital converter)		2 (10-bit, 15-channel[4])	
LINFlex		2	
DSPI (deserial serial peripheral interface)		4	
CRC (cyclic redundancy check) unit		Yes	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Level 2+)	
Supply	Digital power supply[5]	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP100 LQFP144	
Temperature	Standard ambient temperature	–40 to 125 °C	

1. 32 message buffers, selectable single or dual channel support

2. Each FlexCAN module has 32 message buffers.

3. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.

4. Four channels shared between the two ADCs

5. The different supply voltages vary according to the part number ordered.

SPC560P44Lx, SPC560P50Lx is available in two configurations having different features: full-featured and airbag. *Table 3* shows the main differences between the two versions.

Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences

Feature	Full-featured	Airbag
CTU (cross triggering unit)	Yes	No
FlexPWM	Yes	No

Table 3.   SPC560P44Lx, SPC560P50Lx device configuration differences (continued)

Feature	Full-featured	Airbag
FlexRay	Yes	No
FMPLL (frequency-modulated phase-locked loop) module	2 (one FMPLL, one for FlexRay)	1 (only FMPLL)

1.4   Block diagram

Figure 1 shows a top-level block diagram of the SPC560P44Lx, SPC560P50Lx MCU.
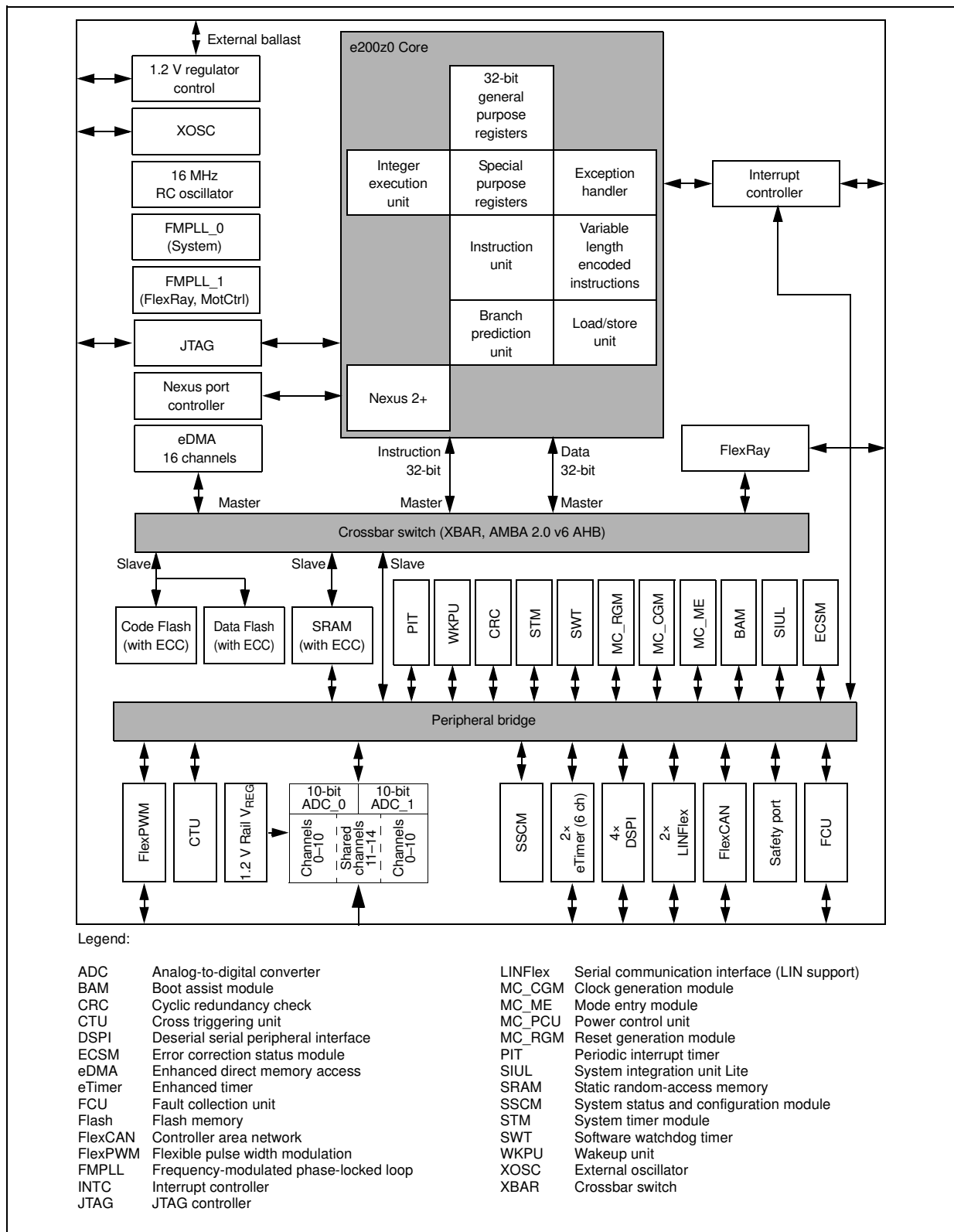
Figure 1.   SPC560P44Lx, SPC560P50Lx block diagram

Table 4.   SPC560P44Lx, SPC560P50Lx series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with minimum load on CPU
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 4. SPC560P44Lx, SPC560P50Lx series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which is capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR[1] and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, 1 of which can cause non-maskable interrupt requests or wakeup events

1. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

● High performance e200z0 core processor for managing peripherals and interrupts

● Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU

● Harvard architecture

● Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
   – Results in smaller code size footprint
   – Minimizes impact on performance

● Branch processing acceleration using lookahead instruction buffer

● Load/store unit
   – 1 cycle load latency
   – Misaligned access support
   – No load-to-use pipeline bubbles

● Thirty-two 32-bit general purpose registers (GPRs)

● Separate instruction bus and load/store bus Harvard architecture

● Hardware vectored interrupt support

● Reservation instructions for implementing read-modify-write constructs

● Long cycle time instructions, except for guarded loads, do not increase interrupt latency

● Extensive system development support through Nexus debug port

● Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 4 master ports:
  - e200z0 core complex Instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
  - FlexRay
- 3 slave ports:
  - Flash memory (code flash and data flash)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8, 16 or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer for assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The SPC560P44Lx, SPC560P50Lx provides as much as 576 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

The flash memory module provides the following features:

● As much as 576 KB flash memory
  – 8 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 3×128 KB) code flash
  – 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  – Full Read While Write (RWW) capability between code and data flash

● Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)

● Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz

● Hardware managed flash memory writes handled by 32-bit RISC Krypton engine

● Hardware and software configurable read and write access protections on a per-master basis

● Configurable access timing allowing use in a wide range of system frequencies

● Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types.

● Software programmable block program/erase restriction control

● Erase of selected block(s)

● Read page sizes
  – Code flash memory: 128 bits (4 words)
  – Data flash memory: 32 bits (1 word)

● ECC with single-bit correction, double-bit detection for data integrity
  – Code flash memory: 64-bit ECC
  – Data flash memory: 64-bit ECC

● Embedded hardware program and erase algorithm

● Erase suspend, program suspend and erase-suspended program

● Censorship protection scheme to prevent flash memory content visibility

● Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The SPC560P44Lx, SPC560P50Lx SRAM module provides up to 40 KB of general-purpose memory.

The SRAM module provides the following features:

● Supports read/write accesses mapped to the SRAM from any master

● Up to 40 KB general purpose SRAM

● Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

● Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 147 selectable-priority interrupt sources.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

● Unique 9-bit vector for each separate interrupt source

● 8 software triggerable interrupt sources

● 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source

● Ability to modify the ISR or task priority: modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.

● 2 external high priority interrupts directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

● System configuration and status
    – Memory sizes/status
    – Device mode and security status
    – Determine boot vector
    – Search code flash for bootable sector
    – DMA status
● Debug status port enable and selection
● Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P44Lx, SPC560P50Lx:

● Lock detect circuitry continuously monitors lock status

● Loss of clock (LOC) detection for PLL outputs

● Programmable output clock divider ($\div 1$, $\div 2$, $\div 4$, $\div 8$)

● FlexPWM module and eTimer module can run on an independent clock source

● On-chip oscillator with automatic level control

● Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

● Input clock frequency: 4–40 MHz
● Maximum output frequency: 64 MHz
● Voltage controlled oscillator (VCO)—frequency 256–512 MHz
● Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
● Frequency-modulated PLL
    – Modulation enabled/disabled through software
    – Triangle wave modulation
● Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
● Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

● Input frequency range: 4–40 MHz
● Crystal input mode or oscillator input mode
● PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

● Nominal frequency 16 MHz
● ±5% variation over voltage and temperature after process trim
● Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
● RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

● 4 general purpose interrupt timers
● 32-bit counter resolution
● Clocked by system clock frequency
● Each channel can be used as trigger for a DMA request

1.5.13 System timer module (STM)

The STM module implements these features:

● One 32-bit up counter with 8-bit prescaler
● Four 32-bit compare channels
● Independent interrupt source for each channel
● Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

● 32-bit time-out register to set the time-out period
● Programmable selection of system or oscillator clock for timer operation
● Programmable selection of window mode or regular servicing
● Programmable selection of reset or interrupt on an initial time-out
● Master access protection
● Hard and soft configuration lock bits
● Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

● FCU status register reporting the device status
● Continuous monitoring of critical fault signals
● User selection of critical signals from different fault sources inside the device
● Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, safety relay or FlexRay transceiver)
● Faults are latched into a register

1.5.16 System integration unit – Lite (SIUL)

The SPC560P44Lx, SPC560P50Lx SIUL controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

● Centralized general purpose input output (GPIO) control of as many as 80 input/output pins and 26 analog input-only pads (package dependent)

● All GPIO pins can be independently configured to support pull-up, pull down, or no pull

● Reading and writing to GPIO supported both as individual pins and 16-bit wide ports

● All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins

● ADC channels support alternative configuration as general purpose inputs

● Direct readback of the pin value is supported on all pins through the SIUL

● Configurable digital input filter that can be applied to some general purpose input pins for noise elimination: as many as 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the SPC560P44Lx, SPC560P50Lx: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC560Pxx devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

● Serial bootloading via FlexCAN or LINFlex

● Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

● Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented

● For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC560P44Lx, SPC560P50Lx.

The sources of the ECC errors are:

● Flash memory
● SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

● Duplicated periphery
● Master access privilege level per peripheral (per master: read access enable; write access enable)
● Write buffering for peripherals
● Checker applied on PBRIDGE output toward periphery
● Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

● Full implementation of the CAN protocol specification, version 2.0B
    – Standard data and remote frames
    – Extended data and remote frames
    – Up to 8-bytes data length
    – Programmable bit rate up to 1 Mbit/s
● 32 message buffers of up to 8-bytes data length
● Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
● Programmable loop-back mode supporting self-test operation
● 3 programmable mask registers
● Programmable transmit-first scheme: lowest ID or lowest buffer number
● Time stamp based on 16-bit free-running timer
● Global network time, synchronized by a specific message
● Maskable interrupts
● Independent of the transmission medium (an external transceiver is assumed)
● High immunity to EMI
● Short latency time due to an arbitration scheme for high-priority messages
● Transmit features
    – Supports configuration of multiple mailboxes to form message queues of scalable depth
    – Arbitration scheme according to message ID or message buffer number
    – Internal arbitration to guarantee no inner or outer priority inversion
    – Transmit abort procedure and notification
● Receive features
    – Individual programmable filters for each mailbox
    – 8 mailboxes configurable as a six-entry receive FIFO
    – 8 programmable acceptance filters for receive FIFO
● Programmable clock source
    – System clock
    – Direct oscillator clock to avoid PLL jitter

1.5.21 Safety port (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

● Identical to the FlexCAN module
● Bit rate as fast as 7.5 Mbit/s at 60 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
● 32 message buffers of up to 8 bytes data length
● Can be used as a second independent CAN module

1.5.22 FlexRay

The FlexRay module provides the following features:

● Full implementation of FlexRay Protocol Specification 2.1
● 32 configurable message buffers can be handled
● Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
● Message buffers configurable as Tx, Rx or RxFIFO
● Message buffer size configurable
● Message filtering for all message buffers based on FrameID, cycle count and message ID
● Programmable acceptance filters for RxFIFO message buffers

1.5.23 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P44Lx, SPC560P50Lx features the following:

● Supports LIN Master mode, LIN Slave mode and UART mode
● LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
● Handles LIN frame transmission and reception without CPU intervention
● LIN features
  – Autonomous LIN frame handling
  – Message buffer to store Identifier and as much as 8 data bytes
  – Supports message length as long as 64 bytes
  – Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  – Classic or extended checksum calculation
  – Configurable Break duration as long as 36-bit times
  – Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  – Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  – Interrupt-driven operation with 16 interrupt sources
● LIN slave mode features
  – Autonomous LIN header handling
  – Autonomous LIN response handling
● UART mode
  – Full-duplex operation
  – Standard non return-to-zero (NRZ) mark/space format
  – Data buffers with 4-byte receive, 4-byte transmit
  – Configurable word length (8-bit or 9-bit words)
  – Error detection and flagging
  – Parity, Noise and Framing errors
  – Interrupt-driven operation with four interrupt sources
  – Separate transmitter and receiver CPU interrupt sources
  – 16-bit programmable baud-rate modulus counter and 16-bit fractional
  – 2 receiver wake-up methods

1.5.24 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC560P44Lx, SPC560P50Lx MCU and external devices.

The DSPI modules provide these features:

● Full duplex, synchronous transfers
● Master or slave operation
● Programmable master bit rates
● Programmable clock polarity and phase
● End-of-transmission interrupt flag
● Programmable transfer baud rate
● Programmable data frames from 4 to 16 bits
● Up to 20 chip select lines available
    – 8 on DSPI_0
    – 4 each on DSPI_1, DSPI_2 and DSPI_3
● 8 clock and transfer attributes registers
● Chip select strobe available as alternate function on one of the chip select pins for deglitching
● FIFOs for buffering as many as 5 transfers on the transmit and receive side
● Queueing operation possible through use of the eDMA
● General purpose I/O functionality on pins when not used for SPI

1.5.25 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules, each capable of controlling a single half-bridge power stage. There are also four fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

● 16-bit resolution for center, edge-aligned, and asymmetrical PWMs

● Maximum operating clock frequency of 120 MHz

● PWM outputs can operate as complementary pairs or independent channels

● Can accept signed numbers for PWM generation

● Independent control of both edges of each PWM output

● Synchronization to external hardware or other PWM supported

● Double buffered PWM registers

  – Integral reload rates from 1 to 16

  – Half cycle reload capability

● Multiple ADC trigger events can be generated per PWM cycle via hardware

● Write protection for critical registers

● Fault inputs can be assigned to control multiple PWM outputs

● Programmable filters for fault inputs

● Independently programmable PWM output polarity

● Independent top and bottom deadtime insertion

● Each complementary pair can operate with its own PWM frequency and deadtime values

● Individual software-control for each PWM output

● All outputs can be programmed to change simultaneously via a "Force Out" event

● PWMX pin can optionally output a third PWM signal from each submodule

● Channels not used for PWM generation can be used for buffered output compare functions

● Channels not used for PWM generation can be used for input capture functions

● Enhanced dual-edge capture functionality

● eDMA support with automatic reload

● 2 fault inputs

● Capture capability for PWMA, PWMB, and PWMX channels not supported

1.5.26 eTimer

The SPC560P44Lx, SPC560P50Lx includes two eTimer modules. Each module provides six 16-bit general purpose up/down timer/counter units with the following features:

● Maximum operating clock frequency of 120 MHz
● Individual channel capability
  – Input capture trigger
  – Output compare
  – Double buffer (to capture rising edge and falling edge)
  – Separate prescaler for each counter
  – Selectable clock source
  – 0–100% pulse measurement
  – Rotation direction flag (Quad decoder mode)
● Maximum count rate
  – External event counting: max. count rate = peripheral clock/2
  – Internal clock counting: max. count rate = peripheral clock
● Counters are:
  – Cascadable
  – Preloadable
● Programmable count modulo
● Quadrature decode capabilities
● Counters can share available input pins
● Count once or repeatedly
● Pins available as GPIO when timer functionality not in use

1.5.27 Analog-to-digital converter (ADC) module

The ADC module provides the following features:

Analog part:

● 2 on-chip AD converters
  – 10-bit AD resolution
  – 1 sample and hold unit per ADC
  – Conversion time, including sampling time, less than 1 μs (at full precision)
  – Typical sampling time is 150 ns min. (at full precision)
  – Differential non-linearity error (DNL) ±1 LSB
  – Integral non-linearity error (INL) ±1.5 LSB
  – TUE <3 LSB
  – Single-ended input signal up to 5.0 V
  – The ADC and its reference can be supplied with a voltage independent from V_{DDIO}
  – The ADC supply can be equal or higher than V_{DDIO}
  – The ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
  – Sample times of 2 (default), 8, 64, or 128 ADC clock cycles