



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MPC5642A Microcontroller Datasheet

This is the MPC5642A Datasheet set consisting of the following files:

- MPC5642A Datasheet *Addendum (MPC5642A_AD)*, Rev. 1
- MPC5642A Datasheet (*MPC5642A*), Rev. 3.1

MPC5642A Microcontroller Datasheet Addendum

This addendum describes corrections to the *MPC5642A Microcontroller Datasheet*, order number MPC5642A. For convenience, the addenda items are grouped by revision. Please check our website at <http://www.freescale.com/powerarchitecture> for the latest updates.

The current version available of the *MPC5642A Microcontroller Datasheet* is Revision 3.1.

Table of Contents

1	Addendum List for Revision 3.1	2
2	Revision History	2

1 Addendum List for Revision 3.1

Table 1. MPC5642A Rev 3.1 Addendum

Location	Description
Section 3.11, "Temperature Sensor Electrical Characteristics", Page 77	In "Temperature Sensor Electrical Characteristics" table, update the Min and Max value of "Accuracy" parameter to -20°C and +20°C, respectively.

2 Revision History

[Table 2](#) provides a revision history for this datasheet addendum document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release.	12/2014

How to Reach Us:**Home Page:**

freescale.com

Web Support:

freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale, the Freescale logo, Altivec, C-5, CodeTest, CodeWarrior, ColdFire, C-Ware, Energy Efficient Solutions logo, Kinetis, mobileGT, PowerQUICC, Processor Expert, QorIQ, Qorivva, StarCore, Symphony, and VortiQa are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast, BeeKit, BeeStack, ColdFire+, CoreNet, Flexis, MagniV, MXC, Platform in a Package, QorIQ Qonverge, QUICC Engine, Ready Play, SafeAssure, SMARTMOS, TurboLink, Vybrid, and Xtrinsic are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2014 Freescale Semiconductor, Inc.

Document Number: MPC5642A_AD

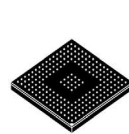
Rev. 1

12/2014



Qorivva MPC5642A Microcontroller Data Sheet

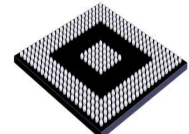
MPC5642A



208 MAPBGA
(17 x 17 mm)



176 LQFP
(24 x 24 mm)



324 TEPBGA
(23 x 23 mm)

- 150 MHz e200z4 Power Architecture core
 - Variable length instruction encoding (VLE)
 - Superscalar architecture with 2 execution units
 - Up to 2 integer or floating point instructions per cycle
 - Up to 4 multiply and accumulate operations per cycle
- Memory organization
 - 2 MB on-chip flash memory with ECC and read-while-write (RWW)
 - 128 KB on-chip SRAM with standby functionality (32 KB) and ECC
 - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
 - 14 + 3 KB eTPU code and data RAM
 - 4 x 4 crossbar switch (XBAR)
 - 24-entry MMU
- Fail Safe Protection
 - 16-entry Memory Protection Unit (MPU)
 - CRC unit with 3 submodules
 - Junction temperature sensor
- Interrupt
 - Configurable interrupt controller (INTC) with non-maskable interrupt (NMI)
 - 64-channel eDMA
- Serial channels
 - 3 eSCI modules
 - 3 DSPI modules (2 of which support downstream Micro Second Channel [MSC])
 - 3 FlexCAN modules with 64 message buffers each
 - 1 FlexRay module (V2.1) up to 10 Mbit/s w/dual or single channel, 128 message objects, ECC
- 1 eMIOS
 - 24 unified channels
- 1 eTPU2 (second generation eTPU)
 - 32 standard channels
 - 1 reaction module (6 channels with 3 outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
 - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
 - 6 command queues
 - Trigger and DMA support
 - 688 ns minimum conversion time
- On-chip CAN/SCI Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
 - EVTO pin for communication with external tool
- Clock generation
 - On-chip 4–40 MHz main oscillator
 - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 112 general purpose I/O lines
 - Individually programmable as input, output or special function
 - Programmable threshold (hysteresis)
- Power reduction modes: slow, stop, and standby
- Flexible supply scheme
 - 5 V single supply with external ballast
 - Multiple external supply: 5 V, 3.3 V, and 1.2 V

Table of Contents

1	Introduction	3	2.5	Signal details	49
1.1	Document overview	3	3	Electrical characteristics	55
1.2	Description	3	3.1	Parameter classification	55
1.3	Device feature summary	3	3.2	Maximum ratings	56
1.4	Block diagram	5	3.3	Thermal characteristics	58
1.5	Feature details	9	3.3.1	General notes for specifications at maximum junction temperature	59
1.5.1	e200z4 core	9	3.4	EMI (electromagnetic interference) characteristics	61
1.5.2	Crossbar switch (XBAR)	10	3.5	Electrostatic discharge (ESD) characteristics	62
1.5.3	Enhanced direct memory access (eDMA)	10	3.6	Power management control (PMC) and power on reset (POR) electrical specifications	62
1.5.4	Interrupt controller (INTC)	11	3.6.1	Regulator example	65
1.5.5	Memory protection unit (MPU)	11	3.6.2	Recommended power transistors	66
1.5.6	Frequency-modulated phase-locked loop (FMPLL)	12	3.7	Power up/down sequencing	66
1.5.7	System integration unit (SIU)	12	3.8	DC electrical specifications	67
1.5.8	Flash memory	13	3.9	I/O pad current specifications	72
1.5.9	Static random access memory (SRAM)	14	3.9.1	I/O pad V_{RC33} current specifications	73
1.5.10	Boot assist module (BAM)	14	3.9.2	LVDS pad specifications	74
1.5.11	Enhanced modular input/output system (eMIOS)	14	3.10	Oscillator and PLLMRFM electrical characteristics	75
1.5.12	Second generation enhanced time processing unit (eTPU2)	15	3.11	Temperature sensor electrical characteristics	77
1.5.13	Reaction module (REACM)	16	3.12	eQADC electrical characteristics	77
1.5.14	Enhanced queued analog-to-digital converter (eQADC)	17	3.13	Configuring SRAM wait states	79
1.5.15	Deserial serial peripheral interface (DSPI)	18	3.14	Platform flash controller electrical characteristics	80
1.5.16	Enhanced serial communications interface (eSCI)	19	3.15	Flash memory electrical characteristics	80
1.5.17	Controller area network (FlexCAN)	19	3.16	AC specifications	82
1.5.18	FlexRay	20	3.16.1	Pad AC specifications	82
1.5.19	System timers	20	3.17	AC timing	86
1.5.20	Software watchdog timer (SWT)	21	3.17.1	Reset and configuration pin timing	86
1.5.21	Cyclic redundancy check (CRC) module	21	3.17.2	IEEE 1149.1 interface timing	86
1.5.22	Error correction status module (ECSM)	22	3.17.3	Nexus timing	90
1.5.23	Peripheral bridge (PBRIDGE)	22	3.17.4	Calibration bus interface timing	95
1.5.24	Calibration bus interface	22	3.17.5	External interrupt timing (IRQ pin)	99
1.5.25	Power management controller (PMC)	22	3.17.6	eTPU timing	99
1.5.26	Nexus port controller (NPC)	23	3.17.7	eMIOS timing	100
1.5.27	JTAG controller (JTAGC)	23	3.17.8	DSPI timing	100
1.5.28	Development trigger semaphore (DTS)	23	3.17.9	eQADC SSI timing	107
2	Pinout and signal description	23	3.17.10	FlexCAN system clock source	108
2.1	176 LQFP pinout	24	4	Packages	109
2.2	208 MAP BGA ballmap	25	4.1	Package mechanical data	109
2.3	324 TEPBGA ballmap	26	4.1.1	176 LQFP	109
2.4	Signal summary	30	4.1.2	208 MAPBGA	112
			4.1.3	324 TEPBGA	114
			5	Ordering information	116
			6	Document revision history	117

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5642A series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This microcontroller is a 32-bit system-on-chip (SoC) device intended for use in mid-range engine control and automotive transmission control applications.

It is compatible with devices in Freescale's MPC5600 family and offers performance and capabilities beyond the MPC5632M devices.

The microcontroller's e200z4 host processor core is built on the Power Architecture® technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The device has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by a 128 KB on-chip SRAM and a 2 MB internal flash memory.

For development, the device includes a calibration bus that is accessible only when using the Freescale VertiCal Calibration System.

1.3 Device feature summary

Table 1 summarizes the MPC5642A features and compares them to those of the MPC5644A.

Table 1. MPC5642A device feature summary

Feature		MPC5642A	MPC5644A
Process		90 nm	
Core		e200z4	
	SIMD	Yes	
	VLE	Yes	
	Cache	8 KB instruction	
	Non-Maskable Interrupt (NMI)	NMI and Critical Interrupt	
	MMU	24-entry	
	MPU	16-entry	
	Crossbar switch	4 × 4	5 × 4
	Core performance	0–150 MHz	
Windowing software watchdog		Yes	
Core Nexus		Class 3+	
SRAM		128 KB	192 KB
Flash		2 MB	4 MB
Flash fetch accelerator		4 × 128-bit	4 × 256-bit

Table 1. MPC5642A device feature summary (continued)

Feature		MPC5642A	MPC5644A
External bus		None	16-bit (incl. 32-bit muxed)
Calibration bus		16-bit (incl. 32-bit muxed)	
DMA		64 channels	
DMA Nexus		None	
Serial		3	
	eSCI_A	Yes (MSC uplink)	
	eSCI_B	Yes (MSC uplink)	
	eSCI_C	Yes	
CAN		3	
	CAN_A	64 message buffers	
	CAN_B	64 message buffers	
	CAN_C	64 message buffers	
SPI		3	
	Micro Second Channel (MSC) bus downlink	Yes	
	DSPI_A	No	
	DSPI_B	Yes (with LVDS)	
	DSPI_C	Yes (with LVDS)	
	DSPI_D	Yes	
FlexRay		Yes	
System timers		5 PIT channels 4 STM channels 1 Software Watchdog	
eMIOS		24 channels	
eTPU		32-channel eTPU2	
	Code memory	14 KB	
	Data memory	3 KB	
	Reaction module	6 channels	
Interrupt controller		485 channels ¹	
ADC		40 channels	
	ADC_0	Yes	
	ADC_1	Yes	
	Temperature sensor	Yes	
	Variable gain amplifier	Yes	
	Decimation filter	2	
	Sensor diagnostics	Yes	

Table 1. MPC5642A device feature summary (continued)

Feature	MPC5642A	MPC5644A
CRC	Yes	
FMPLL	Yes	
VRC	Yes	
Supplies	5 V, 3.3 V ²	
Low-power modes	Stop mode Slow mode	
Packages	176 LQFP ³ 208 MAPBGA ^{3,4} 324 TEPBGA ⁵ 496-pin CSP ⁶	176 LQFP ³ 208 MAPBGA ^{3,4} 324 TEPBGA ⁵ 496-pin CSP ⁶

¹ 197 interrupt vectors are reserved.

² 5 V single supply only for 176 LQFP

³ Pinout compatible with Freescale's MPC5634M devices

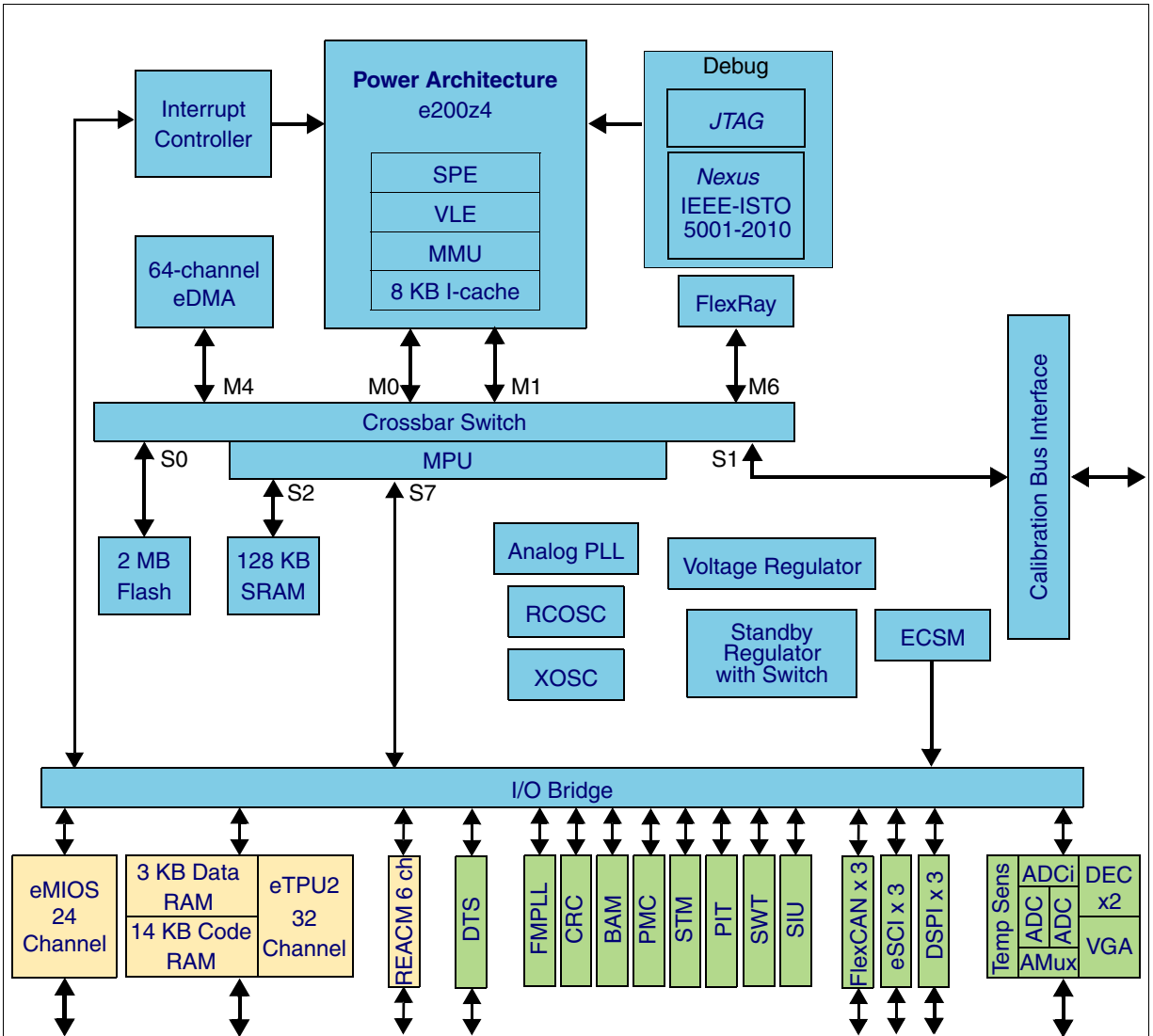
⁴ Pinout compatible with Freescale's MPC5534

⁵ Ballmap upwardly compatible with the standardized package ballmap used for various Freescale MPC563xM family members

⁶ For Freescale VertiCal Calibration System only

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5642A series.



LEGEND

ADC	– Analog to Digital Converter	JTAG	– IEEE 1149.1 Test Controller
ADCi	– ADC interface	MMU	– Memory Management Unit
AMux	– Analog Multiplexer	MPU	– Memory Protection Unit
BAM	– Boot Assist Module	PMC	– Power Management Controller
CRC	– Cyclic Redundancy Check unit	PIT	– Periodic Interrupt Timer
DEC	– Decimation Filter	RCOSC	– Low-speed RC Oscillator
DTS	– Development Trigger Semaphore	REACM	– Reaction Module
DSPI	– Deserial/Serial Peripheral Interface	SIU	– System Integration Unit
ECSM	– Error Correction Status Module	SPE	– Signal Processing Extension
eDMA	– Enhanced Direct Memory Access	SRAM	– Static RAM
eMIOS	– Enhanced Modular Input Output System	STM	– System Timer Module
eSCI	– Enhanced Serial Communications Interface	SWT	– Software Watchdog Timer
eTPU2	– Second gen. Enhanced Time Processing Unit	VGA	– Variable Gain Amplifier
FlexCAN	– Controller Area Network	VLE	– Variable Length (instruction) Encoding
FMPLL	– Frequency-Modulated Phase-Locked Loop	XOSC	– XTAL Oscillator

Figure 1. MPC5642A series block diagram

Table 2 summarizes the functions of the blocks present on the MPC5642A series microcontrollers.

Table 2. MPC5642A series block summary

Block	Function
Boot assist module (BAM)	Block of read-only memory containing executable code that searches for user-supplied boot code and, if none is found, executes the BAM boot code resident in device ROM
Calibration bus interface	Transfers data across the crossbar switch to/from peripherals attached to the calibration system connector
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Crossbar switch (XBAR)	Internal busmaster
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
e200z4 core	Executes programs and interrupt handlers
Enhanced direct memory access (eDMA)	Performs complex data movements with minimal intervention from the core.
Enhanced modular input-output system (eMIOS)	Provides the functionality to generate or measure events
Enhanced queued analog-to-digital converter (eQADC)	Provides accurate and fast conversions for a wide range of applications
Enhanced serial communication interface (eSCI)	Provides asynchronous serial communication capability with peripheral devices and other microcontroller units
Enhanced time processor unit (eTPU2)	Second-generation co-processor processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
Error Correction Status Module (ECSM)	The Error Correction Status Module supports a number of miscellaneous control functions for the platform, and includes registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
Flash memory	Provides storage for program code, constants, and variables
FlexRay	Provides high-speed distributed control for advanced automotive applications
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
Memory protection unit (MPU)	Provides hardware access control for all memory references generated
Nexus port controller (NPC)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2010 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Reaction Module (REACM)	Works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

Table 2. MPC5642A series block summary (continued)

Block	Function
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer
System watchdog timer (SWT)	Provides protection from runaway code
Temperature sensor	Provides the temperature of the device as an analog value

1.5 Feature details

1.5.1 e200z4 core

MPC5642A devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
 - Dedicated branch address calculation adder
 - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
 - 2-cycle load latency
 - Fully pipelined
 - Big and Little endian support
 - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
 - Low power design – extensive clock gating
 - Power saving modes: wait
 - Dynamic power management of execution units, cache and MMU
- Testability
 - Synthesizeable, MuxD scan design
 - ABIST/MBIST for arrays
 - Built-in Parallel Signature Unit

- Calibration support allowing an external tool to modify address mapping

1.5.2 Crossbar switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 4 master ports
 - CPU instruction bus
 - CPU data bus
 - eDMA
 - FlexRay
- 4 slave ports
 - Flash
 - Calibration bus interface
 - SRAM
 - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation minimizes overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
 - Explicit software initiation
 - Initiation via a channel-to-channel linking mechanism for continuous transfers
 - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

1.5.4 Interrupt controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—3 clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
 - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
 - MPU is invalid at reset, thus no access restrictions are enforced
 - 2 types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay) support {read, write} attributes
 - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
 - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only
 - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
 - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the preprogrammed memory region descriptors

- An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
- 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
 - Bypass mode with PLL off
 - Bypass mode with PLL running (default mode out of reset)
 - PLL normal mode
- Each of the 3 modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
 - Modulation enabled/disabled through software
 - Triangle wave modulation up to 100 kHz modulation frequency
 - Programmable modulation depth (0% to 2% modulation depth)
 - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
 - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
 - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 System integration unit (SIU)

The MPC5642A SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
 - MCU reset configuration via external pins
 - Pad configuration control for each pad
 - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
 - Power-on reset support
 - Reset status register provides last reset source to software

- Glitch detection on reset input
- Software controlled reset assertion
- External interrupt
 - Rising or falling edge event detection
 - Programmable digital filter for glitch rejection
 - Critical Interrupt request
 - Non-Maskable Interrupt request
- GPIO
 - Centralized control of I/O and bus pins
 - Virtual GPIO via DSPI serialization (requires external deserialization device)
 - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
 - Allows serial and parallel chaining of DSPIs
 - Allows flexible selection of eQADC trigger inputs
 - Allows selection of interrupt requests between external pins and DSPI
 - From a set of eTPU output channels, allows selection of source signals for decimation filter integrators

1.5.8 Flash memory

The MPC5642A provides 2 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
 - Architected to optimize the performance of the flash
 - Configurable read buffering and line prefetch support
 - 4-entry 128-bit wide line read buffer
 - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (4 words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is 2 consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC

- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.5.9 Static random access memory (SRAM)

The SRAM provides 128 KB of general purpose system SRAM. The first 32 KB block of the SRAM is powered by its own power supply pin only during standby operation.

The SRAM controller includes these features:

- 128 KB data RAM implemented as eight 16 KB (2048 × 78 bits) blocks
- Each 16 KB block has 2 rows repairable (RAMs with internal repair feature)
- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single bit correction, double bit detection

1.5.10 Boot assist module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale and is identical for all MPC5642A MCUs. The BAM program is executed every time the MCU is powered on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (boot code is downloaded into RAM via eSCI or the FlexCAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the MPC5642A hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping of all physical addresses to logical addresses with minimum address translation
- Sets up MMU to allow user boot code to execute as either Power Architecture technology code (default) or as Freescale VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using Freescale protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture technology code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.5.11 Enhanced modular input/output system (eMIOS)

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels

- 3 channels' internal timebases sharable between channels
- 1 timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)
- Each channel (0–23) supports the following functions:
 - General Purpose Input/Output (GPIO)
 - Single Action Input Capture (SAIC)
 - Single Action Output Compare (SAOC)
 - Output Pulse Width Modulation Buffered (OPWMB)
 - Input Period Measurement (IPM)
 - Input Pulse Width Measurement (IPWM)
 - Double Action Output Compare (DOAC)
 - Modulus Counter Buffered (MCB)
 - Output Pulse Width & Frequency Modulation Buffered (OPWFMB)
- Each channel has its own pin (not available on all package types)

1.5.12 Second generation enhanced time processing unit (eTPU2)

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

MPC5642A devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
 - Enhanced input digital filters on the input pins for improved noise immunity
 - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
 - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
 - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
 - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler

- Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
- Both time bases can be exported to the eMIOS timer module
- Both time bases visible from the host
- Event-triggered microengine:
 - Fixed-length instruction execution in two-system-clock microcycle
 - 14 KB of code memory (SCM)
 - 3 KB of parameter (data) RAM (SPRAM)
 - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
 - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
 - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
 - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
 - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
 - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
 - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
 - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host
- Test and development support features:
 - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
 - Software breakpoints
 - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

1.5.14 Enhanced queued analog-to-digital converter (eQADC)

The eQADC block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog-to-digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
 - 2×12 -bit ADC resolution
 - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
 - 12-bit conversion time – 938 ns (1M sample/s)
 - 10-bit conversion time – 813 ns (1.2M sample/s)
 - 8-bit conversion time – 688 ns (1.4M sample/s)
 - Up to 10-bit accuracy at 500K sample/s and 8-bit accuracy at 1M sample/s
 - Differential conversions
 - Single-ended signal range from 0 to 5 V
 - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
 - Provides time stamp information when requested
 - Allows time stamp information relative to eTPU clock sources, such as an angle clock
 - Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
 - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports 4 external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range ($\times 1$, $\times 2$, $\times 4$)
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 k Ω , 100 k Ω , 5 k Ω)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor

- Provides temperature of silicon as an analog value
- Read using an internal ADC analog channel
- May be read with either ADC
- 2 decimation filters
 - Programmable decimation factor (1 to 16)
 - Selectable IIR or FIR filter
 - Up to 4th order IIR or 8th order FIR
 - Programmable coefficients
 - Saturated or non-saturated modes
 - Programmable Rounding (Convergent; Two's Complement; Truncated)
 - Prefill mode to precondition the filter before the sample window opens
 - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
 - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface (SSI) to an external device
 - Free-running clock for use by an external device
 - Supports a 26-bit message length
- Priority based queues
 - Supports 6 queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
 - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
 - Supports software and hardware trigger modes to arm a particular queue
 - Generates interrupt when command coherency is not achieved
- External hardware triggers
 - Supports rising edge, falling edge, high level and low level triggers
 - Supports configurable digital filter

1.5.15 Deserial serial peripheral interface (DSPI)

The DSPI block provides a synchronous serial interface for communication between the MPC5642A MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the MPC5642A MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHz for SOUT and SCK pins for DSPI_B and DSPI_C
- Support for downstream Micro Second Channel (MSC) with Timed Serial Bus (TSB) configuration on DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels, and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI module can generate and check parity in a serial frame

1.5.16 Enhanced serial communications interface (eSCI)

Three eSCI modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
 - Compatible with LIN slaves from revisions 1.x and 2.0 of the LIN standard
 - Autonomous transmission of entire frames
 - Configurable to support all revisions of the LIN standard
 - Automatic parity bit generation
 - Double stop bit after bit error
 - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
 - Idle line wake-up
 - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
 - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.17 Controller area network (FlexCAN)

The MPC5642A MCU includes three FlexCAN blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

The FlexCAN modules provide the following features:

- Based on and including all existing features of the Freescale TouCAN module
- Full Implementation of the CAN protocol specification, Version 2.0B
 - Standard data and remote frames
 - Extended data and remote frames
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of 0 to 8 bytes data length
- Individual Rx Mask Register per message buffer

- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full-featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wakeup on bus activity

1.5.18 FlexRay

The MPC5642A includes one dual-channel FlexRay module that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A. Features include:

- Single channel support
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 message buffers, each configurable as:
 - Receive message buffer
 - Single-buffered transmit message buffer
 - Double-buffered transmit message buffer (combines two single-buffered message buffers)
- 2 independent receive FIFOs
 - 1 receive FIFO per channel
 - Up to 255 entries for each FIFO
- ECC support

1.5.19 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

1.5.19.1 Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system ‘tick’ signals to the operating system, as well as periodic

triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

1.5.19.2 System timer module (STM)

The STM is designed to implement the software task monitor as defined by AUTOSAR¹. It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.20 Software watchdog timer (SWT)

The SWT is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.5.21 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (x25 protocol):
— $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
— $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

1. AUTOSAR: AUTomotive Open System ARchitecture (see <http://www.autosar.org>)