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SPC564A70B4, SPC564A70L7

32-bit Power Architecture® based MCU for automotive powertrain applications

Datasheet – preliminary data

Features

- 150 MHz e200z4 Power Architecture® core
  - Variable length instruction encoding (VLE)
  - Superscalar architecture with 2 execution units
  - Up to 2 integer or floating point instructions per cycle
  - Up to 4 multiply and accumulate operations per cycle
- Memory organization
  - 2 MB on-chip flash memory with ECC and read-while-write (RWW)
  - 128 KB on-chip SRAM with standby functionality (32 KB) and ECC
  - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
  - 14 + 3 KB eTPU code and data RAM
  - 4 × 4 crossbar switch (XBAR)
  - 24-entry MMU
- Fail Safe Protection
  - 16-entry Memory Protection Unit (MPU)
  - CRC unit with 3 submodules
  - Junction temperature sensor
- Interrupt
  - Configurable interrupt controller (INTC) with non-maskable interrupt (NMI)
  - 64-channel eDMA
- Serial channels
  - 3 eSCI modules
  - 3 DSPI modules (2 of which support downstream Micro Second Channel [MSC])
  - 3 FlexCAN modules with 64 message buffers each


PBGA324 (23 mm x 23 mm)


LQFP176 (24 mm x 24 mm)

  - 1 FlexRay module (V2.1) up to 10 Mbit/s w/dual or single channel, 128 message objects, ECC
- 1 eMIOS (24 unified channels)
- 1 eTPU2 (second generation eTPU)
  - 32 standard channels
  - 1 reaction module (6 channels with 3 outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels
  - 688 ns minimum conversion time
- On-chip CAN/SCI Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
- Clock generation
  - On-chip 4–40 MHz main oscillator
  - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 112 general purpose I/O lines
- Power reduction modes: slow, stop, and standby
- Flexible supply scheme
  - 5 V single supply with external ballast
  - Multiple external supply: 5 V, 3.3 V , and 1.2 V
- Designed for LQFP176, LBGA208, PBGA324

Table 1. Device summary

Memory Flash size	Part number		
	Package LQFP176	Package LBGA208	Package PBGA324
2MB	SPC564A70L7	-	SPC564A70B4

Contents

List of tables

List of figures

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC564A70 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This microcontroller is a 32-bit system-on-chip (SoC) device intended for use in mid-range engine control and automotive transmission control applications.

It is compatible with devices in ST's SPC56xx family and offers performance and capability above that of the SPC563M devices.

The microcontroller's e200z4 host processor core is built on the Power Architecture technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The device has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by a 128 KB on-chip SRAM and a 2 MB internal flash memory.

For development, the device includes a calibration bus that is accessible only when using the STMicroelectronics calibration tool.

1.3 Device feature summary

Table 2 summarizes the SPC564A70 features and compares them to those of the SPC564A80.

Table 2. SPC564A70 device feature summary

Feature		SPC564A70	SPC564A80
Process		90 nm	
Core		e200z4	
	SIMD	Yes	
	VLE	Yes	
	Cache	8 KB instruction	
	Non-Maskable Interrupt (NMI)	NMI and Critical Interrupt	
	MMU	24-entry	
	MPU	16-entry	
	Crossbar switch	4 × 4	5 × 4
	Core performance	0–150 MHz	
Windowing software watchdog		Yes	

Table 2. SPC564A70 device feature summary (continued)

Feature		SPC564A70	SPC564A80
Core Nexus		Class 3+	
SRAM		128 KB	192 KB
Flash		2 MB	4 MB
Flash fetch accelerator		4 × 128-bit	4 × 256-bit
External bus		None	16-bit (incl. 32-bit muxed)
Calibration bus		16-bit (incl. 32-bit muxed)	
DMA		64 channels	
DMA Nexus		None	
Serial		3	
	eSCI_A	Yes (MSC uplink)	
	eSCI_B	Yes (MSC uplink)	
	eSCI_C	Yes	
CAN		3	
	CAN_A	64 message buffers	
	CAN_B	64 message buffers	
	CAN_C	64 message buffers	
SPI		3	
	Micro Second Channel (MSC) bus downlink	Yes	
	DSPI_A	No	
	DSPI_B	Yes (with LVDS)	
	DSPI_C	Yes (with LVDS)	
	DSPI_D	Yes	
FlexRay		Yes	
System timers		5 PIT channels 4 STM channels 1 Software Watchdog	
eMIOS		24 channels	
eTPU		32-channel eTPU2	
	Code memory	14 KB	
	Data memory	3 KB	
	Reaction module	6 channels	
Interrupt controller		485 channels(1)	
ADC		40 channels	

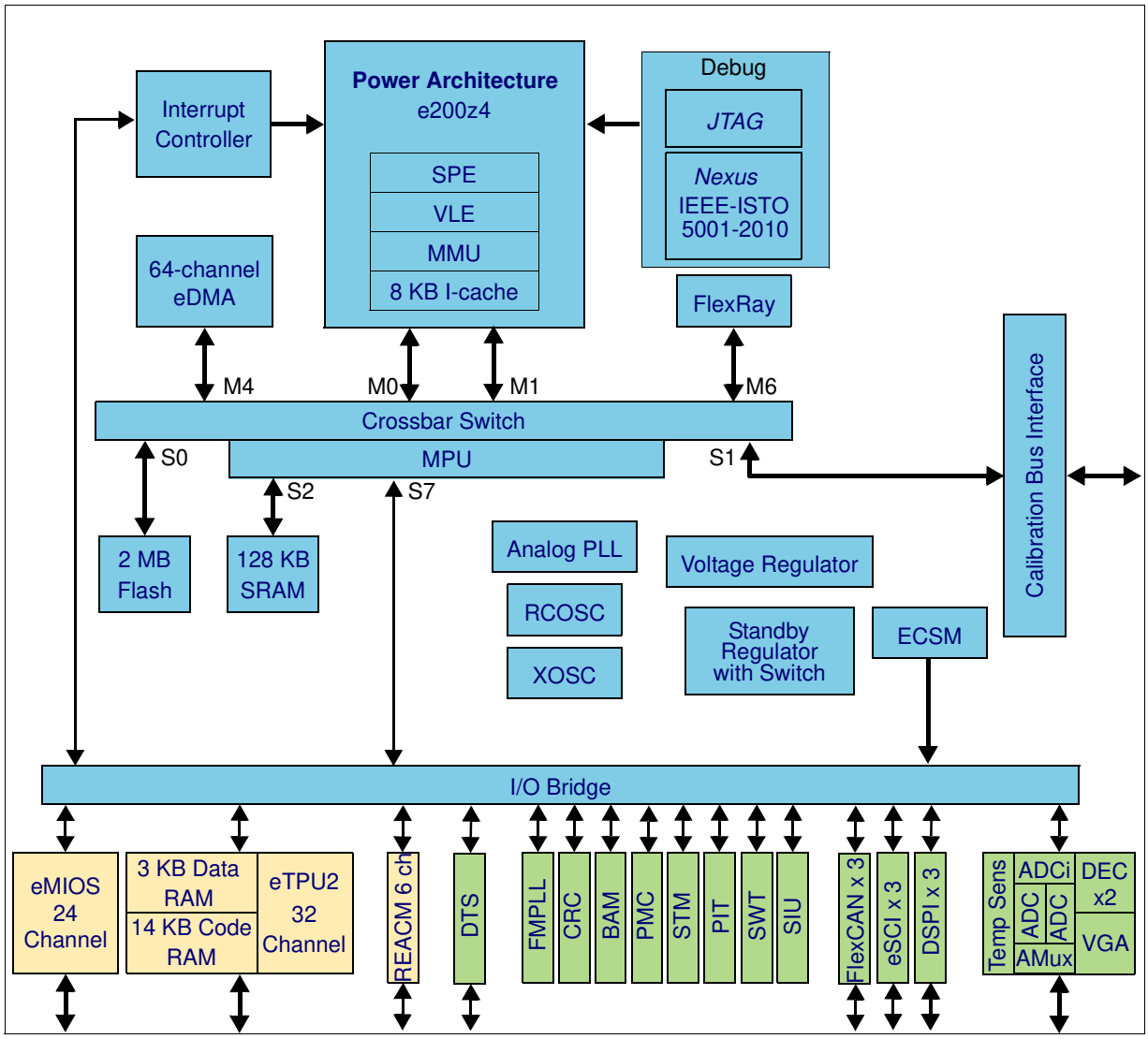
Table 2. SPC564A70 device feature summary (continued)

Feature		SPC564A70	SPC564A80
	ADC_0	Yes	
	ADC_1	Yes	
	Temperature sensor	Yes	
	Variable gain amplifier	Yes	
	Decimation filter	2	
	Sensor diagnostics	Yes	
CRC		Yes	
FMPLL		Yes	
VRC		Yes	
Supplies		5 V, 3.3 V(2)	
Low-power modes		Stop mode Slow mode	
Packages		LQFP176(3) PBGA324 496-pin CSP(4)	LQFP176(3) PBGA324 Known Good Die (KGD) 496-pin CSP(4)

1. 197 interrupt vectors are reserved.
2. 5 V single supply only for LQFP176
3. Pinout compatible with STMicroelectronics' SPC563M64 devices
4. For ST calibration tool only

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC564A70 series.



LEGEND

ADC	– Analog to Digital Converter	**JTAG**	– IEEE 1149.1 Test Controller
ADCi	– ADC interface	**MMU**	– Memory Management Unit
AMux	– Analog Multiplexer	**MPU**	– Memory Protection Unit
BAM	– Boot Assist Module	**PMC**	– Power Management Controller
CRC	– Cyclic Redundancy Check unit	**PIT**	– Periodic Interrupt Timer
DEC	– Decimation Filter	**RCOSC**	– Low-speed RC Oscillator
DTS	– Development Trigger Semaphore	**REACM**	– Reaction Module
DSPI	– Deserial/Serial Peripheral Interface	**SIU**	– System Integration Unit
ECSM	– Error Correction Status Module	**SPE**	– Signal Processing Extension
eDMA	– Enhanced Direct Memory Access	**SRAM**	– Static RAM
eMIOS	– Enhanced Modular Input Output System	**STM**	– System Timer Module
eSCI	– Enhanced Serial Communications Interface	**SWT**	– Software Watchdog Timer
eTPU2	– Second gen. Enhanced Time Processing Unit	**VGA**	– Variable Gain Amplifier
FlexCAN	– Controller Area Network	**VLE**	– Variable Length (instruction) Encoding
FMPLL	– Frequency-Modulated Phase-Locked Loop	**XOSC**	– XTAL Oscillator

Figure 1. SPC564A70 series block diagram

Table 3 summarizes the functions of the blocks present on the SPC564A70 series microcontrollers.

Table 3. SPC564A70 series block summary

Block	Function
Boot assist module (BAM)	Block of read-only memory containing executable code that searches for user-supplied boot code and, if none is found, executes the BAM boot code resident in device ROM
Calibration bus interface	Transfers data across the crossbar switch to/from peripherals attached to the calibration tool connector
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Crossbar switch (XBAR)	Internal busmaster
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
e200z4 core	Executes programs and interrupt handlers
Enhanced direct memory access (eDMA)	Performs complex data movements with minimal intervention from the core.
Enhanced modular input-output system (eMIOS)	Provides the functionality to generate or measure events
Enhanced queued analog-to-digital converter (eQADC)	Provides accurate and fast conversions for a wide range of applications
Enhanced serial communication interface (eSCI)	Provides asynchronous serial communication capability with peripheral devices and other microcontroller units
Enhanced time processor unit (eTPU2)	Second-generation co-processor processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
Error Correction Status Module (ECSM)	The Error Correction Status Module supports a number of miscellaneous control functions for the platform, and includes registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
Flash memory	Provides storage for program code, constants, and variables
FlexRay	Provides high-speed distributed control for advanced automotive applications
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
Memory protection unit (MPU)	Provides hardware access control for all memory references generated
Nexus port controller (NPC)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2010 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers

Table 3. SPC564A70 series block summary (continued)

Block	Function
Reaction Module (REACM)	Works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer
System watchdog timer (SWT)	Provides protection from runaway code
Temperature sensor	Provides the temperature of the device as an analog value

- 150 MHz e200z4 Power Architecture® core
  - Variable length instruction encoding (VLE)
  - Superscalar architecture with 2 execution units
  - Up to 2 integer or floating point instructions per cycle
  - Up to 4 multiply and accumulate operations per cycle
- Memory organization
  - 2 MB on-chip flash memory with ECC and read-while-write (RWW)
  - 128 KB on-chip SRAM with standby functionality (32 KB) and ECC
  - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
  - 14 + 3 KB eTPU code and data RAM
  - 4 × 4 crossbar switch (XBAR)
  - 24-entry MMU
- Fail Safe Protection
  - 16-entry Memory Protection Unit (MPU)
  - CRC unit with 3 submodules
  - Junction temperature sensor
- Interrupt
  - Configurable interrupt controller (INTC) with non-maskable interrupt (NMI)
  - 64-channel eDMA
- Serial channels
  - 3 eSCI modules
  - 3 DSPI modules (2 of which support downstream Micro Second Channel [MSC])
  - 3 FlexCAN modules with 64 message buffers each
  - 1 FlexRay module (V2.1) up to 10 Mbit/s w/dual or single channel, 128 message objects, ECC
- 1 eMIOS
  - 24 unified channels
- 1 eTPU2 (second generation eTPU)
  - 32 standard channels

  - 1 reaction module (6 channels with 3 outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
  - 6 command queues
  - Trigger and DMA support
  - 688 ns minimum conversion time
- On-chip CAN/SCI Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
  - EVTO pin for communication with external tool
- Clock generation
  - On-chip 4–40 MHz main oscillator
  - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 112 general purpose I/O lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Power reduction modes: slow, stop, and standby
- Flexible supply scheme
  - 5 V single supply with external ballast
  - Multiple external supply: 5 V, 3.3 V, and 1.2 V

1.5 Feature details

1.5.1 e200z4 core

SPC564A70 devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability

  - Synthesizeable, MuxD scan design
  - ABIST/MBIST for arrays
  - Built-in Parallel Signature Unit
- Calibration support allowing an external tool to modify address mapping

1.5.2 Crossbar switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 4 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
- 4 slave ports
  - Flash
  - Calibration bus interface
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation minimizes overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count

- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

1.5.4 Interrupt controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—3 clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all

system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - 2 types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the preprogrammed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the 3 modes may be run with a crystal oscillator or an external clock reference

- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 System integration unit (SIU)

The SPC564A70 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin

- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI
  - From a set of eTPU output channels, allows selection of source signals for decimation filter integrators

1.5.8 Flash memory

The SPC564A70 provides 2 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU 'loads', DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support
  - 4-entry 128-bit wide line read buffer
  - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (4 words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is 2 consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.5.9 Static random access memory (SRAM)

The SRAM provides 128 KB of general purpose system SRAM. The first 32 KB block of the SRAM is powered by its own power supply pin only during standby operation.

The SRAM controller includes these features:

- 128 KB data RAM implemented as eight 16 KB (2048 × 78 bits) blocks
- Each 16 KB block has 2 rows repairable (RAMs with internal repair feature)
- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single bit correction, double bit detection

1.5.10 Boot assist module (BAM)

The BAM is a block of read-only memory that is programmed once by ST and is identical for all SPC564A70 MCUs. The BAM program is executed every time the MCU is powered on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (boot code is downloaded into RAM via eSCI or the FlexCAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the SPC564A70 hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping of all physical addresses to logical addresses with minimum address translation
- Sets up MMU to allow user boot code to execute as either Power Architecture technology code (default) or as VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using standard protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture technology code (default) or VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.5.11 Enhanced modular input/output system (eMIOS)

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels
- 3 channels' internal timebases sharable between channels
- 1 timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)
- Each channel (0–23) supports the following functions:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
  - Output Pulse Width Modulation Buffered (OPWMB)
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (DOAC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width & Frequency Modulation Buffered (OPWFMB)
- Each channel has its own pin (not available on all package types)

1.5.12 Second generation enhanced time processing unit (eTPU2)

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

SPC564A70 devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host

- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

1.5.14 Enhanced queued analog-to-digital converter (eQADC)

The eQADC block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog-to-digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of

out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
    12-bit conversion time – 938 ns (1 M sample/s)
    10-bit conversion time – 813 ns (1.2 M sample/s)
    8-bit conversion time – 688 ns (1.4M sample/s)
  - Up to 10-bit accuracy at 500K sample/s and 8-bit accuracy at 1M sample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Allows time stamp information relative to eTPU clock sources, such as an angle clock
  - Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
  - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports 4 external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range (×1, ×2, ×4)
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ, 100 kΩ, 5 kΩ)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor
  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
  - May be read with either ADC
- 2 decimation filters
  - Programmable decimation factor (1 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)