



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





SPC564A74B4, SPC564A74L7, SPC564A80B4, SPC564A80L7

32-bit MCU family built on the embedded Power Architecture®

Features

- 150 MHz e200z4 Power Architecture® core
 - Variable length instruction encoding (VLE)
 - Superscalar architecture with 2 execution units
 - Up to 2 integer or floating point instructions per cycle
 - Up to 4 multiply and accumulate operations per cycle
- Memory organization
 - 4 MB on-chip flash memory with ECC and Read While Write (RWW)
 - 192 KB on-chip RAM with standby functionality (32 KB) and ECC
 - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
 - 14 + 3 KB eTPU code and data RAM
 - 5 × 4 crossbar switch (XBAR)
 - 24-entry MMU
 - External Bus Interface (EBI) with slave and master port
- Fail Safe Protection
 - 16-entry Memory Protection Unit (MPU)
 - CRC unit with 3 sub-modules
 - Junction temperature sensor
- Interrupts
 - Configurable interrupt controller (with NMI)
 - 64-channel DMA
- Serial channels
 - 3 × eSCI
 - 3 × DSPI (2 of which support downstream Micro Second Channel [MSC])



- 3 × FlexCAN with 64 messages each
- 1 × FlexRay module (V2.1) up to 10 Mbit/s with dual or single channel and 128 message objects and ECC
- 1 × eMIOS
- 1 × eTPU2 (second generation eTPU)
- 2 enhanced queued analog-to-digital converters (eQADCs)
- On-chip CAN/SCI/FlexRay Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for the eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
- Clock generation
 - On-chip 4–40 MHz main oscillator
 - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 120 general purpose I/O lines
- Power reduction mode: slow, stop and stand-by modes
- Flexible supply scheme
 - 5 V single supply with external ballast
 - Multiple external supply: 5 V, 3.3 V and 1.2 V
- Designed for LQFP176, LPGA208, PBGA324 and Known Good Die (KGD)

Table 1. Device summary

Memory Flash size	Part number			
	Package LQFP176	Package: LPGA208	Package: PBGA324	KGD
4MB	SPC564A80L7	-	SPC564A80B4	-
3MB	SPC564A74L7	-	SPC564A74B4	-

Contents

1	Introduction	8
1.1	Document Overview	8
1.2	Description	8
1.3	Device comparison	9
1.4	SPC564A80 feature list	11
1.5	Feature details	13
1.5.1	e200z4 core	13
1.5.2	Crossbar Switch (XBAR)	13
1.5.3	eDMA	14
1.5.4	Interrupt controller	14
1.5.5	Memory protection unit (MPU)	15
1.5.6	FMPLL	16
1.5.7	SIU	16
1.5.8	Flash memory	17
1.5.9	BAM	18
1.5.10	eMIOS	19
1.5.11	eTPU2	19
1.5.12	Reaction module	21
1.5.13	eQADC	21
1.5.14	DSPI	23
1.5.15	eSCI	24
1.5.16	FlexCAN	24
1.5.17	FlexRay	26
1.5.18	System timers	26
1.5.19	Software watchdog timer (SWT)	27
1.5.20	Cyclic redundancy check (CRC) module	27
1.5.21	Error correction status module (ECSM)	27
1.5.22	External bus interface (EBI)	28
1.5.23	Calibration EBI	28
1.5.24	Power management controller (PMC)	29
1.5.25	Nexus port controller	29
1.5.26	JTAG	29
1.5.27	Development Trigger Semaphore (DTS)	29
1.6	SPC564A80 series architecture	30

1.6.1	Block diagram	30
1.6.2	Block summary	32
2	Pinout and signal description	34
2.1	LQFP176 pinout	35
2.2	LBGA208 ballmap	36
2.3	PBGA324 ballmap	37
2.4	Signal summary	41
2.5	Signal details	73
3	Electrical characteristics	81
3.1	Parameter classification	81
3.2	Maximum ratings	82
3.3	Thermal characteristics	83
3.3.1	General notes for specifications at maximum junction temperature	85
3.4	EMI (electromagnetic interference) characteristics	88
3.5	Electrostatic discharge (ESD) characteristics	88
3.6	Power management control (PMC) and power on reset (POR) electrical specifications	89
3.6.1	Regulator Example	92
3.6.2	Recommended power transistors	94
3.7	Power up/down sequencing	94
3.8	DC electrical specifications	95
3.9	I/O pad current specifications	101
3.9.1	I/O pad V_{RC33} current specifications	102
3.9.2	LVDS pad specifications	103
3.10	Oscillator and PLLMRFM electrical characteristics	104
3.11	Temperature sensor electrical characteristics	106
3.12	eQADC electrical characteristics	106
3.13	Configuring SRAM wait states	109
3.14	Platform flash controller electrical characteristics	109
3.15	Flash memory electrical characteristics	109
3.16	AC specifications	111
3.16.1	Pad AC specifications	111
3.17	AC timing	114

3.17.1	Reset and configuration pin timing	114
3.17.2	IEEE 1149.1 interface timing	115
3.17.3	Nexus timing	118
3.17.4	External Bus Interface (EBI) and calibration bus interface timing	122
3.17.5	External interrupt timing (IRQ pin)	126
3.17.6	eTPU timing	126
3.17.7	eMIOS timing	127
3.17.8	DSPI timing	127
3.17.9	eQADC SSI timing	135
3.17.10	FlexCAN system clock source	136
4	Packages	137
4.1	ECOPACK	137
4.2	Package mechanical data	138
4.2.1	LQFP176	138
4.2.2	BGA208	141
4.2.3	PBGA324	142
5	Ordering information	145
6	Document revision history	147

List of tables

Table 1.	Device summary	1
Table 2.	SPC564A80, SPC563M64 and SPC564A70 comparison	9
Table 3.	SPC564A80 series block summary	32
Table 4.	SPC564A80 signal properties.	41
Table 5.	Pad types	73
Table 6.	Signal details	73
Table 7.	Power/ground segmentation.	79
Table 8.	Parameter classifications	81
Table 9.	Absolute maximum ratings	82
Table 10.	Thermal characteristics for 176-pin QFP	83
Table 11.	Thermal characteristics for 208-pin LBGA	84
Table 12.	Thermal characteristics for 324-pin PBGA	85
Table 13.	EMI Testing Specifications	88
Table 14.	ESD ratings,	88
Table 15.	PMC Operating Conditions and External Regulators Supply Voltage	89
Table 16.	PMC Electrical Characteristics	89
Table 17.	SPC564A80 External network specification	93
Table 18.	Recommended operating characteristics	94
Table 19.	Power sequence pin states (fast pads).	94
Table 20.	Power sequence pin states (medium, slow, and multi-voltage pads).	94
Table 21.	DC electrical specifications.	95
Table 22.	I/O pad average I_{DDE} specifications	101
Table 23.	I/O pad V_{RC33} average I_{DDE} specifications.	102
Table 24.	V_{RC33} pad average DC current.	103
Table 25.	DSPI LVDS pad specification	103
Table 26.	PLLMRFM electrical specifications.	104
Table 27.	Temperature sensor electrical characteristics	106
Table 28.	eQADC conversion specifications (operating)	106
Table 29.	eQADC single ended conversion specifications (operating).	107
Table 30.	eQADC differential ended conversion specifications (operating)	107
Table 31.	Cutoff frequency for additional SRAM wait state	109
Table 32.	APC, RWSC, WWSC settings vs. frequency of operation.	109
Table 33.	Flash program and erase specifications	109
Table 34.	Flash module life.	110
Table 35.	Pad AC specifications (5.0 V).	111
Table 36.	Pad AC specifications ($V_{DDE} = 3.3$ V)	112
Table 37.	Reset and Configuration Pin Timing	114
Table 38.	JTAG pin AC electrical characteristics	115
Table 39.	Nexus debug port timing.	118
Table 40.	Nexus debug port operating frequency.	121
Table 41.	External Bus Interface maximum operating frequency	122
Table 42.	Calibration bus interface maximum operating frequency	122
Table 43.	External bus interface (EBI) and calibration bus operation timing	122
Table 44.	External interrupt timing	126
Table 45.	eTPU timing	126
Table 46.	eMIOS timing	127
Table 47.	DSPI channel frequency support	127
Table 48.	DSPI timing.	127

Table 49.	eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)	135
Table 50.	FlexCAN engine system clock divider threshold.	136
Table 51.	FlexCAN engine system clock divider	136
Table 52.	LQFP176 package mechanical data.	140
Table 53.	LBGA208 mechanical data.	141
Table 54.	PBGA324 package mechanical data	144
Table 55.	Order codes	145
Table 56.	Revision history	147

List of figures

Figure 1.	SPC564A80 series block diagram	31
Figure 2.	176-pin LQFP pinout (top view)	35
Figure 3.	208-pin LBGA package ballmap (viewed from above)	36
Figure 4.	324-pin PBGA package ballmap (northwest, viewed from above)	37
Figure 5.	324-pin PBGA package ballmap (southwest, viewed from above)	38
Figure 6.	324-pin PBGA package ballmap (northeast, viewed from above)	39
Figure 7.	324-pin PBGA package ballmap (southeast, viewed from above)	40
Figure 8.	Core voltage regulator controller external components preferred configuration	93
Figure 9.	Pad output delay	113
Figure 10.	Reset and Configuration Pin Timing	114
Figure 11.	JTAG test clock input timing	116
Figure 12.	JTAG test access port timing	116
Figure 13.	JTAG JCOMP timing	117
Figure 14.	JTAG boundary scan timing	118
Figure 15.	Nexus output timing	119
Figure 16.	Nexus event trigger and test clock timings	120
Figure 17.	Nexus TDI, TMS, TDO timing	120
Figure 18.	CLKOUT timing	123
Figure 19.	Synchronous output timing	124
Figure 20.	Synchronous input timing	125
Figure 21.	ALE signal timing	125
Figure 22.	External Interrupt Timing	126
Figure 23.	DSPI classic SPI timing — master, CPHA = 0	129
Figure 24.	DSPI classic SPI timing — master, CPHA = 1	130
Figure 25.	DSPI classic SPI timing — slave, CPHA = 0	131
Figure 26.	DSPI classic SPI timing — slave, CPHA = 1	131
Figure 27.	DSPI modified transfer format timing — master, CPHA = 0	132
Figure 28.	DSPI modified transfer format timing — master, CPHA = 1	132
Figure 29.	DSPI modified transfer format timing — slave, CPHA = 0	133
Figure 30.	DSPI modified transfer format timing — slave, CPHA = 1	134
Figure 31.	DSPI PCS strobe (PCSS) timing	134
Figure 32.	eQADC SSI timing	135
Figure 33.	LQFP176 package mechanical drawing	139
Figure 34.	PBGA324 package mechanical drawing	143
Figure 35.	Product code structure	146

1 Introduction

1.1 Document Overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC564A80 series of microcontroller units (MCUs). For functional characteristics, refer to the *SPC564A80 Microcontroller Reference Manual*.

1.2 Description

The microcontroller's e200z4 host processor core is built on Power Architecture technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The SPC564A80 has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by 192 KB on-chip SRAM and 4 MB of internal flash memory. The SPC564A80 includes an external bus interface, and also a calibration bus that is only accessible when using the calibration tools.

This document describes the features of the SPC564A80 and highlights important electrical and physical characteristics of the device.

1.3 Device comparison

[Table 2](#) summarizes the SPC564A80 and compares it to the SPC563M64.

Table 2. SPC564A80, SPC563M64 and SPC564A70 comparison

Feature		SPC564A80	SPC563M64	SPC564A70
Process		90 nm		
Core		e200z4	e200z3	e200z4
	SIMD	Yes		
	VLE	Yes		
	Cache	8 KB instruction	No	8 KB instruction
	Non-Maskable Interrupt (NMI)	NMI & Critical Interrupt		
	MMU	24 entry	16 entry	24 entry
	MPU	16 entry	No	16 entry
	Crossbar switch	5 × 4	3 × 4	4 × 4
	Core performance	0–150 MHz	0–80 MHz	0–150 MHz
Windowing software watchdog		Yes		
Core Nexus		Class 3+	Class 2+	Class 3+
SRAM		192 KB	94 KB	128 KB
Flash		4 MB	1.5 MB	2 MB
Flash fetch accelerator		4 × 256-bit	4 × 128-bit	
External bus		16-bit (incl 32-bit muxed)	None	
Calibration bus		16-bit (incl 32-bit muxed)	16-bit	16-bit (incl 32-bit muxed)
DMA		64 ch.	32 ch.	64 ch.
DMA Nexus		None		
Serial		3	2	3
	eSCI_A	Yes (MSC Uplink)		
	eSCI_B	Yes (MSC Uplink)		
	eSCI_C	Yes	No	Yes
CAN		3	2	3
	CAN_A	64 buf		
	CAN_B	64 buf	No	64 buf
	CAN_C	64 buf	32 buf	64 buf
SPI		3	2	3

Table 2. SPC564A80, SPC563M64 and SPC564A70 comparison (continued)

Feature		SPC564A80	SPC563M64	SPC564A70
	Micro Second Channel (MSC) bus downlink	Yes		
	DSPI_A	No		
	DSPI_B	Yes (with LVDS)		
	DSPI_C	Yes (with LVDS)		
	DSPI_D	Yes	No	Yes
FlexRay		Yes	No	Yes
System timers		5 PIT channels 4 STM channels 1 Software Watchdog		
eMIOS		24 ch.	16 ch.	24 ch.
eTPU		32 ch. eTPU2		
	Code memory	14 KB		
	Data memory	3 KB		
Interrupt controller		486 ch. ⁽¹⁾	307 ch.	486 ch. ⁽¹⁾
ADC		40 ch.	34 ch.	40 ch.
	ADC_A	Yes		
	ADC_B	Yes		
	Temp sensor	Yes		
	Variable gain amp.	Yes		
	Decimation filter	2	1	2
	Sensor diagnostics	Yes		
CRC		Yes	No	Yes
FMPLL		Yes		
VRC		Yes		
Supplies		5 V, 3.3 V ⁽²⁾	5 V, 3.3 V ⁽³⁾	5 V, 3.3 V ⁽²⁾
Low-power modes		Stop Mode Slow Mode		
Packages		LQFP176 ⁽⁴⁾ LBGA208 ⁽⁴⁾ PBGA Known Good Die (KGD) 496-pin CSP ⁽⁵⁾	LQFP100 LQFP144 LQFP176 LBGA208 496-pin CSP ⁽⁵⁾	LQFP176 ⁽⁴⁾ LBGA208 ⁽⁴⁾ PBGAKnown Good Die (KGD) 496-pin CSP ⁽⁵⁾

1. 199 interrupt vectors are reserved.

2. 5 V single supply only for LQFP176.

3. 5 V single supply only for LQFP144 and LQFP100.

4. Pinout compatible with STMicroelectronics' SPC563M64 devices.

5. For ST calibration tool only.

1.4 SPC564A80 feature list

- 150 MHz e200z4 Power Architecture core
 - Variable length instruction encoding (VLE)
 - Superscalar architecture with 2 execution units
 - Up to 2 integer or floating point instructions per cycle
 - Up to 4 multiply and accumulate operations per cycle
- Memory organization
 - 4 MB on-chip flash memory with ECC and Read While Write (RWW)
 - 192 KB on-chip SRAM with standby functionality (32 KB) and ECC
 - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
 - 14 + 3 KB eTPU code and data RAM
 - 5 × 4 crossbar switch (XBAR)
 - 24-entry MMU
 - External Bus Interface (EBI) with slave and master port
- Fail Safe Protection
 - 16-entry Memory Protection Unit (MPU)
 - CRC unit with 3 sub-modules
 - Junction temperature sensor
- Interrupts
 - Configurable interrupt controller (with NMI)
 - 64-channel DMA
- Serial channels
 - 3 × eSCI
 - 3 × DSPI (2 of which support downstream Micro Second Channel [MSC])
 - 3 × FlexCAN with 64 messages each
 - 1 × FlexRay module (V2.1) up to 10 Mbit/s with dual or single channel and 128 message objects and ECC
- 1 × eMIOS: 24 unified channels
- 1 × eTPU2 (second generation eTPU)
 - 32 standard channels
 - 1 × reaction module (6 channels with three outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
 - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
 - 6 command queues
 - Trigger and DMA support
 - 688 ns minimum conversion time
- On-chip CAN/SCI/FlexRay Bootstrap loader with Boot Assist Module (BAM)
- Nexus
 - Class 3+ for the e200z4 core
 - Class 1 for the eTPU
- JTAG (5-pin)

- Development Trigger Semaphore (DTS)
 - Register of semaphores (32-bits) and an identification register
 - Used as part of a triggered data acquisition protocol
 - EVTO pin is used to communicate to the external tool
- Clock generation
 - On-chip 4–40 MHz main oscillator
 - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 120 general purpose I/O lines
 - Individually programmable as input, output or special function
 - Programmable threshold (hysteresis)
- Power reduction mode: slow, stop and stand-by modes
- Flexible supply scheme
 - 5 V single supply with external ballast
 - Multiple external supply: 5 V, 3.3 V and 1.2 V
- Packages
 - LQFP176
 - LBGA208
 - PBGA324
 - Known Good Die (KGD)
 - 496-pin CSP (calibration tool only)

1.5 Feature details

1.5.1 e200z4 core

SPC564A80 devices have a high performance e200z448n3 core processor:

- Dual issue, 32-bit Power Architecture embedded category CPU
- Variable Length Encoding Enhancements
- 8 KB instruction cache: 2- or 4- way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory management unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool

1.5.2 Crossbar Switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between five master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 5 master ports
 - CPU instruction bus
 - CPU data bus
 - eDMA
 - FlexRay
 - External Bus Interface

- 4 slave ports
 - Flash
 - Calibration and EBI bus
 - SRAM
 - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
 - Explicit software initiation
 - Initiation via a channel-to-channel linking mechanism for continuous transfers
 - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

1.5.4 Interrupt controller

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By

providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
 - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
 - MPU is invalid at reset, thus no access restrictions are enforced
 - Two types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay, and EBI¹) support {read, write} attributes
 - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
 - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only^(a)
 - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
 - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the pre-programmed memory region descriptors

- An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
- 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Three modes of operation
 - Bypass mode with PLL off
 - Bypass mode with PLL running (default mode out of reset)
 - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
 - Modulation enabled/disabled through software
 - Triangle wave modulation up to 100 kHz modulation frequency
 - Programmable modulation depth (0% to 2% modulation depth)
 - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
 - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
 - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 SIU

The SPC564A80 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The

a. EBI not available on all packages and is not available, as a master, for customer.

GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
 - MCU reset configuration via external pins
 - Pad configuration control for each pad
 - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
 - Power-on reset support
 - Reset status register provides last reset source to software
 - Glitch detection on reset input
 - Software controlled reset assertion
- External interrupt
 - Rising or falling edge event detection
 - Programmable digital filter for glitch rejection
 - Critical Interrupt request
 - Non-Maskable Interrupt request
- GPIO
 - Centralized control of I/O and bus pins
 - Virtual GPIO via DSPI serialization (requires external deserialization device)
 - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
 - Allows serial and parallel chaining of DSPIs
 - Allows flexible selection of eQADC trigger inputs
 - Allows selection of interrupt requests between external pins and DSPI

1.5.8 Flash memory

The SPC564A80 provides up to 4 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU 'loads', DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128- and 256-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
 - Architected to optimize the performance of the flash
 - Configurable read buffering and line prefetch support

- Four-entry 256-bit wide line read buffer
- Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (four words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.5.9 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by ST and is identical for all SPC564A80 MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on external bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the SPC564A80 hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping of all physical addresses to logical addresses with minimum address translation
- Sets up MMU to allow user boot code to execute as either Power Architecture embedded category (default) or as VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using standard protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or VLE code

- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.5.10 eMIOS

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels
- 3 channels' internal timebases can be shared between channels
- 1 Timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)

Each channel (0–23) supports the following functions:

- General-purpose input/output (GPIO)
- Single-action input capture (SAIC)
- Single-action output compare (SAOC)
- Output pulse-width modulation buffered (OPWMB)
- Input period measurement (IPM)
- Input pulse-width measurement (IPWM)
- Double-action output compare (DAOC)
- Modulus counter buffered (MCB)
- Output pulse width and frequency modulation buffered (OPWFMB)

1.5.11 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

SPC564A80 devices feature the second generation of the eTPU, called eTPU2.

Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.

- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
 - Enhanced input digital filters on the input pins for improved noise immunity
 - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
 - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
 - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
 - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
 - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
 - Both time bases can be exported to the eMIOS timer module
 - Both time bases visible from the host
- Event-triggered microengine:
 - Fixed-length instruction execution in two-system-clock microcycle
 - 14 KB of code memory (SCM)
 - 3 KB of parameter (data) RAM (SPRAM)
 - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
 - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
 - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
 - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
 - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel

- SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
- Hardware implementation of four semaphores support coherent parameter sharing between both eTPU engines
- Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
 - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
 - Software breakpoints
 - SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.12 Reaction module

The reaction module provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The reaction module has the following features:

- Six reaction channels
- Each channel output is a bus of three signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions

1.5.13 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command 'queues' to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features

include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
 - $2 \times$ 12-bit ADC resolution
 - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
 - 12-bit conversion time: 938 ns (1 M sample/sec)
 - 10-bit conversion time: 813 ns (1.2 M sample/second)
 - 8-bit conversion time: 688 ns (1.4 M sample/second)
 - Up to 10-bit accuracy at 500 KSample/s and 8-bit accuracy at 1 MSample/s
 - Differential conversions
 - Single-ended signal range from 0 to 5 V
 - Variable gain amplifiers on differential inputs ($\times 1$, $\times 2$, $\times 4$)
 - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
 - Provides time stamp information when requested
 - Allows time stamp information relative to eTPU clock sources, such as an angle clock
 - Parallel interface to eQADC CFIFOs and RFIFOs
 - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports four external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 k Ω , 100 k Ω , 5 k Ω)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor
 - Provides temperature of silicon as an analog value
 - Read using an internal ADC analog channel
 - May be read with either ADC
- 2 Decimation Filters
 - Programmable decimation factor (1 to 16)
 - Selectable IIR or FIR filter
 - Up to 4th order IIR or 8th order FIR
 - Programmable coefficients

- Saturated or non-saturated modes
- Programmable Rounding (Convergent; Two's Complement; Truncated)
- Prefill mode to precondition the filter before the sample window opens
- Supports Multiple Cascading Decimation Filters to implement more complex filter designs
- Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface to an external device
 - Free-running clock for use by an external device
 - Supports a 26-bit message length
- Priority based queues
 - Supports six queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
 - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
 - Supports software and hardware trigger modes to arm a particular queue
 - Generates interrupt when command coherency is not achieved
- External hardware triggers
 - Supports rising edge, falling edge, high level and low level triggers
 - Supports configurable digital filter

1.5.14 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the SPC564A80 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the SPC564A80 MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHz for SOUT and SCK pins for DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI Module can generate and check parity in a serial frame

1.5.15 eSCI

Three enhanced serial communications interface (eSCI) modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
 - Autonomous transmission of entire frames
 - Configurable to support all revisions of the LIN standard
 - Automatic parity bit generation
 - Double stop bit after bit error
 - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
 - Idle line wake-up
 - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
 - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.16 FlexCAN

The SPC564A80 MCU includes three controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
 - Standard data and remote frames
 - Extended data and remote frames
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity