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Freescale Semiconductor
Data Sheet: Advance Information

Document Number: MPC5674F
Rev. 10.1, 06/2015

RoHS

MPC5674F

MPC5674F Microcontroller Data Sheet

Covers: MPC5674F and MPC5673F


TEPBGA–416
27mm x 27mm


TEPBGA–516
27mm x 27mm


TEPBGA–324
23mm x 23mm

- Dual issue, 32-bit CPU core complex (e200z7)
  - Compliant with the Power Architecture® embedded category
  - 16 KB I-Cache and 16 KB D-Cache
  - Includes an instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - Includes signal processing extension (SPE2) instruction support for digital signal processing (DSP) and single-precision floating point operations
- 4 MB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 256 KB on-chip general-purpose SRAM including 32 KB of standby RAM
- Two direct memory access controller (eDMA2) blocks
  - One supporting 64 channels
  - One supporting 32 channels
- Interrupt controller (INTC)
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- External bus interface (EBI) for calibration and application development (not available on all packages)
- System integration unit (SIU)
- Error correction status module (ECSM)
- Boot assist module (BAM) supports serial bootload via CAN or SCI
- Two second-generation enhanced time processor units (eTPU2) that share code and data RAM.
  - 32 standard channels per eTPU2
  - 24 KB code RAM
  - 6 KB parameter (data) RAM
- Enhanced modular input output system supporting 32 unified channels (eMIOS) with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Four enhanced queued analog-to-digital converters (eQADC)
  - Support for 64 analog channels
  - Includes one absolute reference ADC channel
  - Includes eight decimation filters
- Four deserial serial peripheral interface (DSPI) modules
- Three enhanced serial communication interface (eSCI) modules
- Four controller area network (FlexCAN) modules
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003/5001-2008 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller regulates supply voltage down to 1.2 V for core logic

freescale™ semiconductor

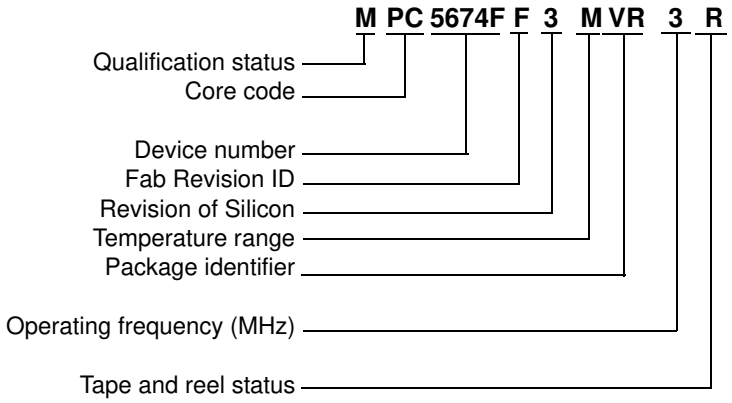
Table of Contents

1 Ordering Information

1.1 Orderable Parts

Figure 1 and Table 1 describe and list the orderable part numbers for the MPC5674F.

Note: Not all options are available on all devices. Refer to Table 1.



Temperature Range
M = –40 °C to 125 °C

Package Identifier
VZ = 324 BGA Pb-free
VR = 416 BGA Pb-free
VY = 516 BGA Pb-free
VV = 516 BGA SnPb

Operating Frequency
2 = 200 MHz
3 = 264 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Revision of Silicon
3 = Rev 3 (ATMC)
0 = Rev 0 (TSMC14)

Fab Revision ID
F = ATMC
K = TSMC14

Figure 1. MPC5674F Orderable Part Number Description

Table 1. Orderable Part Numbers

Freescale Part Number	Package Description	Speed (MHz)[1]		Operating Temperature[2]	
		Nominal	Max[3] (f_{MAX})	Min (T_L)	Max (T_H)
SPC5674FK0MVR3	416 PBGA, no EBI, Pb-free	264	270	–40 °C	125 °C
SPC5674FK0MVY3	516 PBGA, w/EBI, Pb-free	264	270	–40 °C	125 °C
SPC5674FK0MVV3R	516 PBGA, w/EBI, SnPb	264	270	–40 °C	125 °C
SPC5674FK0MVV3	516 PBGA, w/EBI, SnPb	264	200	–40 °C	125 °C
SPC5674FK0MVY3R	516 PBGA, w/EBI, Pb-free	264	270	–40 °C	125 °C
SPC5674FK0MVY3	516 PBGA, w/EBI, Pb-free	264	270	–40 °C	125 °C
SPC5673FK0MVR2R	416 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C
SPC5673FK0MVR2	416 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C
SPC5673FK0MVV2R	324 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C
SPC5673FK0MVV2	324 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C

1 For the operating mode frequency of various blocks on the device, see Table 28.

2 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

3 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

1.2 MPC567xF Family Differences

Table 2 lists the differences between the MPC567xF devices. Refer to the *MPC5674F Reference Manual* for a full feature list and comparison.

Table 2. MPC567xF Family Differences

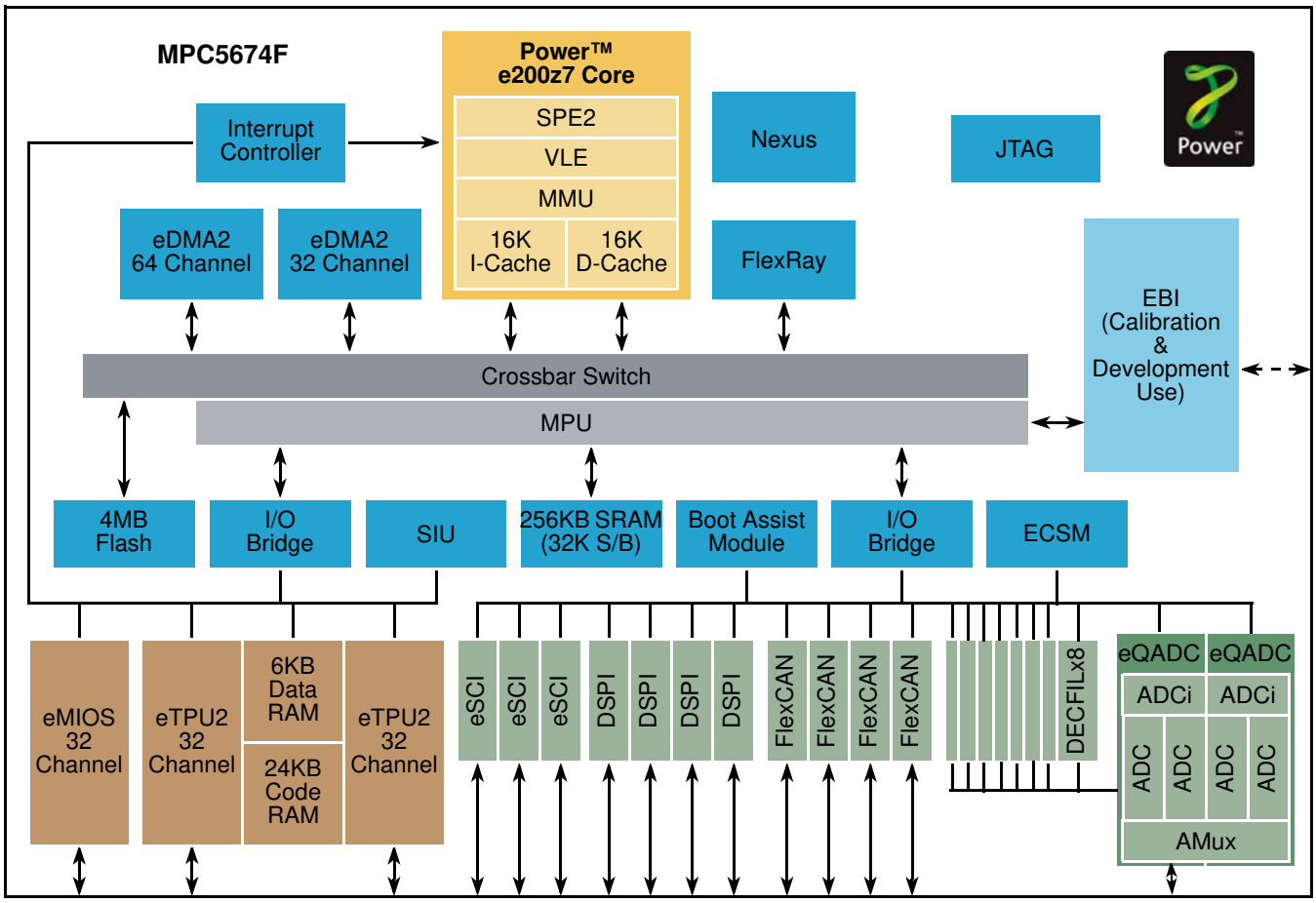
Feature	MPC5674F	MPC5674F	MPC5673F	MPC5673F
Package	416 BGA 516 BGA	324 BGA	416 BGA 516 BGA	324 BGA
Flash	4 MB	4 MB	3 MB	3 MB
SRAM	256 KB	256 KB	192 KB	192 KB
External bus	Yes (516 BGA only)	No	Yes (516 BGA only)	No
Serial	3	2	3	2
eSCI_A	Yes	Yes	Yes	Yes
eSCI_B	Yes	Yes	Yes	Yes
eSCI_C	Yes	No	Yes	No
SPI	4	3	4	3
DSPI_A	Yes	No	Yes	No
DSPI_B	Yes	Yes	Yes	Yes
DSPI_C	Yes	Yes	Yes	Yes
DSPI_D	Yes	Yes	Yes	Yes
eMIOS	32 channel	22 channel	32 channel	22 channel
eTPU2	64 channel	47 channel	64 channel	47 channel
eTPU_A	Yes (32 ch)	Yes (26 ch)	Yes	Yes (26 ch)
eTPU_B	Yes (32 ch)	Yes (21 ch, no TCRCLK)	Yes	Yes (21 ch, no TCRCLK)
ADC	64 channel	48 channel	64 channel	48 channel
eQADC_A	Yes (64 ch)[1]	Yes (24 ch)	Yes (64 ch)[1]	Yes (24 ch)
eQADC_B		Yes (24 ch)		Yes (24 ch)

1 There are are two pairs of 24 channels plus 16 shared channels. This gives 64 channels total: 40 per ADC (since 16 are shared).

2 MPC5674F Blocks

2.1 Block Diagram

Figure 2 shows a top-level block diagram of the MPC5674F device.



LEGEND

ADC	– Analog to digital convertor	**eSCI**	– Enhanced serial communications interface
ADCi	– ADC interface	**eTPU2**	– Enhanced time processing unit 2
AMux	– Analog multiplexer	**FlexCAN**	– Controller area network
DECFIL	– Decimation filter	**MMU**	– Memory management unit
DSPI	– Deserial/serial peripheral interface	**MPU**	– Memory protection unit
EBI	– External bus interface	**S/B**	– Stand-by
ECSM	– Error correction status module	**SIU**	– System integration unit
eDMA2	– Enhanced direct memory access	**SPE2**	– Signal processing engine 2
eMIOS	– Enhanced modular I/O system	**SRAM**	– General-purpose static RAM
eQADC	– Enhanced queued A/D converter module	**VLE**	– Variable length instruction encoding

Figure 2. Block Diagram

3 Pin Assignments

The figures in this section show the primary pin function. For the full signal properties and muxing table, see Appendix A, Signal Properties and Muxing.

3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

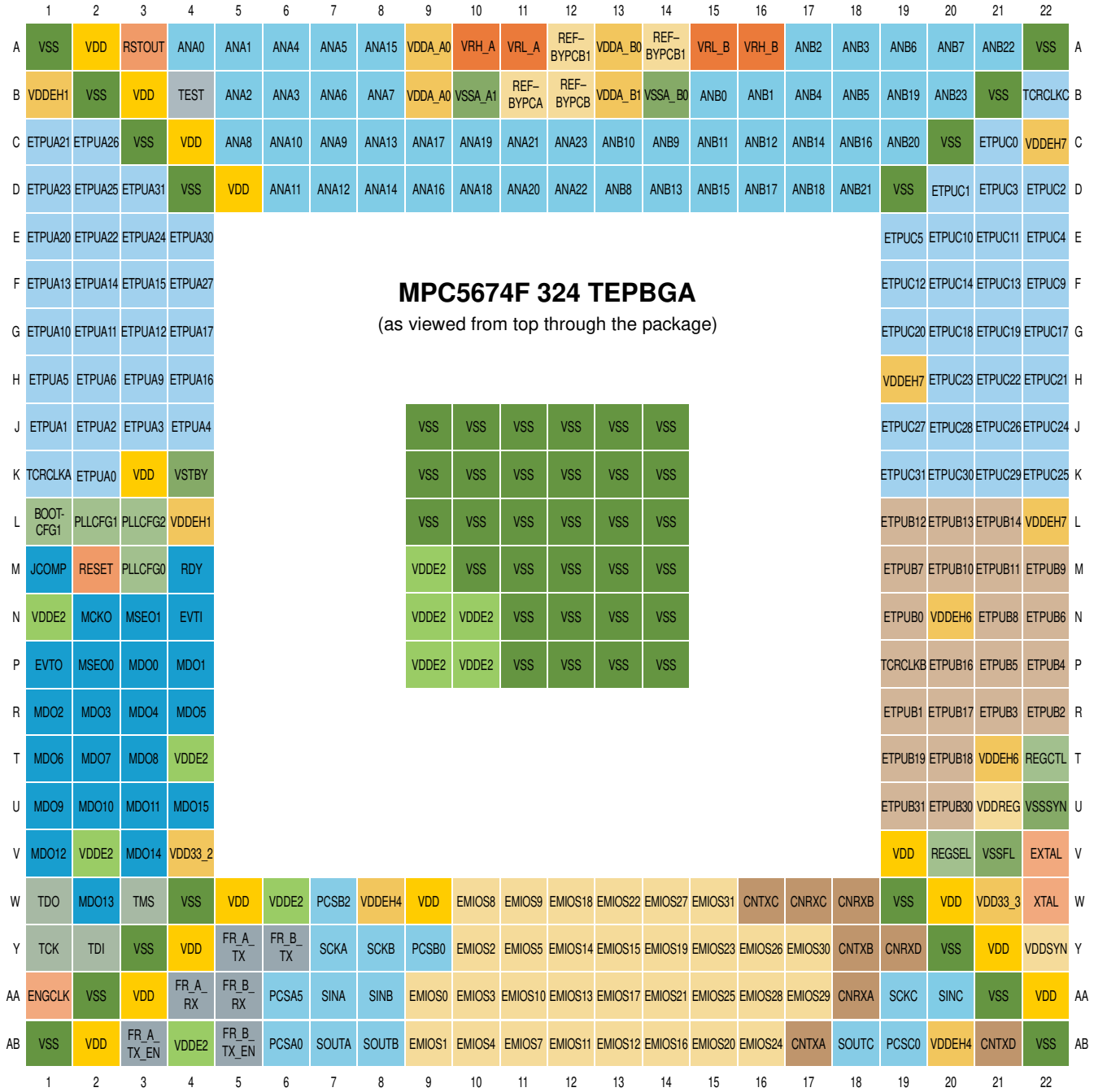


Figure 3. MPC5674F 324-ball TEPBGA (full diagram)

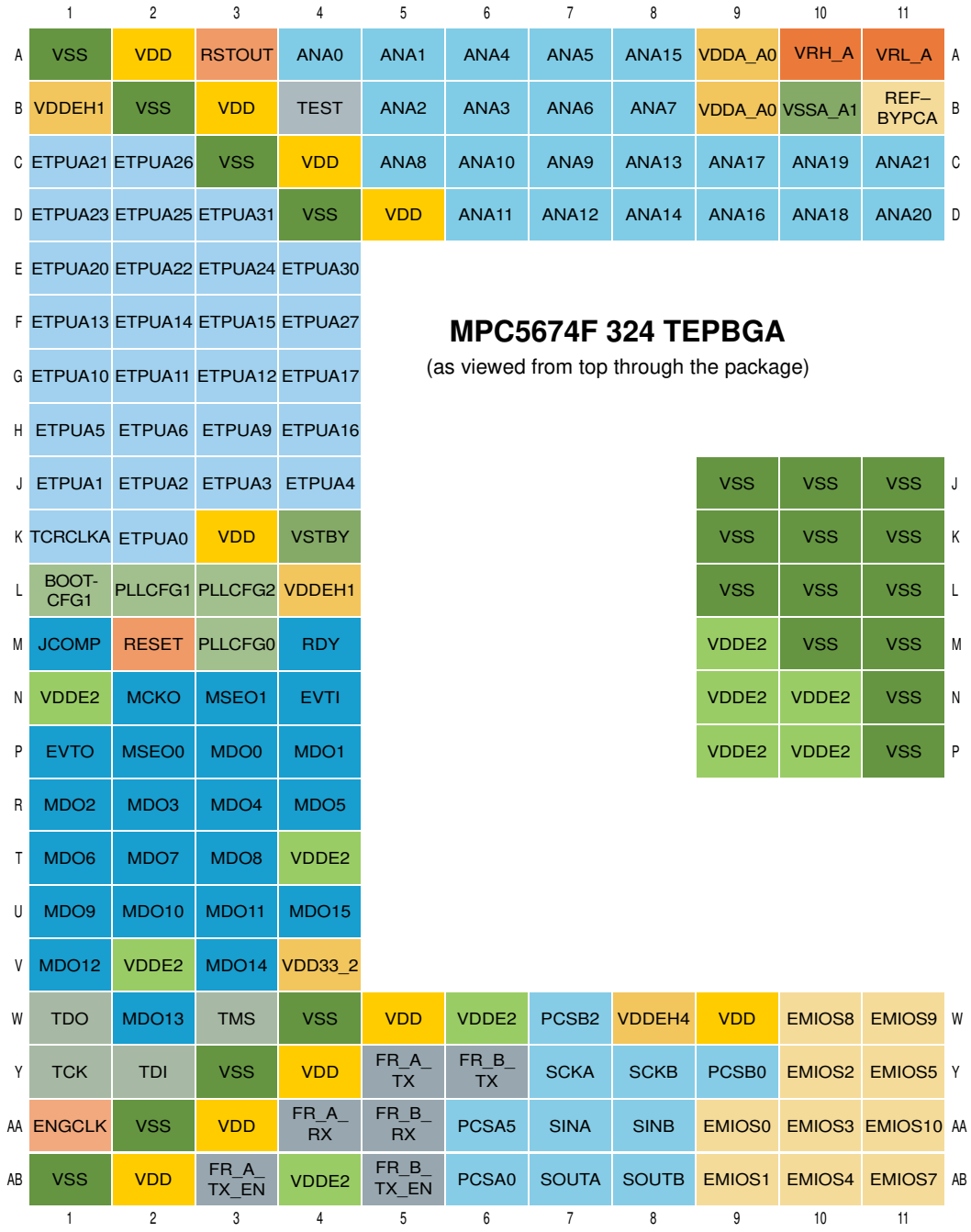


Figure 4. MPC5674F 324-ball TEPBGA (1 of 2)

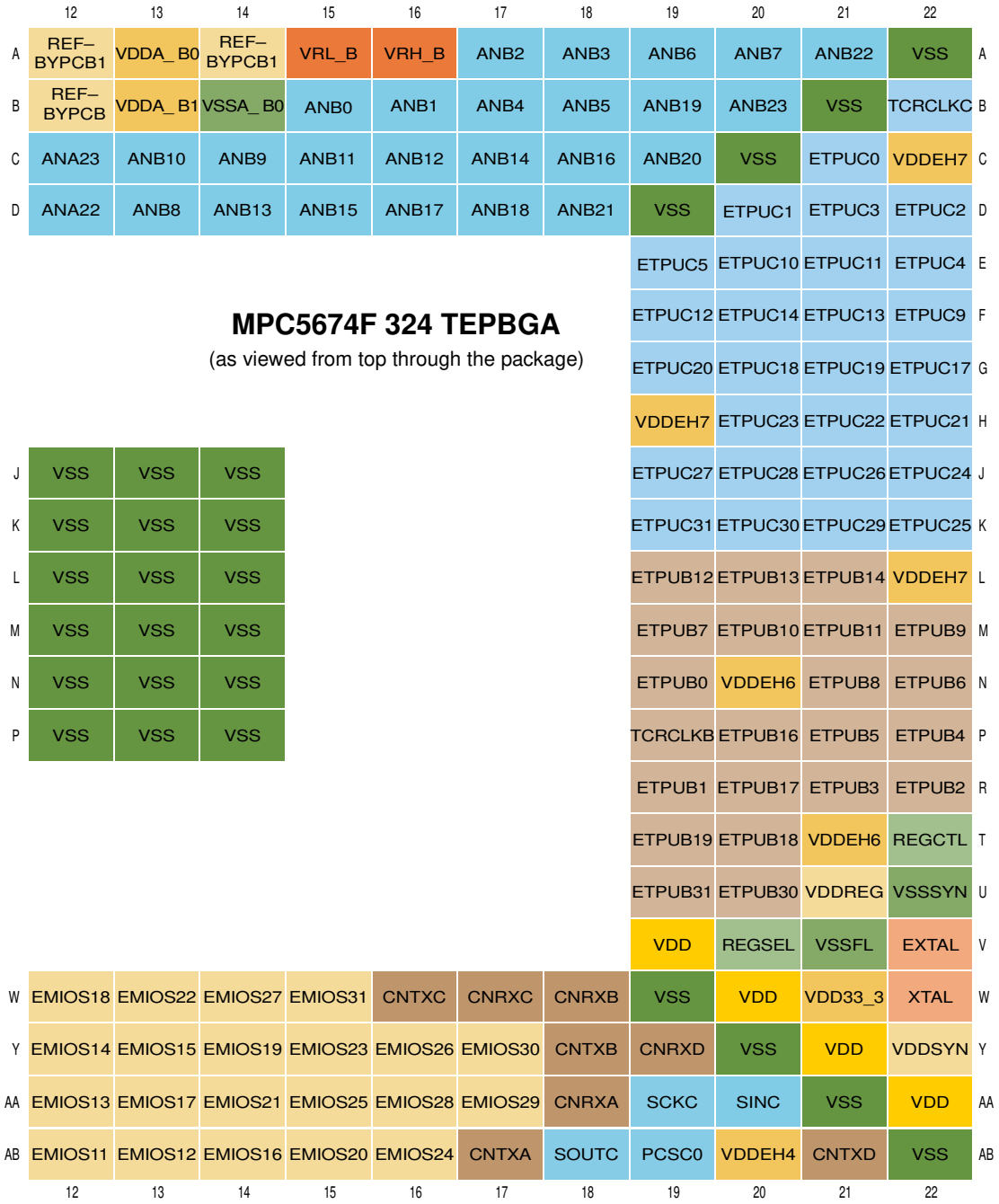


Figure 5. MPC5674F 324-ball TEPBGA (2 of 2)

3.2 416-ball TEPBGA Pin Assignments

Figure 6 shows the 416-ball TEPBGA pin assignments in one figure. The same information is shown in Figure 7 through Figure 10.

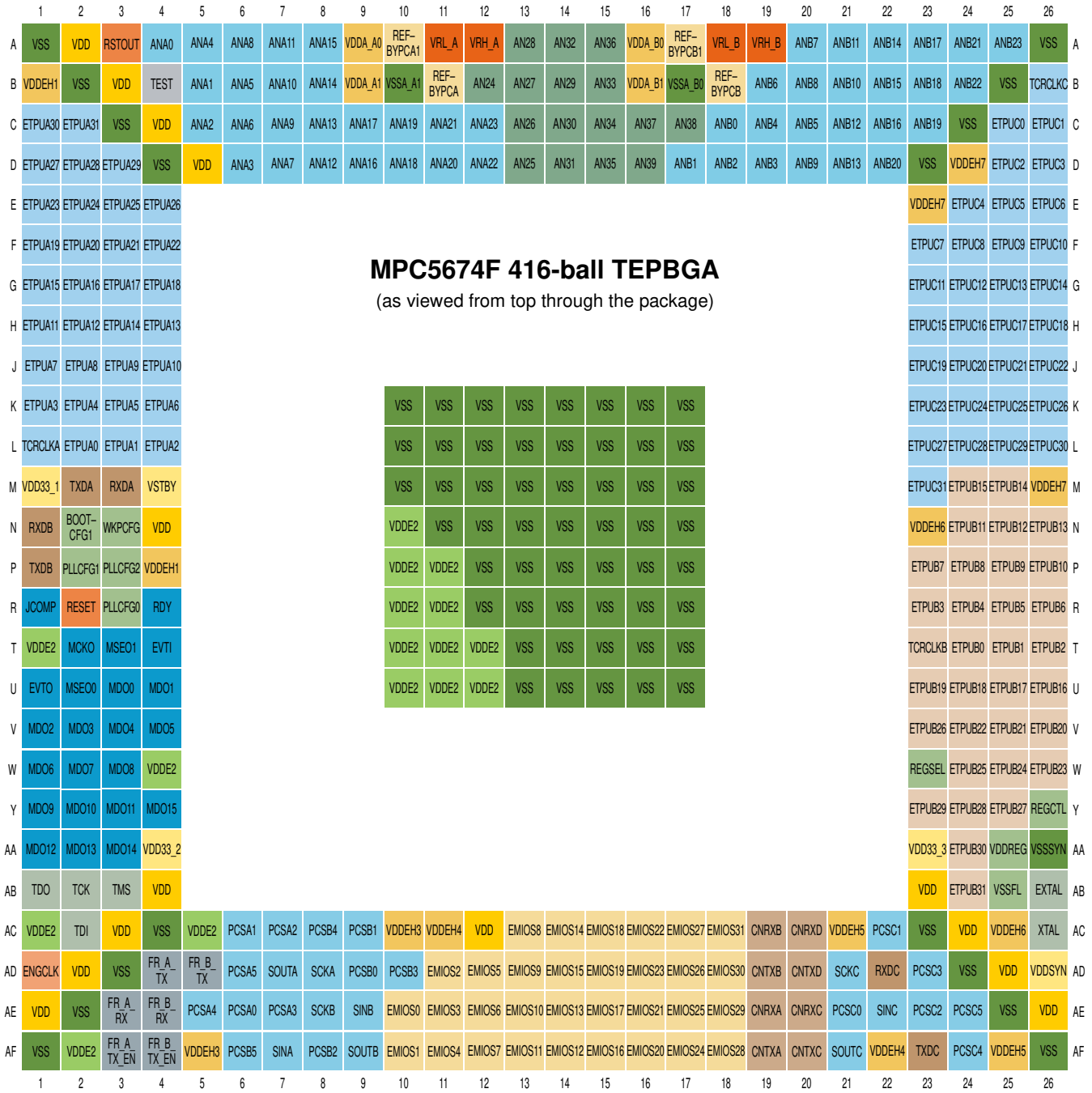
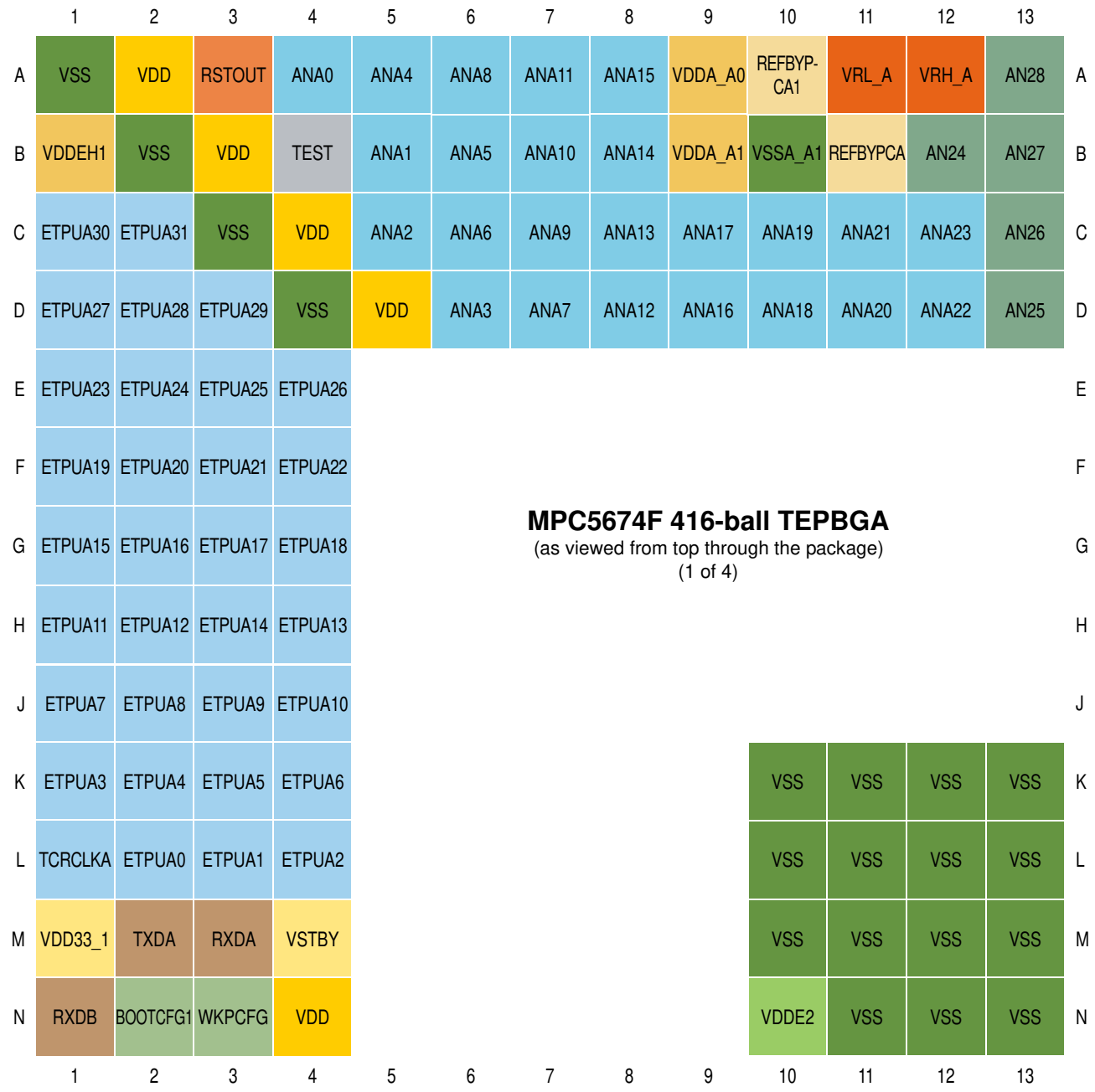
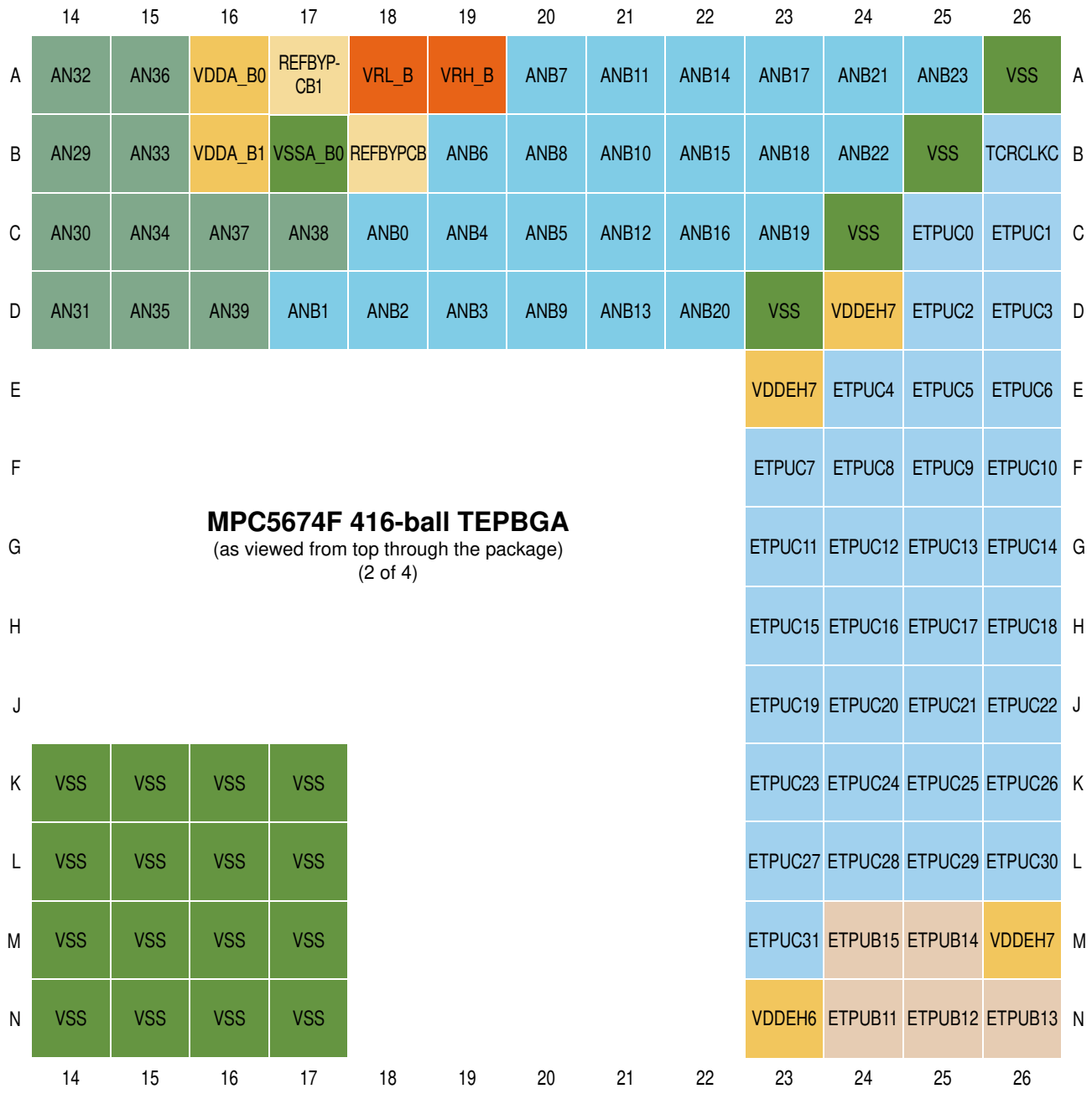


Figure 6. MPC5674F 416-ball TEPBGA (full diagram)



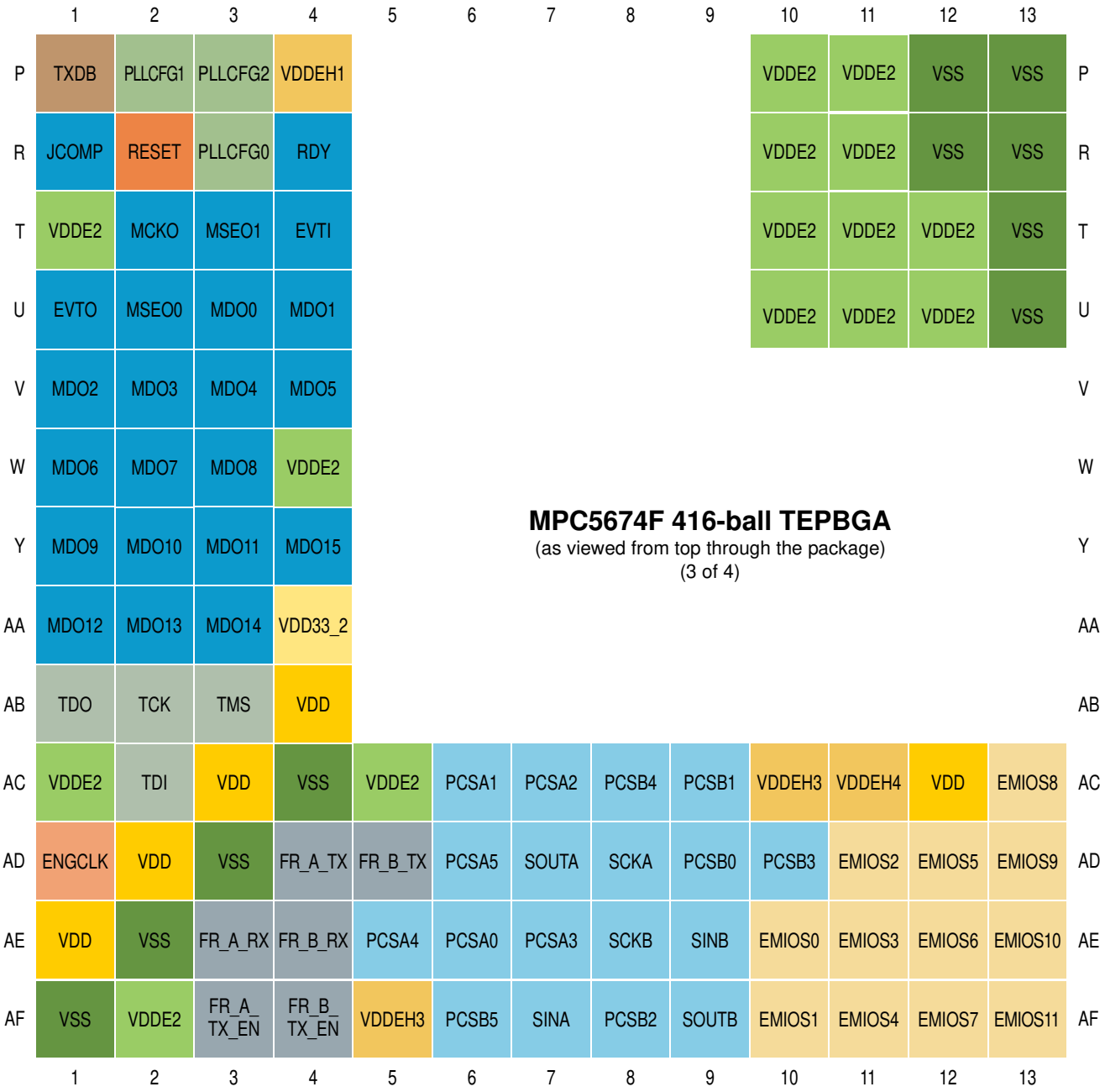
	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	VSS	VDD	RSTOUT	ANA0	ANA4	ANA8	ANA11	ANA15	VDDA_A0	REFBYP-CA1	VRL_A	VRH_A	AN28	A
B	VDDEH1	VSS	VDD	TEST	ANA1	ANA5	ANA10	ANA14	VDDA_A1	VSSA_A1	REFBYPCA	AN24	AN27	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2	ANA6	ANA9	ANA13	ANA17	ANA19	ANA21	ANA23	AN26	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3	ANA7	ANA12	ANA16	ANA18	ANA20	ANA22	AN25	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26										E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22										F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18										G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13										H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10										J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	L
M	VDD33_1	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	M
N	RXDB	BOOTCFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 7. MPC5674F 416-ball TEPBGA (1 of 4)



	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN32	AN36	VDDA_B0	REFBYP-CB1	VRL_B	VRH_B	ANB7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	AN29	AN33	VDDA_B1	VSSA_B0	REFBYPCB	ANB6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	AN30	AN34	AN37	AN38	ANB0	ANB4	ANB5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	AN31	AN35	AN39	ANB1	ANB2	ANB3	ANB9	ANB13	ANB20	VSS	VDDEH7	ETPUC2	ETPUC3	D
E										VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F										ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G										ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H										ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J										ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 8. MPC5674F 416-ball TEPBGA (2 of 4)



	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	U
V	MDO2	MDO3	MDO4	MDO5										V
W	MDO6	MDO7	MDO8	VDDE2										W
Y	MDO9	MDO10	MDO11	MDO15										Y
AA	MDO12	MDO13	MDO14	VDD33_2										AA
AB	TDO	TCK	TMS	VDD										AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 9. MPC5674F 416-ball TEPBGA (3 of 4)

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

3.3 516-ball TEPBGA Pin Assignments

Figure 11 shows the 516-ball TEPBGA pin assignments in one figure. The same information is shown split into four quadrants in Figure 12 through Figure 15.

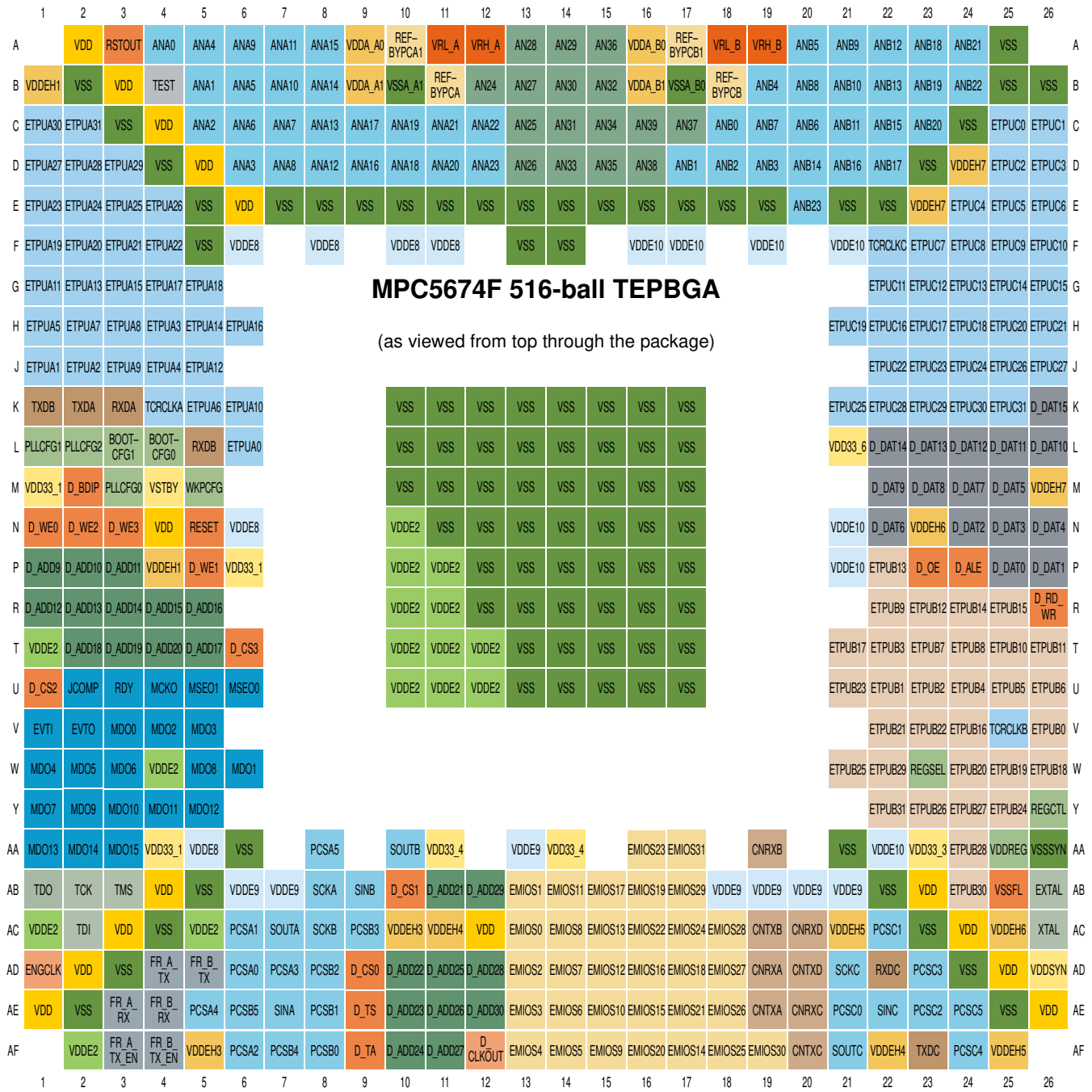


Figure 11. MPC5674F 516-ball TEPBGA (full diagram)

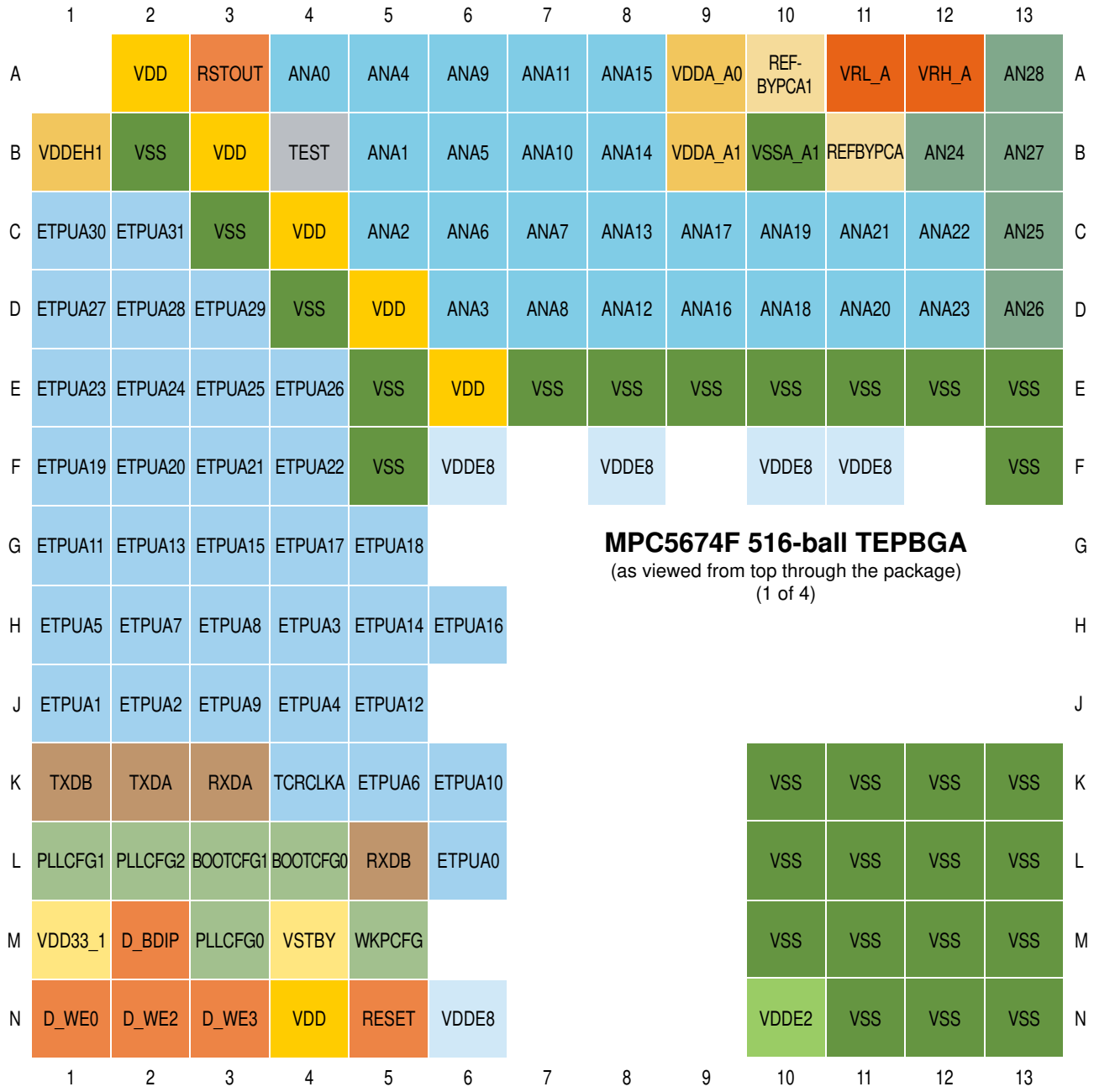
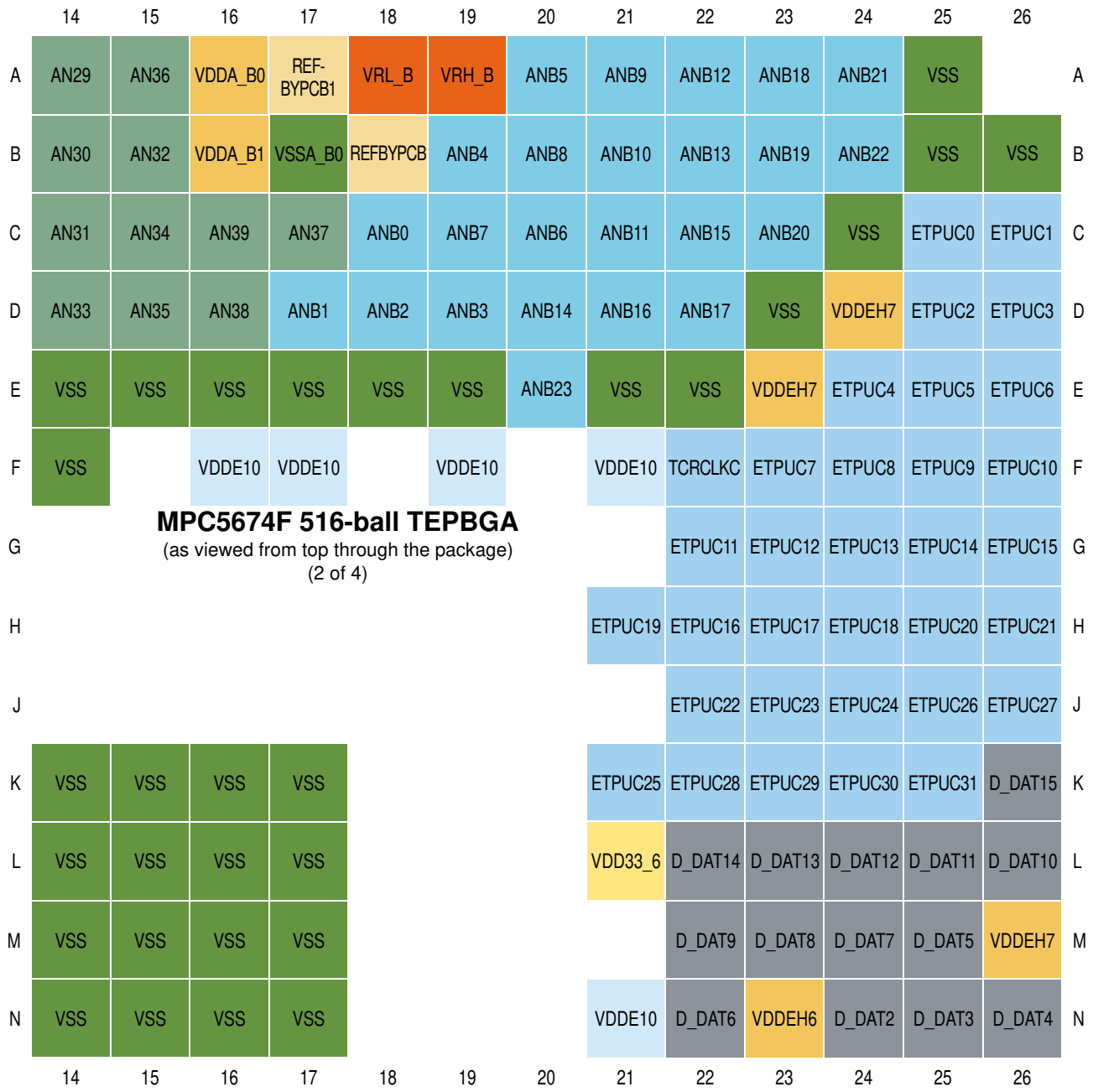
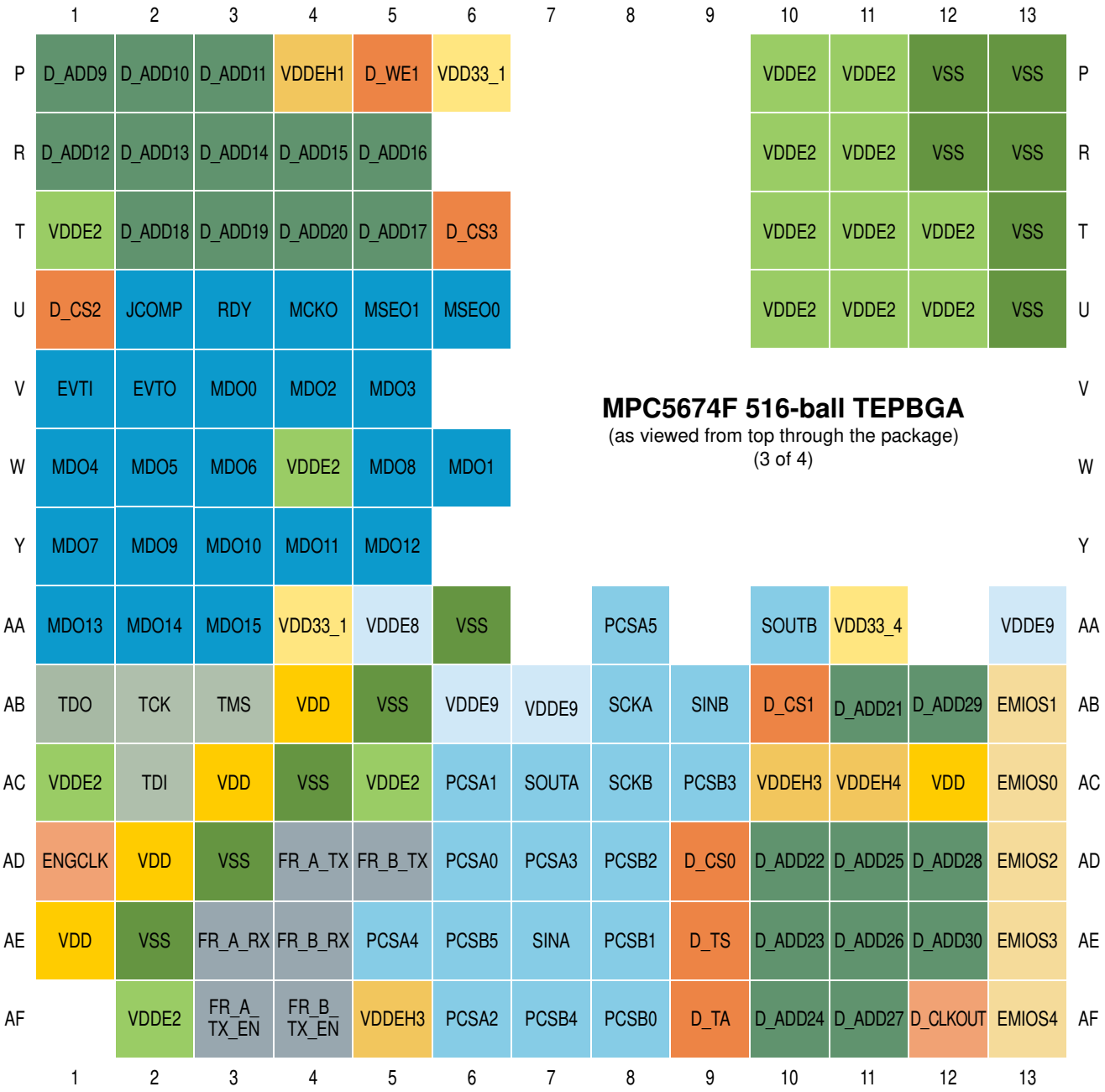


Figure 12. MPC5674F 516-ball TEPBGA (1 of 4)



	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN29	AN36	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	AN30	AN32	VDDA_B1	VSSA_B0	REFBYPCB	ANB4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	AN31	AN34	AN39	AN37	ANB0	ANB7	ANB6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	AN33	AN35	AN38	ANB1	ANB2	ANB3	ANB14	ANB16	ANB17	VSS	VDDEH7	ETPUC2	ETPUC3	D
E	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G									ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H								ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J									ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	VSS	VSS	VSS	VSS				VDD33_6	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 13. MPC5674F 516-ball TEPBGA (2 of 4)



	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	VDD33_1				VDDE2	VDDE2	VSS	VSS	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	U
V	EVTI	EVTO	MDO0	MDO2	MDO3									V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1								W
Y	MDO7	MDO9	MDO10	MDO11	MDO12									Y
AA	MDO13	MDO14	MDO15	VDD33_1	VDDE8	VSS		PCSA5		SOUTB	VDD33_4		VDDE9	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	AE
AF		VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 14. MPC5674F 516-ball TEPBGA (3 of 4)

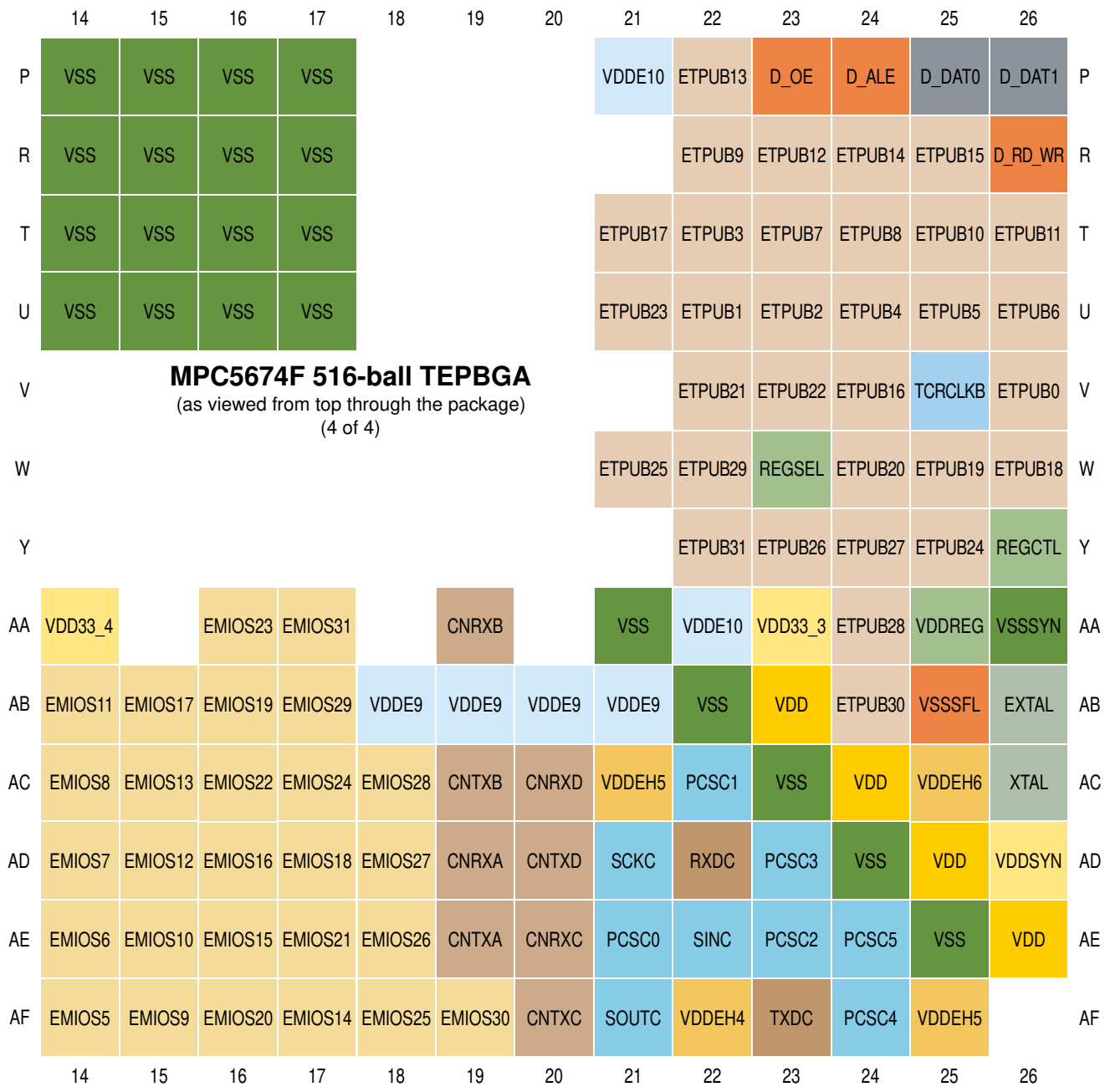


Figure 15. MPC5674F 516-ball TEPBGA (4 of 4)

3.4 Signal Properties and Muxing

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5674F.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

4.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage	V_{DD}	–0.3	2.0 [2]	V
2	SRAM Standby Voltage	V_{STBY}	–0.3	6.4 [3,4]	V
3	Clock Synthesizer Voltage	V_{DDSYN}	–0.3	5.3 [4,5]	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	–0.3	5.3 [4,5]	V
5	Analog Supply Voltage (reference to V_{SSA}[6])	V_{DDA}[7]	–0.3	6.4 [3,4]	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	–0.3	5.3 [4,5]	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	–0.3	6.4 [3,4]	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	–0.3	6.4 [3,4]	V
9	Analog Reference High Voltage (reference to V_{RL}[8])	V_{RH}[9]	–0.3	6.4 [3,4]	V
10	V_{SS} to V_{SSA}[8] Differential Voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	–0.3	6.4 [3,4]	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} – V_{DDSYN}$	–0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
15	Maximum Digital Input Current [10] (per pin, applies to all digital pins)	I_{MAXD}	–3 [11]	3 [11]	mA
16	Maximum Analog Input Current [12] (per pin, applies to all analog pins)	I_{MAXA}	– 3 [7]	3 [7,11]	mA
17	Maximum Operating Temperature Range [13] – Die Junction Temperature	T_J	–40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	–55.0	150.0	°C
19	Maximum Solder Temperature [14] Pb-free package SnPb package	T_{sdr}	 — —	 260.0 245.0	°C
20	Moisture Sensitivity Level [15]	MSL	—	3	—

[1] Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

[2] 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

[3] 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

[4] Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

[5] 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

[6] MPC5674F has two analog power supply pins on the pinout: VDDA_A and VDDA_B.

[7] MPC5674F has two analog ground supply pins on the pinout: VSSA_A and VSSA_B.

[8] MPC5674F has two analog low reference voltage pins on the pinout: VRL_A and VRL_B.

[9] MPC5674F has two analog high reference voltage pins on the pinout: VRH_A and VRH_B.

[10] Total injection current for all pins must not exceed 25 mA at maximum operating voltage.

[11] Injection current of ±5 mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or V_{DDEH} supply when under this stress condition.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Lifetime operation at these specification limits is not guaranteed.

[14] Solder profile per CDF-AEC-Q100.

[15] Moisture sensitivity per JEDEC test method A112.

4.2 Thermal Characteristics

Table 4. Thermal Characteristics, 416-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	24	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	19	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	14	°C/W
Junction to Board [5]	$R_{\theta JB}$	9	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

[2] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[3] Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

[4] Per JEDEC JESD51-6 with the board horizontal.

[5] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[6] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

[7] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 5. Thermal Characteristics, 516-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	25	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	20	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
Junction to Board [5]	$R_{\theta JB}$	10	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 6. Thermal Characteristics, 324-pin Package[1]

MPC5674F Thermal Characteristic	Symbol	Value	Unit
Junction to ambient [2, 3], natural convection (one-layer board)	$R_{\theta JA}$	29	°C/W
Junction to ambient [1, 4], natural convection (four-layer board 2s2p)	$R_{\theta JA}$	19	°C/W
Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	23	°C/W
Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	16	°C/W
Junction to board [5] (four-layer board 2s2p)	$R_{\theta JB}$	10	°C/W
Junction to case [6]	$R_{\theta JC}$	7	°C/W
Junction to package top [7], natural convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.3 EMI (Electromagnetic Interference) Characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to www.freescale.com and perform a keyword search for “radiated emissions.” The following tables list the values of the device's radiated emissions operating behaviors.

Table 7. EMC Radiated Emissions Operating Behaviors: 416 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	26	dBµV	1
				50–150	30		
				150–500	34		
				500–1000	30		
				IEC and SAE level	I[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK off FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	24	dBµV	1
				50–150	25		
				150–500	25		
				500–1000	21		
				IEC and SAE level	K[5]	—	1,3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 I = 36 dBµV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 "FM on" = FM depth of ±2%

5 K = 30 dBµV

Table 8. EMC Radiated Emissions Operating Behaviors: 516 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBµV	1
				50–150	48		
				150–500	48		
				500–1000	47		
				IEC and SAE level	G[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBµV	1
				50–150	44		
				150–500	41		
				500–1000	36		
				IEC and SAE level	G[2]	—	1, 3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 G = 48 dBµV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 "FM on" = FM depth of ±2%

4.4 ESD Characteristics

Table 9. ESD Ratings[1,2]

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.5 PMC/POR/LVI Electrical Specifications

Note: For ADC internal resource measurements, see Table 21 in Section 4.9.1, "ADC Internal Resource Measurements."