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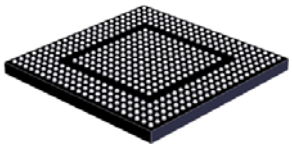
Freescale Semiconductor
Data Sheet: Technical Data

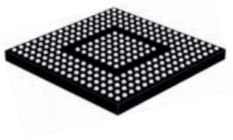
Document Number: MPC5675K
Rev. 8, 10/2013

MPC5675K

Qorivva MPC5675K Microcontroller Data Sheet



473 MAPBGA
(19 x 19 mm)



257 MAPBGA
(14 x 14 mm)

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the Qorivva MPC5675K series of microcontroller units (MCUs).

1.2 Description

The Qorivva MPC5675K microcontroller, a SafeAssure solution, is a 32-bit embedded controller designed for advanced driver assistance systems with RADAR, CMOS imaging, LIDAR and ultrasonic sensors, and multiple 3-phase motor control applications as in hybrid electric vehicles (HEV) in automotive and high temperature industrial applications.

A member of Freescale Semiconductor's Qorivva MPC5500/5600 family, it contains the Book E compliant Power Architecture® technology core with Variable Length Encoding (VLE). This core complies with the Power Architecture embedded category, and is 100 percent user mode compatible with the original Power PC™ user instruction set architecture (UISA). It offers system performance up to four times that of its MPC5561 predecessor, while bringing you the reliability and familiarity of the proven Power Architecture technology.

A comprehensive suite of hardware and software development tools is available to help simplify and speed system design. Development support is available from leading tools vendors providing compilers, debuggers and simulation development environments.

1.3 Device comparison

Table 1. MPC5675K family device comparison

Features		MPC5673K	MPC5674K	MPC5675K
CPU	Type	2 × e200z7d (SoR[1]) in lock-step or decoupled operation		
	Architecture	Harvard		
	Execution speed	0–150 MHz (+2% FM)	0–180 MHz (+2% FM)	0–180 MHz (+2% FM)
	Nominal platform frequency (in 1:1, 1:2, and 1:3 modes)	0–75 MHz (+2% FM)	0–90 MHz (+2% FM)	0–90 MHz (+2% FM)
	MMU	64 entries (SoR)		
	Instruction set PPC	Yes		
	Instruction set VLE	Yes		
	Instruction cache	16 KB, 4-way with EDC (SoR)		
	Data cache	16 KB, 4-way with Parity (SoR)		
	MPU	Yes (SoR)		
Buses	Core bus	32-bit address, 64-bit data		
	Internal periphery bus	32-bit address, 32-bit data		
XBAR	Master × slave ports	Yes (SoR)		
Memory	Static RAM (SRAM)	256 KB (ECC)	384 KB (ECC)	512 KB (ECC)
	Code flash memory	1 MB[2] (ECC)	1.5 MB[2] (ECC)	2 MB[2] (ECC)
	Data flash memory	64 KB[2] (ECC)		
Modules	Analog-to-Digital Converter (ADC)	257 pin pkg: 4 × 12 bit (22 external channels) 473 pin pkg: 4 × 12 bit (up to 34 external channels)		
	CRC unit	2 (3 contexts each)		
	Cross Triggering Unit (CTU)	2 modules		
	Deserial Serial Peripheral Interface (DSPI)	2 modules (3 chip selects)[3]	3 modules[4]	
	Digital I/Os	≥ 16		
	DRAM Controller (DRAMC)	No	Yes[5]	
	Enhanced Direct Memory Access (eDMA)	2 modules, 32 channels each		
	eTimer	3 modules, 6 channels each		

Table 1. MPC5675K family device comparison (continued)

Features		MPC5673K	MPC5674K	MPC5675K
Modules (cont.)	External Bus Interface (EBI)	1 module[5] 16-bit Data + Address or 32-bit Data with Address bus muxed[8]		
	Fast Ethernet Controller (FEC)	1 module		
	Fault Collection and Control Unit (FCCU)	1 module		
	FlexCAN	4 modules (32 message buffers each)		
	FlexPWM	3 modules (each 4 × 3 channels)		
	FlexRay	Optional		
	I^2C	2 modules[6]	3 modules	
	Interrupt Controller (INTC)	Yes (SoR)		
	LINFlex	3 modules[7]	4 modules	
	Parallel Data Interface (PDI)	1 module[8]		
	Periodic Interrupt Timer (PIT)	1 module, 4 channels		
	Software Watchdog Timer (SWT)	Yes (SoR)		
	System Timer Module (STM)	Yes (SoR)		
	Temperature sensor	1 module		
	Wakeup Unit (WKPU)	Yes		
	Crossbar switch (XBAR)	3 modules, 2 are user-configurable		
Clocking	Clock monitor unit (CMU)	3 modules		
	Frequency-modulated phase-locked loop (FMPLL)	2 modules (system and auxiliary)		
	IRCOSC – 16 MHz	1		
	XOSC 4–40 MHz	1		
Supply	Power management unit (PMU)	Yes		
	1.2 V low-voltage detector (LVD12)	1		
	1.2 V high-voltage detector (HVD12)	1		
	2.7 V low-voltage detector (LVD27)	4		
Debug	Nexus	Class 3+ (for cores and SRAM ports)		

Table 1. MPC5675K family device comparison (continued)

Features		MPC5673K	MPC5674K	MPC5675K
Packages	MAPBGA	257 pins 473 pins		
Temperature	Ambient	See the T_A recommended operating condition in the device data sheet		

1 Sphere of Replication.

2 Does not include Test or Shadow Flash memory space.

3 DSPI_0 and DSPI_1.

4 DSPI_0 has 8 chip selects; DSPI_1 and DSPI_2 have 4 chip selects each.

5 Available only on 473-pin package.

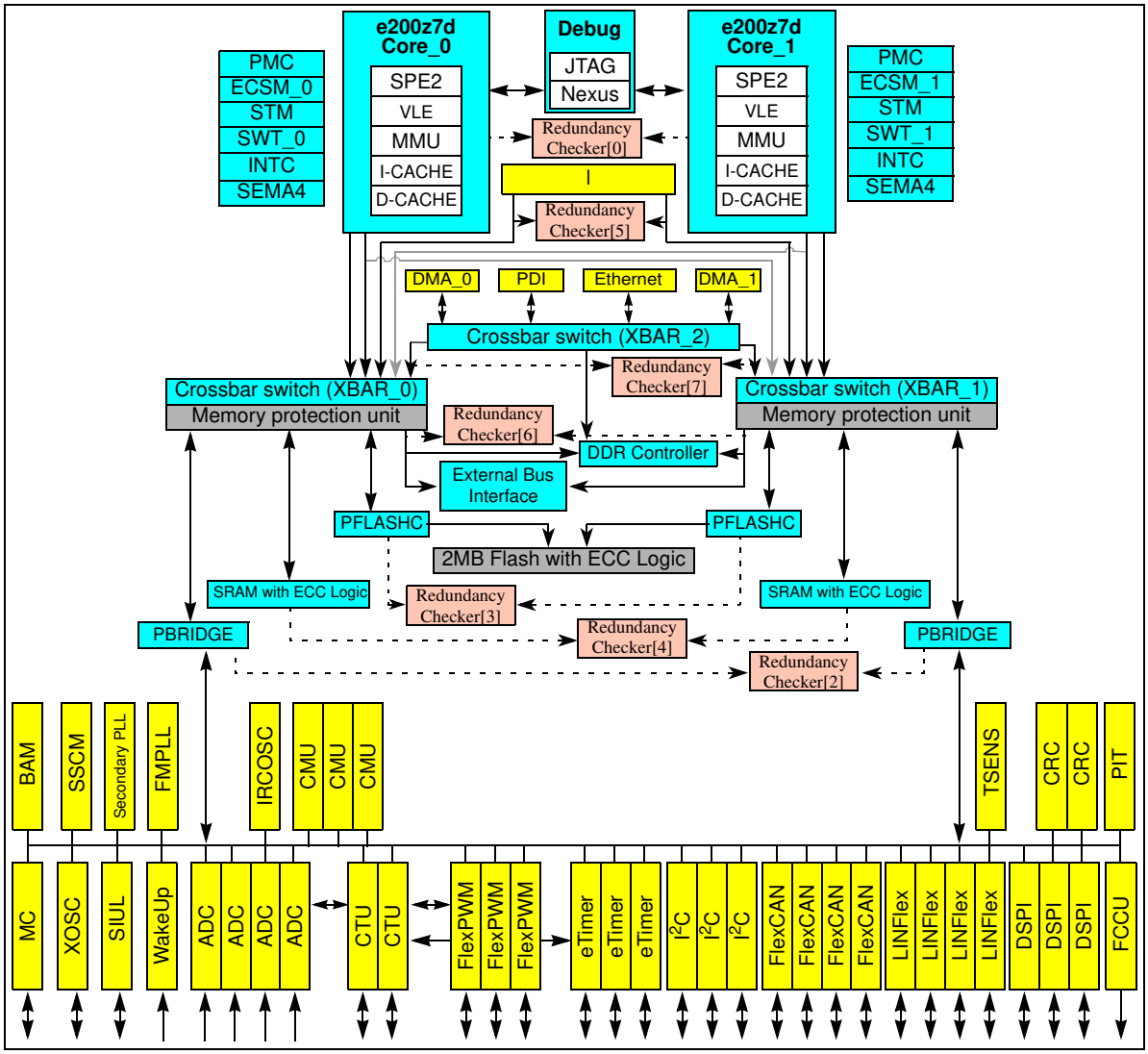
6 Any two of the three I2C can be chosen.

7 LinFlex_0, LinFlex_1, and LinFlex_2.

8 DDR available only on 473 package. Other modules available as follows:
EBI or DDR on 473 package
EBI + PDI on 473 package
DDR + PDI on 473 package
PDI only on 257 package

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5675K device.



ADC – Analog-to-digital converter
BAM – Boot assist module
CMU – Clock monitoring unit
CRC – Cyclic redundancy check unit
CTU – Cross triggering unit
DSPI – Deserial serial peripheral interface
EBI – External bus interface
ECC – Error correction code
ECSM – Error correction status module
eDMA – Enhanced direct memory access controller
FCCU – Fault collection and control unit
FEC – Fast Ethernet controller
FlexCAN – Controller area network controller
FlexPWM – Pulse width modulator module
FMPLL – Frequency-modulated phase-locked loop
I2C – Inter-integrated circuit controller
INTC – Interrupt controller
IRCOSC – Internal RC oscillator
JTAG – Joint Test Action Group interface
MC – Mode entry, clock, reset, and power modules
mDDR – Mobile double data rate dynamic RAM
PBRIDGE – Peripheral bridge
PDI – Parallel data interface
PIT – Periodic interrupt timer
PMC – Power management controller
RC – Redundancy checker
RTC – Real time clock
SEMA4 – Semaphore unit
SIUL – System integration unit Lite
SSCM – System status and configuration module
STM – System timer module
SWT – Software watchdog timer
TSENS – Temperature sensor
XOSC – Crystal oscillator

Figure 1. MPC5675K block diagram

1.5 Feature list

- High-performance e200z7d dual core
  - 32-bit Power Architecture® technology CPU
  - Up to 180 MHz core frequency
  - Dual-issue core
  - Variable length encoding (VLE)
  - Memory management unit (MMU) with 64 entries
  - 16 KB instruction cache and 16 KB data cache
- Memory available
  - Up to 2 MB code flash memory with ECC
  - 64 KB data flash memory with ECC
  - Up to 512 KB on-chip SRAM with ECC
- SIL3/ASILD innovative safety concept: LockStep mode and fail-safe protection
  - Sphere of replication (SoR) for key components
  - Redundancy checking units on outputs of the SoR connected to FCCU
  - Fault collection and control unit (FCCU)
  - Boot-time built-in self-test for memory (MBIST) and logic (LBIST) triggered by hardware
  - Boot-time built-in self-test for ADC and flash memory
  - Replicated safety-enhanced watchdog timer
  - Silicon substrate (die) temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) units
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority interrupt controller
- GPIOs individually programmable as input, output, or special function
- 3 general-purpose eTimer units (6 channels each)
- 3 FlexPWM units with four 16-bit channels per module
- Communications interfaces
  - 4 LINFlex modules
  - 3 DSPI modules with automatic chip select generation
  - 4 FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1) with dual channel, up to 128 message objects and up to 10 Mbit/s
  - Fast Ethernet Controller (FEC)
  - 3 I^2C modules
- Four 12-bit analog-to-digital converters (ADCs)
  - 22 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADC conversion with timer and PWM
- External bus interface
- 16-bit external DDR memory controller
- Parallel digital interface (PDI)

- On-chip CAN/UART bootstrap loader
- Capable of operating on a single 3.3 V voltage supply
  - 3.3 V-only modules: I/O, oscillators, flash memory
  - 3.3 V or 5 V modules: ADCs, supply to internal VREG
  - 1.8–3.3 V supply range: DRAM/PDI
- Operating junction temperature range –40 to 150 °C

1.6 Feature details

1.6.1 High-performance e200z7d core processor

- Dual 32-bit Power Architecture® processor core
- Loose or tight core coupling
- Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
- Thirty-two 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 64-entry fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 16 KB Instruction and 16 KB Data caches per core with line locking
  - Four way set associative
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports tag and data cache parity
  - Supports EDC for instruction cache
- Vectored interrupt support
- Signal processing engine 2 (SPE2) auxiliary processing unit (APU) operating on 64-bit general purpose registers
- Floating point
  - IEEE® 754 compatible with software wrapper
  - Single precision in hardware; double precision with software library
  - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions (except for guarded loads) do not increase interrupt latency in the MPC5675K
- To reduce latency, long cycle time instructions are aborted upon interrupt requests
- Extensive system development support through Nexus debug module

1.6.2 Crossbar Switch (XBAR)

- 32-bit address bus, 64-bit data bus
- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

1.6.3 Memory Protection Unit (MPU)

Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

1.6.4 Enhanced Direct Memory Access (eDMA) controller

- 32 channels support independent 8-, 16-, 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

1.6.5 Interrupt Controller (INTC)

- 208 peripheral interrupt requests
- 8 software settable sources
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

1.6.6 Frequency-Modulated Phase-Locked Loop (FMPLL)

Two FMPLLs are available on each device.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor and output clock divider ratio are software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 2 modes of operation
  - Normal PLL mode with crystal reference (default)
  - Normal PLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers as well as jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows running motor control periphery at different (precisely lower, equal, or higher, as required) frequency than the system to ensure higher resolution

1.6.7 External Bus Interface (EBI)

- Available on 473-pin devices
- Data and address options:
  - 16-bit data and address (non-muxed)
  - 32-bit data and address (bus-muxed)
- MPC5561 324 BGA compatibility mode: 16-bit data bus, 24-bit address bus is default ADDR[8:31], but configurable to 26-bit address bus
- Memory controller with support for various memory types
  - Non-burst and burst mode SDR flash and SRAM
  - Asynchronous/legacy flash and SRAM
- Configurable bus speed modes
- Support for 2 MB address space
- Chip select and write/byte enable options as presented in the pin-muxing table in the “Signal Description” chapter of the MPC5675K reference manual
- Configurable wait states (via chip selects)
- Optional automatic CLKOUT gating to save power and reduce EMI

1.6.8 On-chip flash memory

- Up to 2 MB code flash memory with ECC
- 64 KB data flash memory with ECC
- Censorship protection scheme to prevent flash content visibility
- Multiple block sizes to support features such as boot block, operating system block, and EEPROM emulation
- Read-while-write with multiple partitions
- Parallel programming mode to support rapid end-of-line programming
- Hardware programming state machine

1.6.9 Cache memory

- Harvard architecture cache
- 16 KB instruction / 16 KB data
- Four-way set-associative Harvard (instruction and data) 256-bit long cache
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports tag and data cache parity
  - Supports EDC for instruction cache

1.6.10 On-chip internal static RAM (SRAM)

- Up to 512 KB general-purpose SRAM
- ECC performs single-bit correction, double-bit error detection
  - Address included in ECC checkbase

1.6.11 DRAM controller

The DRAM controller (available only on 473-pin devices) is a multi-port controller that monitors incoming requests on the three AHB slave ports and decides (at each rising clock edge) what command needs to be sent to the external DRAM.

The DRAM controller on this device supports the following types of memories:

- Mobile DDR (mDDR)
- DDR 1
- DDR 2 (optional)
- SDR

The controller has the following features:

- Optimized timing for 32-byte bursts and single read accesses on the AHB interface
- Optimized timing for 8-byte and 16-byte bursts on the DRAMC interface
- Supports priority elevation on the slave ports for single accesses
- 16-bit wide DRAM interface
- One chip select (CS)
- mDDR memory controller
  - 16-bit external interface
  - Address range up to 8 MB

1.6.12 Boot Assist Module (BAM)

- Enables booting via serial mode (FlexCAN, LINFlex)
- Handles static mode in case of an erroneous boot procedure
- Implemented in 8 KB ROM
- Supports Lock Step Mode (LSM) and Decoupled Parallel Mode (DPM)

1.6.13 Parallel Data Interface (PDI)

- Support for external ADC and CMOS image sensors
- Parallel interface operation up to MCU system bus frequency
- Selectable data capture from rising or falling edge
- Receive FIFO with adjustable trigger thresholds
- Data width for 8, 10, 12, 14, and 16 bits
- Data Packing Unit to pack input data on 64-bit words — data packed on 8- or 16- bit boundary, depending on input data width
- Binary increasing channel select that allows as many as eight channels to be selected
- Frame synchronization through Vsync, Hsync, PIXCLK

1.6.14 Deserial Serial Peripheral Interface (DSPI) modules

- Three serial peripheral interfaces
  - Full duplex communication ports with interrupt and eDMA request support
  - Support for all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame basis

  - Modified SPI mode for interfacing to peripherals with longer setup time requirements
- Support for up to 60 Mbit/s in slave only Rx mode

1.6.15 Serial Communication Interface Module (LINFlex)

The LINFlex on this device features the following:

- Supports LIN Master mode, LIN Slave mode, and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and timeout errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (loop back, LIN bus stuck dominant detection)
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, or 16-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (parity, noise, and framing errors)
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods
- Support for DMA-enabled transfers

1.6.16 FlexCAN

- Thirty-two message buffers each
- Full implementation of the CAN protocol specification, Version 2.0B
- Programmable acceptance filters
- Individual Rx filtering per message buffer
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number
- Listen-only mode capabilities
- Programmable clock source: system clock or oscillator clock

- Reception queue possible by setting more than one Rx message buffer with the same ID
- Backwards compatible with previous FlexCAN modules
- Safety CAN features on 1 CAN module as implemented on MPC5604P

1.6.17 Dual-channel FlexRay controller

- Full implementation of FlexRay Protocol Specification 2.1
- Sixty-four configurable message buffers can be handled
- Message buffers configurable as Tx, Rx, or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count, and message ID
- Programmable acceptance filters for RxFIFO message buffers
- Dual channel, each at up to 10 Mbit/s data rate

1.6.18 Periodic Interrupt Timer (PIT)

The PIT module implements the features below:

- Four general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for real time interrupt, clocked from main external oscillator
- Can be used for software tick or DMA trigger operation

1.6.19 System Timer Module (STM)

The STM implements the features below:

- Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)
- Up-counter with four output compare registers
- OS task protection and hardware tick implementation as per current state-of-the-art AUTOSAR requirement

1.6.20 Motor control (MOTC) peripherals

The peripherals in this section can be used for general-purpose applications, but are specifically designed for motor control (MOTC) applications.

1.6.20.1 FlexPWM

The pulse width modulator module (FlexPWM) contains three PWM channels, each of which is configured to control a single half-bridge power stage. There may also be one or more fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency lower than or equal to platform frequency
- Clock source not modulated and independent from system clock (generated via auxiliary PLL)
- Fine granularity control for enhanced resolution of the PWM period

- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM is supported
- Double-buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for:
  - buffered output compare functions
  - input capture functions
- Enhanced dual-edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high and low limit registers
- Supports safety measures using DMA

1.6.20.2 Cross Triggering Unit (CTU)

The CTU provides automatic generation of ADC conversion requests on user-selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double-buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Maximum operating frequency lower than or equal to platform
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low-pass filter
- Double-buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double-buffered ADC command list pointers to minimize ADC trigger unit update
- Double-buffered ADC conversion command list with as many as twenty-four ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows controlling ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- Supports safety measures using DMA

1.6.20.3 Analog-To-Digital Converter (ADC)

- Four independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5 V or 0–3.3 V
- Twenty-two single-ended input channels
- Supports eight FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal, or external triggers
- DMA and interrupt request support

1.6.20.4 eTimer module

Three 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Ability to operate up to platform frequency
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality is not in use
- DMA support

1.6.21 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to enable high diagnostic coverage (check of checker)
- Replicated IP to be used as checkers on the PBRIDGE output, Flash Controller output, SRAM output, DMA Channel Mux inputs

1.6.22 Software Watchdog Timer (SWT)

This module implements the features below:

- Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)
- Fault-tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog

- Program flow control monitor with 16-bit pseudorandom key generation
- Provides measures to target high safety integrity levels (for example, SIL 3, ASIL D)

1.6.23 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, NMI, reset, or safe mode)
  - External reaction (failure is reported to the outside world via configurable output pins)

1.6.24 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pullup/pulldown
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.6.25 Cyclic Redundancy Checker (CRC) unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to an input register.

The CRC unit has the following features:

- Three sets of registers to allow three concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores the result in an internal register
- Implements the following standard CRC polynomials:
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to support implementation of safe communication protocol
- Offloads the core from cycle-consuming CRC and helps in checking the configuration signature for safe start-up or periodic procedures
- Connected as a peripheral on the internal peripheral bus
- Provides DMA support

1.6.26 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter is available to support high priority core exceptions.

1.6.27 System Status and Configuration Module (SSCM)

The SSCM on the MPC5675K features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid reset configuration halfword
- Sets up the MMU to allow user boot code to execute as either Classic Power Architecture Book E code (default) or as Freescale VLE code out of flash
- Supports serial bootloading of either Classic Power Architecture Book E code (default) or Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid

1.6.28 Nexus Development Interface (NDI)

- Per IEEE-ISTO 5001-2008
- Real-time development support for Power Architecture core through Nexus class 3 (some class 4 support)
- Nexus support to snoop system SRAM traffic
- Data trace of FlexRay accesses
- Read and write access
- Configured via the IEEE 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

1.6.29 IEEE 1149.1 JTAG Controller (JTAGC)

- IEEE 1149.1-2001 Test Access Port (TAP) interface
- JCOMP input that provides the ability to share the TAP —selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
- 5-bit instruction register that supports additional public instructions
- Three test data registers:
  - Bypass register
  - Boundary scan register
  - Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register, and associated circuitry

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the MPC5675K in the 257 MAPBGA package. Figure 3, Figure 4, Figure 5, and Figure 6 show the MPC5675K in the 473 MAPBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS_HV_IO	VSS_HV_IO	VDD_HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	VDD_HV_IO	fec RXD[2]	fec RX_CLK	fec RXD[0]	fec MDIO	fec TX_EN	fec TXD[3]	VSS_HV_IO	VSS_HV_IO	A
B	VSS_HV_IO	VSS_HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO [14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	VSS_HV_IO	fec RXD[3]	fec RX_ER	fec RXD[1]	fec TX_ER	fec TX_CLK	can0 TXD	VDD_HV_IO	VSS_HV_IO	B
C	VDD_HV_IO	nexus MDO [15]	VSS_HV_IO	FCCU_F[1]	flexray CB_RX	etimer0 ETC[0]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	JCOMP	fec CRS	fec TXD[0]	fec COL	can0 RXD	VSS_HV_PDI	pdi DATA [5]	pdi CLOCK	C
D	nexus MDO [2]	nexus MDO [3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[4]	VDD_HV_FLA	VSS_HV_FLA	fec TXD[2]	fec TXD[1]	fec RX_DV	fec MDC	VDD_HV_PDI	VSS_HV_IO	pdi DATA [0]	pdi DATA [1]	D
E	nexus MDO [0]	nexus MDO [1]	flexray CA_RX	NMI										pdi LINE_V	pdi DATA [2]	pdi DATA [3]	pdi DATA [4]	E
F	nexus MDO[6]	nexus MDO [11]	dspi1 SOUT	dspi1 SIN		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		mc_cgl clk_out	pdi DATA [6]	pdi DATA [7]	pdi DATA [8]	F
G	nexus MDO [4]	VDD_HV_IO	dspi0 SCK	dspi1 SCK		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [9]	pdi DATA [10]	pdi DATA [11]	pdi FRAME_V	G
H	nexus MDO [10]	VSS_HV_IO	dspi0 CS0	dspi1 CS0		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [12]	pdi DATA [13]	VDD_HV_PDI	flexpwm 0 X[0]	H
J	nexus MCKO	nexus MDO[8]	dspi2 CS0	dspi2 CS2		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [14]	pdi DATA [15]	VSS_HV_PDI	flexpwm 0 X[1]	J
K	nexus MSEO_B[0]	nexus MSEO_B[1]	nexus RDY_B	dspi0 SIN		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		flexpwm 0 X[2]	flexpwm 0 X[3]	flexpwm 0 A[1]	flexpwm 0 B[0]	K
L	nexus EVTO_B	nexus EVTI_B	dspi2 SCK	nexus MDO [13]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		VDD_HV_DRAM_VREF	TCK	flexpwm 0 B[1]	TDO	L
M	VDD_HV_OSC	VDD_HV_IO	dspi1 CS2	nexus MDO [12]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		flexpwm 0 B[2]	TDI	TMS	flexpwm 1 A[1]	M
N	XTALIN	VSS_HV_IO	dspi0 CS3	VSS_LV_PLL										flexpwm 0 B[3]	flexpwm 0 A[2]	flexpwm 1 A[0]	flexpwm 1 B[0]	N
P	VSS_HV_OSC	RESET	dspi0 CS2	VDD_LV_PLL	etimer1 ETC[1]	etimer1 ETC[2]	adc0 AN[0]	etimer1 ETC[3]	VSS_HV_IO	VDD_HV_IO	adc0_adc1 AN[14]	etimer1 ETC[4]	etimer1 ETC[5]	VDD_HV_IO	flexpwm 0 A[3]	flexpwm 0 A[0]	flexpwm 1 B[1]	P
R	XTAL OUT	FCCU_F[0]	VSS_HV_IO	dspi1 CS3	adc2 AN[0]	adc2 AN[3]	VDD_HV_ADR_13	adc2_adc3 AN[14]	VDD_HV_ADR_02	adc0 AN[2]	adc0_adc1 AN[13]	adc1 AN[1]	VREG_CTRL	lin0 TXD	VSS_HV_IO	flexpwm 1 A[2]	flexpwm 1 B[2]	R
T	VSS_HV_IO	VDD_HV_IO	dspi2 SOUT	adc3 AN[0]	adc3 AN[3]	adc2 AN[2]	VSS_HV_ADR_13	adc2_adc3 AN[13]	VSS_HV_ADR_02	adc0 AN[1]	adc0_adc1 AN[12]	adc1 AN[0]	adc1 AN[2]	lin0 RXD	etimer1 ETC[0]	VDD_HV_IO	VSS_HV_IO	T
U	VSS_HV_IO	VSS_HV_IO	dspi2 SIN	adc3 AN[1]	adc3 AN[2]	adc2 AN[1]	adc2_adc3 AN[11]	adc2_adc3 AN[12]	VDD_HV_ADV	VSS_HV_ADV	adc0_adc1 AN[11]	VREG_INT_ENABLE	RESET_SUP	VDD_HV_PMU	VSS_HV_PMU	VSS_HV_IO	VSS_HV_IO	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2. MPC5675K 257 MAPBGA pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS_ HV_IO	VSS_ HV_IO	VDD_ HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	fec RX_DV	fec MDIO	fec TX_CLK	fec TX_EN
B	VSS_ HV_IO	VSS_ HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO[14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	fec RXD[3]	fec RX_ER	fec TXD[0]	fec RXD[0]
C	VDD_ HV_IO	nexus MDO[15]	VSS_ HV_IO	FCCU_ F[1]	flexray CB_RX	etimer0 ETC[4]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	fec TXD[2]	fec TXD[1]	fec CRS
D	nexus MDO[1]	nexus MDO[3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[0]	VDD_ HV_IO	VSS_ HV_IO	JCOMP	VSS_ HV_IO	VSS_ HV_FLA
E	nexus MDO[0]	nexus MDO[2]	flexray CA_RX	NMI								
F	nexus MDO[10]	nexus MDO[11]	nexus MDO[6]	nexus MDO[4]		VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR
G	nexus MCKO	VDD_ HV_IO	nexus MDO[8]	nexus MSEO_B[1]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
H	nexus EVTO_B	VSS_ HV_IO	nexus MSEO_B[0]	nexus EVTI_B		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
J	nexus RDY_B	nexus MDO[13]	nexus MDO[12]	dspi1 SIN		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
K	dspi0 SCK	dspi1 CS0	dspi1 SCK	dspi1 SOUT		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
L	dspi0 CS0	dspi2 CS2	dspi2 CS0	VSS_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
M	flexpwm0 X[0]	VDD_ HV_IO	dspi0 SIN	VDD_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR

Figure 3. MPC5675K 473 MAPBGA pinout (northwest, viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12
N	flexpwm0 A[0]	VSS_ HV_IO	flexpwm0 X[1]	flexpwm0 B[2]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
P	flexpwm0 B[0]	flexpwm0 B[1]	flexpwm0 A[2]	flexpwm0 A[3]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
R	flexpwm0 X[2]	flexpwm0 X[3]	flexpwm0 A[1]	VSS_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
T	flexpwm0 B[3]	flexpwm1 A[0]	flexpwm1 A[1]	VDD_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
U	flexpwm1 B[0]	flexpwm1 B[1]	flexpwm1 A[2]	dspi2 SCK		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
V	VDD_ HV_OSC	VDD_ HV_IO	flexpwm1 B[2]	dspi1 CS2		VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR
W	XTALIN	VSS_ HV_IO	dspi0 CS3	VSS_ LV_PLL								
Y	VSS_ HV_OSC	$\overline{\text{RESET}}$	dspi0 CS2	VDD_ LV_PLL	flexpwm1 X[0]	adc3 AN[0]	adc2_adc3 AN[11]	adc2_adc3 AN[14]	etimer1 ETC[1]	etimer1 ETC[2]	etimer1 ETC[3]	VSS_ HV_IO
AA	XTALOUT	FCCU_ F[0]	VSS_ HV_IO	dspi1 CS3	flexpwm1 X[1]	adc3 AN[1]	adc2_adc3 AN[12]	adc2 AN[0]	VDD_ HV_ADV	VSS_ HV_ADV	adc0 AN[2]	adc0 AN[5]
AB	VSS_ HV_IO	VDD_ HV_IO	dspi2 SOUT	flexpwm1 X[2]	flexpwm1 X[3]	adc3 AN[2]	adc2_adc3 AN[13]	adc2 AN[1]	adc2 AN[2]	adc0 AN[0]	adc0 AN[4]	adc0 AN[6]
AC	VSS_ HV_IO	VSS_ HV_IO	dspi2 SIN	flexpwm1 A[3]	flexpwm1 B[3]	adc3 AN[3]	VDD_HV_ ADR_23	VSS_HV_ ADR_23	adc2 AN[3]	adc0 AN[1]	adc0 AN[3]	VDD_ HV_ADR_0

Figure 4. MPC5675K 473 MAPBGA pinout (southwest, viewed from above)

	13	14	15	16	17	18	19	20	21	22	23
A	fec TXD[3]	VDD_ HV_IO	pdi DATA[3]	pdi DATA[1]	pdi CLOCK	pdi DATA[7]	pdi DATA[10]	pdi DATA[13]	pdi DATA[15]	VSS_ HV_IO	VSS_ HV_IO
B	fec TX_ER	VSS_ HV_IO	pdi DATA[6]	pdi DATA[4]	pdi DATA[0]	pdi LINE_V	pdi DATA[9]	pdi DATA[14]	can0 TXD	VDD_ HV_IO	VSS_ HV_IO
C	fec RX_CLK	fec RXD[1]	fec COL	pdi DATA[5]	pdi DATA[2]	pdi DATA[8]	pdi DATA[12]	can0 RXD	VSS_ HV_PDI	siul GPIO[197]	dramc CAS
D	VDD_ HV_FLA	fec RXD[2]	fec MDC	VDD_ HV_PDI	VSS_ HV_PDI	pdi DATA[11]	pdi FRAME_V	VDD_ HV_PDI	dramc BA[1]	siul GPIO[195]	dramc BA[0]
E								mc_cgl clk_out	siul GPIO[149]	dramc CS0	dramc BA[2]
F	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR		dramc RAS	siul GPIO[194]	siul GPIO[148]	dramc D[5]
G	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		siul GPIO[196]	dramc DQS[0]	dramc DM[0]	dramc D[7]
H	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[2]	VDD_HV_ DRAM_VTT	VDD_HV_ DRAM	VSS_HV_ DRAM
J	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[0]	dramc D[1]	dramc D[3]	dramc D[6]
K	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VSS_ HV_IO	dramc D[4]	dramc D[8]	dramc D[9]
L	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VDD_ HV_IO	VDD_HV_ DRAM_VTT	VSS_HV_ DRAM	VDD_HV_ DRAM
M	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc ODT	dramc WEB	dramc D[11]	dramc D[10]

Figure 5. MPC5675K 473 MAPBGA pinout (northeast, viewed from above)

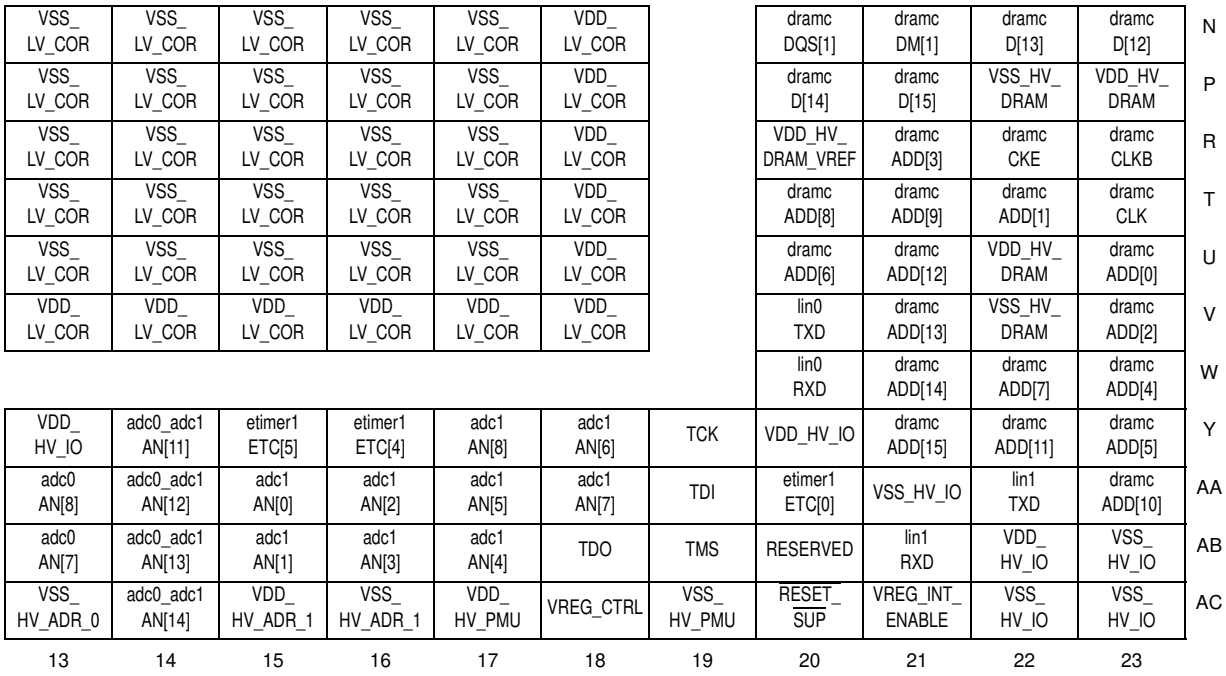


Figure 6. MPC5675K 473 MAPBGA pinout (southeast, viewed from above)

2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration for this device.

2.2.1 Pad types

Table 2 lists the pad types used on the MPC5675K.

Table 2. Pad types

Pad Type	Description
GP Slow	Slow buffer with CMOS Schmitt trigger and pullup/pulldown.
GP Slow/Fast	Programmable slow/fast buffer with CMOS Schmitt trigger, pullup/pulldown.
GP Slow/Medium	Programmable slow/medium buffer with CMOS Schmitt trigger, pullup/pulldown. Programmable slow/medium buffer with CMOS Schmitt trigger, pullup/pulldown and Injection proof analog switch.
GP Slow/Symmetric	Programmable slow/symmetric buffer with CMOS Schmitt trigger, pullup/pulldown.
PDI Medium	Medium slew-rate output with four selectable slew rates. Contains an input buffer and weak pullup/pulldown.
PDI Fast	Fast slew-rate output with four selectable slew rates. Contains an input buffer and weak pullup/pulldown.

Table 2. Pad types (continued)

Pad Type	Description
DRAM ACC	Bidirectional DDR pad. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM CLK	Differential clock driver.
DRAM DQ	Bidirectional DDR pad with integrated ODT. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM ODT CTL	Enable On Die Termination control.
Analog	CMOS Schmitt trigger cell with injection proof analog switch.
Analog Shared	CMOS Schmitt trigger cell with two injection-proof analog switches.

2.2.2 Power supply and reference voltage pins

Table 3 shows the supply pins for the MPC5675K in the 257 MAPBGA package. Table 5 shows the supply pins for the MPC5675K in the 473 MAPBGA package.

Table 4 and Table 6 show the pins not populated on the MPC5675K 257 MAPBGA and 473 MAPBGA packages, respectively.

Table 3. 257 MAPBGA supply pins

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F9	VDD_LV_COR	VDD_LV
A9	VDD_HV_IO	VDD_HV	F10	VDD_LV_COR	VDD_LV
B16	VDD_HV_IO	VDD_HV	F11	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F12	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	G12	VDD_LV_COR	VDD_LV
P10	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
P14	VDD_HV_IO	VDD_HV	H12	VDD_LV_COR	VDD_LV
T2	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T16	VDD_HV_IO	VDD_HV	J12	VDD_LV_COR	VDD_LV
L14	VDD_HV_DRAM_VREF	VDD_HV	K6	VDD_LV_COR	VDD_LV
D8	VDD_HV_FLA	VDD_HV	K12	VDD_LV_COR	VDD_LV
M1	VDD_HV_OSC	VDD_HV	L6	VDD_LV_COR	VDD_LV
D14	VDD_HV_PDI	VDD_HV	L12	VDD_LV_COR	VDD_LV
H16	VDD_HV_PDI	VDD_HV	M6	VDD_LV_COR	VDD_LV
U14	VDD_HV_PMU	VDD_HV	M7	VDD_LV_COR	VDD_LV
R7	VDD_HV_ADR_13	VDD_HV_A	M8	VDD_LV_COR	VDD_LV

Table 3. 257 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
R9	VDD_HV_ADR_02	VDD_HV_A	M9	VDD_LV_COR	VDD_LV
U9	VDD_HV_ADV	VDD_HV_A	M10	VDD_LV_COR	VDD_LV
F6	VDD_LV_COR	VDD_LV	M11	VDD_LV_COR	VDD_LV
F7	VDD_LV_COR	VDD_LV	M12	VDD_LV_COR	VDD_LV
F8	VDD_LV_COR	VDD_LV	P4	VDD_LV_PLL	VDD_LV
V_{SS}					
A1	VSS_HV_IO	VSS_HV	G7	VSS_LV_COR	VSS_LV
A2	VSS_HV_IO	VSS_HV	G8	VSS_LV_COR	VSS_LV
A16	VSS_HV_IO	VSS_HV	G9	VSS_LV_COR	VSS_LV
A17	VSS_HV_IO	VSS_HV	G10	VSS_LV_COR	VSS_LV
B1	VSS_HV_IO	VSS_HV	G11	VSS_LV_COR	VSS_LV
B2	VSS_HV_IO	VSS_HV	H7	VSS_LV_COR	VSS_LV
B9	VSS_HV_IO	VSS_HV	H8	VSS_LV_COR	VSS_LV
B17	VSS_HV_IO	VSS_HV	H9	VSS_LV_COR	VSS_LV
C3	VSS_HV_IO	VSS_HV	H10	VSS_LV_COR	VSS_LV
D15	VSS_HV_IO	VSS_HV	H11	VSS_LV_COR	VSS_LV
H2	VSS_HV_IO	VSS_HV	J7	VSS_LV_COR	VSS_LV
N2	VSS_HV_IO	VSS_HV	J8	VSS_LV_COR	VSS_LV
P9	VSS_HV_IO	VSS_HV	J9	VSS_LV_COR	VSS_LV
R3	VSS_HV_IO	VSS_HV	J10	VSS_LV_COR	VSS_LV
R15	VSS_HV_IO	VSS_HV	J11	VSS_LV_COR	VSS_LV
T1	VSS_HV_IO	VSS_HV	K7	VSS_LV_COR	VSS_LV
T17	VSS_HV_IO	VSS_HV	K8	VSS_LV_COR	VSS_LV
U1	VSS_HV_IO	VSS_HV	K9	VSS_LV_COR	VSS_LV
U2	VSS_HV_IO	VSS_HV	K10	VSS_LV_COR	VSS_LV
U16	VSS_HV_IO	VSS_HV	K11	VSS_LV_COR	VSS_LV
U17	VSS_HV_IO	VSS_HV	L7	VSS_LV_COR	VSS_LV
D9	VSS_HV_FLA	VSS_HV	L8	VSS_LV_COR	VSS_LV
P1	VSS_HV_OSC	VSS_HV	L9	VSS_LV_COR	VSS_LV
C15	VSS_HV_PDI	VSS_HV	L10	VSS_LV_COR	VSS_LV
J16	VSS_HV_PDI	VSS_HV	L11	VSS_LV_COR	VSS_LV
T9	VSS_HV_ADR_02	VSS_HV_A	N4	VSS_LV_PLL	VSS_LV
T7	VSS_HV_ADR_13	VSS_HV_A	U15	VSS_HV_PMU	VSS_LV
U10	VSS_HV_ADV	VSS_HV_A			

Table 4. 257 MAPBGA pins not populated on package

E5	E6	E7	E8	E9	E10	E11	E12
E13	F5	F13	G5	G13	H5	H13	J5
J13	K5	K13	L5	L13	M5	M13	N5
N6	N7	N8	N9	N10	N11	N12	N13

Table 5. 473 MAPBGA supply pins

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F15	VDD_LV_COR	VDD_LV
A14	VDD_HV_IO	VDD_HV	F16	VDD_LV_COR	VDD_LV
B22	VDD_HV_IO	VDD_HV	F17	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F18	VDD_LV_COR	VDD_LV
D8	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G18	VDD_LV_COR	VDD_LV
L20	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	H18	VDD_LV_COR	VDD_LV
M4	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T4	VDD_HV_IO	VDD_HV	J18	VDD_LV_COR	VDD_LV
V2	VDD_HV_IO	VDD_HV	K6	VDD_LV_COR	VDD_LV
Y13	VDD_HV_IO	VDD_HV	K18	VDD_LV_COR	VDD_LV
Y20	VDD_HV_IO	VDD_HV	L6	VDD_LV_COR	VDD_LV
AB2	VDD_HV_IO	VDD_HV	L18	VDD_LV_COR	VDD_LV
AB22	VDD_HV_IO	VDD_HV	M6	VDD_LV_COR	VDD_LV
AC12	VDD_HV_ADR_0	VDD_HV_A	M18	VDD_LV_COR	VDD_LV
AC15	VDD_HV_ADR_1	VDD_HV_A	N6	VDD_LV_COR	VDD_LV
AC7	VDD_HV_ADR_23	VDD_HV_A	N18	VDD_LV_COR	VDD_LV
AA9	VDD_HV_ADV	VDD_HV_A	P6	VDD_LV_COR	VDD_LV
H22	VDD_HV_DRAM	VDD_HV	P18	VDD_LV_COR	VDD_LV
L23	VDD_HV_DRAM	VDD_HV	R6	VDD_LV_COR	VDD_LV
P23	VDD_HV_DRAM	VDD_HV	R18	VDD_LV_COR	VDD_LV
U22	VDD_HV_DRAM	VDD_HV	T6	VDD_LV_COR	VDD_LV
R20	VDD_HV_DRAM_VREF	VDD_HV	T18	VDD_LV_COR	VDD_LV
H21	VDD_HV_DRAM_VTT	VDD_HV	U6	VDD_LV_COR	VDD_LV
L21	VDD_HV_DRAM_VTT	VDD_HV	U18	VDD_LV_COR	VDD_LV

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
D13	VDD_HV_FLA	VDD_HV	V6	VDD_LV_COR	VDD_LV
V1	VDD_HV_OSC	VDD_HV	V7	VDD_LV_COR	VDD_LV
D16	VDD_HV_PDI	VDD_HV	V8	VDD_LV_COR	VDD_LV
D20	VDD_HV_PDI	VDD_HV	V9	VDD_LV_COR	VDD_LV
AC17	VDD_HV_PMU	VDD_HV	V10	VDD_LV_COR	VDD_LV
F6	VDD_LV_COR	VDD_LV	V11	VDD_LV_COR	VDD_LV
F7	VDD_LV_COR	VDD_LV	V12	VDD_LV_COR	VDD_LV
F8	VDD_LV_COR	VDD_LV	V13	VDD_LV_COR	VDD_LV
F9	VDD_LV_COR	VDD_LV	V14	VDD_LV_COR	VDD_LV
F10	VDD_LV_COR	VDD_LV	V15	VDD_LV_COR	VDD_LV
F11	VDD_LV_COR	VDD_LV	V16	VDD_LV_COR	VDD_LV
F12	VDD_LV_COR	VDD_LV	V17	VDD_LV_COR	VDD_LV
F13	VDD_LV_COR	VDD_LV	V18	VDD_LV_COR	VDD_LV
F14	VDD_LV_COR	VDD_LV	Y4	VDD_LV_PLL	VDD_LV
V_{SS}					
A2	VSS_HV_IO	VSS_HV	L7	VSS_LV_COR	VSS_LV
A22	VSS_HV_IO	VSS_HV	L8	VSS_LV_COR	VSS_LV
A23	VSS_HV_IO	VSS_HV	L9	VSS_LV_COR	VSS_LV
B1	VSS_HV_IO	VSS_HV	L10	VSS_LV_COR	VSS_LV
B2	VSS_HV_IO	VSS_HV	L11	VSS_LV_COR	VSS_LV
B14	VSS_HV_IO	VSS_HV	L12	VSS_LV_COR	VSS_LV
B23	VSS_HV_IO	VSS_HV	L13	VSS_LV_COR	VSS_LV
C3	VSS_HV_IO	VSS_HV	L14	VSS_LV_COR	VSS_LV
D9	VSS_HV_IO	VSS_HV	L15	VSS_LV_COR	VSS_LV
D11	VSS_HV_IO	VSS_HV	L16	VSS_LV_COR	VSS_LV
H2	VSS_HV_IO	VSS_HV	L17	VSS_LV_COR	VSS_LV
K20	VSS_HV_IO	VSS_HV	M7	VSS_LV_COR	VSS_LV
L4	VSS_HV_IO	VSS_HV	M8	VSS_LV_COR	VSS_LV
N2	VSS_HV_IO	VSS_HV	M9	VSS_LV_COR	VSS_LV
A1	VSS_HV_IO	VSS_HV	M10	VSS_LV_COR	VSS_LV
R4	VSS_HV_IO	VSS_HV	M11	VSS_LV_COR	VSS_LV
W2	VSS_HV_IO	VSS_HV	M12	VSS_LV_COR	VSS_LV
Y12	VSS_HV_IO	VSS_HV	M13	VSS_LV_COR	VSS_LV
AA3	VSS_HV_IO	VSS_HV	M14	VSS_LV_COR	VSS_LV

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
AA21	VSS_HV_IO	VSS_HV	M15	VSS_LV_COR	VSS_LV
AB1	VSS_HV_IO	VSS_HV	M16	VSS_LV_COR	VSS_LV
AB23	VSS_HV_IO	VSS_HV	M17	VSS_LV_COR	VSS_LV
AC1	VSS_HV_IO	VSS_HV	N7	VSS_LV_COR	VSS_LV
AC2	VSS_HV_IO	VSS_HV	N8	VSS_LV_COR	VSS_LV
AC22	VSS_HV_IO	VSS_HV	N9	VSS_LV_COR	VSS_LV
AC23	VSS_HV_IO	VSS_HV	N10	VSS_LV_COR	VSS_LV
AC13	VSS_HV_ADR_0	VSS_HV_A	N11	VSS_LV_COR	VSS_LV
AC16	VSS_HV_ADR_1	VSS_HV_A	N12	VSS_LV_COR	VSS_LV
AC8	VSS_HV_ADR_23	VSS_HV_A	N13	VSS_LV_COR	VSS_LV
AA10	VSS_HV_ADV	VSS_HV_A	N14	VSS_LV_COR	VSS_LV
H23	VSS_HV_DRAM	VSS_HV	N15	VSS_LV_COR	VSS_LV
L22	VSS_HV_DRAM	VSS_HV	N16	VSS_LV_COR	VSS_LV
P22	VSS_HV_DRAM	VSS_HV	N17	VSS_LV_COR	VSS_LV
V22	VSS_HV_DRAM	VSS_HV	P7	VSS_LV_COR	VSS_LV
D12	VSS_HV_FLA	VSS_HV	P8	VSS_LV_COR	VSS_LV
Y1	VSS_HV_OSC	VSS_HV	P9	VSS_LV_COR	VSS_LV
C21	VSS_HV_PDI	VSS_HV	P10	VSS_LV_COR	VSS_LV
D17	VSS_HV_PDI	VSS_HV	P11	VSS_LV_COR	VSS_LV
G7	VSS_LV_COR	VSS_LV	P12	VSS_LV_COR	VSS_LV
G8	VSS_LV_COR	VSS_LV	P13	VSS_LV_COR	VSS_LV
G9	VSS_LV_COR	VSS_LV	P14	VSS_LV_COR	VSS_LV
G10	VSS_LV_COR	VSS_LV	P15	VSS_LV_COR	VSS_LV
G11	VSS_LV_COR	VSS_LV	P16	VSS_LV_COR	VSS_LV
G12	VSS_LV_COR	VSS_LV	P17	VSS_LV_COR	VSS_LV
G13	VSS_LV_COR	VSS_LV	R7	VSS_LV_COR	VSS_LV
G14	VSS_LV_COR	VSS_LV	R8	VSS_LV_COR	VSS_LV
G15	VSS_LV_COR	VSS_LV	R9	VSS_LV_COR	VSS_LV
G16	VSS_LV_COR	VSS_LV	R10	VSS_LV_COR	VSS_LV
G17	VSS_LV_COR	VSS_LV	R11	VSS_LV_COR	VSS_LV
H7	VSS_LV_COR	VSS_LV	R12	VSS_LV_COR	VSS_LV
H8	VSS_LV_COR	VSS_LV	R13	VSS_LV_COR	VSS_LV
H9	VSS_LV_COR	VSS_LV	R14	VSS_LV_COR	VSS_LV
H10	VSS_LV_COR	VSS_LV	R15	VSS_LV_COR	VSS_LV