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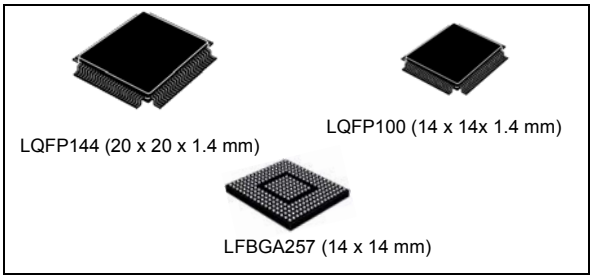
SPC56EL60x, SPC56EL54x, SPC564L60x, SPC564L54x

32-bit Power Architecture® microcontroller for automotive SIL3/ASILD chassis and safety applications

Datasheet - production data



Features

- High-performance e200z4d dual core
- 32-bit Power Architecture® technology CPU
- Core frequency as high as 120 MHz
- Dual issue five-stage pipeline core
- Variable Length Encoding (VLE)
- Memory Management Unit (MMU)
- 4 KB instruction cache with error detection code
- Signal processing engine (SPE)
- Memory available
  - 1 MB flash memory with ECC
  - 128 KB on-chip SRAM with ECC
  - Built-in RWW capabilities for EEPROM emulation
- SIL3/ASILD innovative safety concept: LockStep mode and Fail-safe protection
  - Sphere of replication (SoR) for key components (such as CPU core, eDMA, crossbar switch)
  - Fault collection and control unit (FCCU)
  - Redundancy control and checker unit (RCCU) on outputs of the SoR connected to FCCU
  - Boot-time Built-In Self-Test for Memory (MBIST) and Logic (LBIST) triggered by hardware
  - Boot-time Built-In Self-Test for ADC and flash memory triggered by software
  - Replicated junction temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) unit
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority controller
  - Replicated 16-channel eDMA controller
- GPIOs individually programmable as input, output or special function
- Three 6-channel general-purpose eTimer units
- 2 FlexPWM units
  - Four 16-bit channels per module
- Communications interfaces
  - 2 LINFlexD channels
  - 3 DSPI channels with automatic chip select generation
  - 2 FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1 Rev. A) with 2 channels, 64 message buffers and data rates up to 10 Mbit/s
- Two 12-bit analog-to-digital converters (ADCs)
  - 16 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADCs conversion with timer and PWM
- Sine wave generator (D/A with low pass filter)
- On-chip CAN/UART bootstrap loader
- Single 3.0 V to 3.6 V voltage supply
- Ambient temperature range –40 °C to 125 °C
- Junction temperature range –40 °C to 150 °C

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56ELx/SPC564Lx series of microcontroller units (MCUs). For functional characteristics, see the *SPC56ELx/SPC564Lx Microcontroller Reference Manual*. For use of the SPC56ELx/SPC564Lx in a fail-safe system according to safety standard ISO26262, see the *Safety Application Guide for SPCEL60.*

1.2 Description

The SPC56ELx/SPC564Lx series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The SPC56ELx/SPC564Lx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the SPC56ELx/SPC564Lx automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

1.3 Device comparison

Table 1. SPC56ELx/SPC564Lx device summary

Feature		SPC56EL60	SPC56EL54
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)	
	Architecture	Harvard	
	Execution speed	0–120 MHz (+2% FM)	
	DMIPS intrinsic performance	>240 MIPS	
	SIMD (DSP + FPU)	Yes	
	MMU	16 entry	
	Instruction set PPC	Yes	
	Instruction set VLE	Yes	
	Instruction cache	4 KB, EDC	
	MPU-16 regions	Yes, replicated module	
	Semaphore unit (SEMA4)	Yes	
Buses	Core bus	AHB, 32-bit address, 64-bit data	
	Internal periphery bus	32-bit address, 32-bit data	
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3	
Memory	Flash	1 MB, ECC, RWW	768 KB, ECC, RWW
	Static RAM (SRAM)	128 KB, ECC	96 KB, ECC

Table 1. SPC56ELx/SPC564Lx device summary (continued)

Feature		SPC56EL60	SPC56EL54
Modules	Interrupt Controller (INTC)	16 interrupt levels, replicated module	
	Periodic Interrupt Timer (PIT)	1 × 4 channels	
	System Timer Module (STM)	1 × 4 channels, replicated module	
	Software Watchdog Timer (SWT)	Yes, replicated module	
	eDMA	16 channels, replicated module	
	FlexRay	1 × 64 message buffers, dual channel	
	FlexCAN	2 × 32 message buffers	
	LINFlexD (UART and LIN with DMA support)	2	
	Clock out	Yes	
	Fault Collection and Control Unit (FCCU)	Yes	
	Cross Triggering Unit (CTU)	Yes	
	eTimer	3 × 6 channels(1)	
	FlexPWM	2 Module 4 × (2 + 1) channels(2)	
	Analog-to-Digital Converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)	
	Sine Wave Generator (SWG)	32 point	
Modules (cont.)	Deserial Serial Peripheral Interface (DSPI)	3 × DSPI as many as 8 chip selects	
	Cyclic Redundancy Checker (CRC) unit	Yes	
	Junction temperature sensor (TSENS)	Yes, replicated module	
	Digital I/Os	≥ 16	
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die	
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V	
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4 – 40 MHz	
Debug	Nexus	Level 3+	
Packages	LQFP	100 pins 144 pins	
	LBGA(3)	LBGA257	

Table 1. SPC56ELx/SPC564Lx device summary (continued)

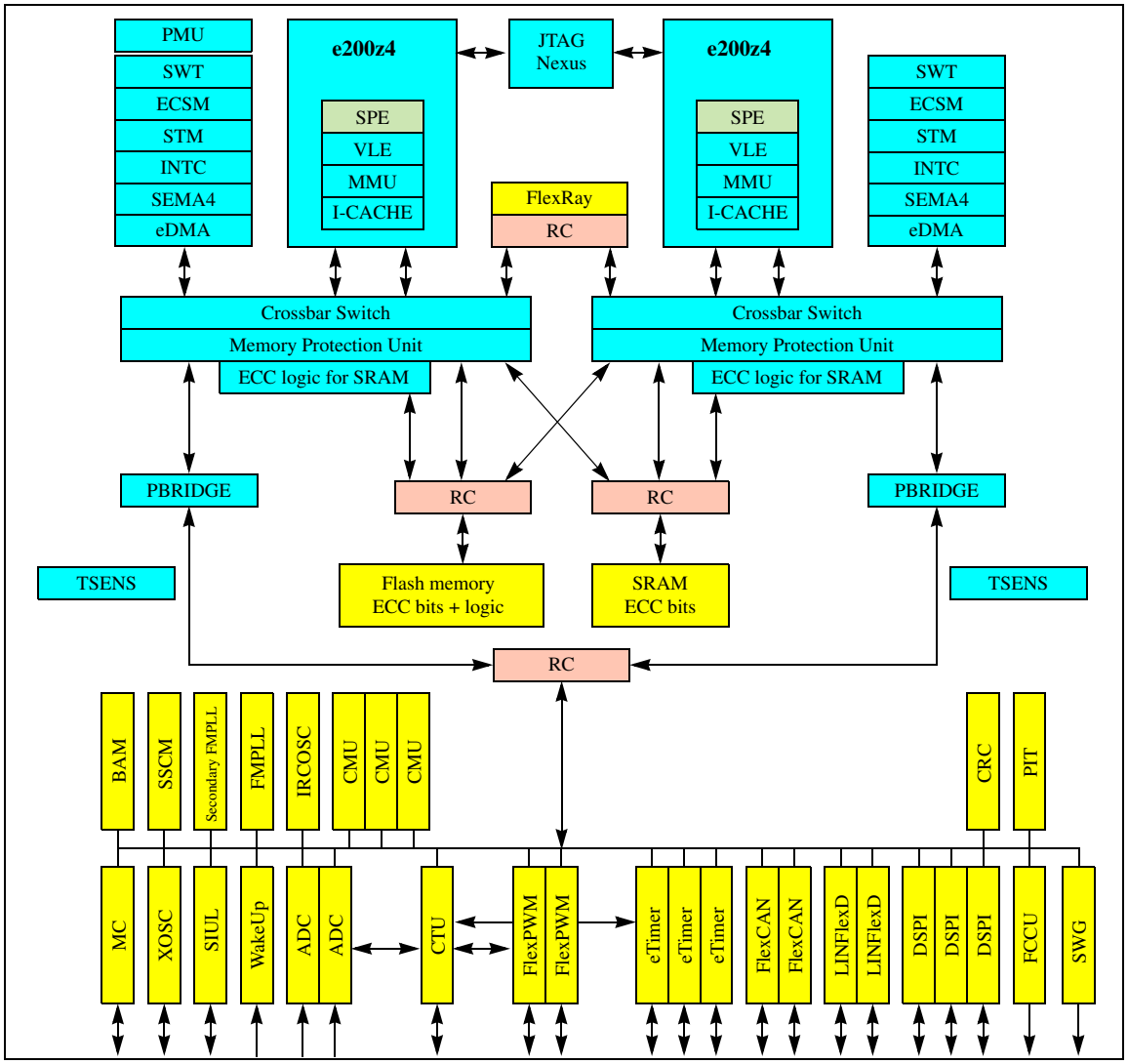
Feature		SPC56EL60	SPC56EL54
Temperature	Temperature range (junction)	–40 to 150 °C	
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C	

1. The third eTimer (eTimer_2) is available with external I/O access only in the BGA package, on the LQFP package eTimer_2 is available internally only without any external I/O access.
2. The second FlexPWM module is available only in the BGA package.
3. LBGA257 available only as development package.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56ELx/SPC564Lx device.

Figure 1. SPC56ELx/SPC564Lx block diagram



ADC – Analog-to-Digital Converter
BAM – Boot Assist Module
CMU – Clock Monitoring Unit
CRC – Cyclic Redundancy Check unit
CTU – Cross Triggering Unit
DSPI – Serial Peripherals Interface
ECC – Error Correction Code
ECSM – Error Correction Status Module
eDMA – Enhanced Direct Memory Access controller
FCCU – Fault Collection and Control Unit
FlexCAN – Controller Area Network controller
FMPLL – Frequency Modulated Phase Locked Loop
INTC – Interrupt Controller
IRCOSC – Internal RC Oscillator
JTAG – Joint Test Action Group interface
LINFlexD – LIN controller with DMA support
MC – Mode Entry, Clock, Reset, & Power
PBRIDGE – Peripheral bridge
PIT – Periodic Interrupt Timer
PMU – Power Management Unit
RC – Redundancy Checker
RTC – Real Time Clock
SEMA4 – Semaphore Unit
SIUL – System Integration Unit Lite
SSCM – System Status and Configuration Module
STM – System Timer Module
SWG – Sine Wave Generator
SWT – Software Watchdog Timer
TSENS – Temperature Sensor
XOSC – Crystal Oscillator

- High-performance e200z4d dual core
  - 32-bit Power Architecture® technology CPU
  - Core frequency as high as 120 MHz
  - Dual issue five-stage pipeline core
  - Variable Length Encoding (VLE)
  - Memory Management Unit (MMU)
  - 4 KB instruction cache with error detection code
  - Signal processing engine (SPE)
- Memory available
  - 1 MB flash memory with ECC
  - 128 KB on-chip SRAM with ECC
  - Built-in RWW capabilities for EEPROM emulation
- SIL3/ASILD innovative safety concept: LockStep mode and Fail-safe protection
  - Sphere of replication (SoR) for key components (such as CPU core, eDMA, crossbar switch)
  - Fault collection and control unit (FCCU)
  - Redundancy control and checker unit (RCCU) on outputs of the SoR connected to FCCU
  - Boot-time Built-In Self-Test for Memory (MBIST) and Logic (LBIST) triggered by hardware
  - Boot-time Built-In Self-Test for ADC and flash memory triggered by software
  - Replicated safety enhanced watchdog
  - Replicated junction temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) unit
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority controller
  - Replicated 16-channel eDMA controller
- GPIOs individually programmable as input, output or special function
- Three 6-channel general-purpose eTimer units
- 2 FlexPWM units
  - Four 16-bit channels per module
- Communications interfaces
  - 2 LINFlexD channels
  - 3 DSPI channels with automatic chip select generation
  - 2 FlexCAN interfaces (2.0B Active) with 32 message objects

  - FlexRay module (V2.1 Rev. A) with 2 channels, 64 message buffers and data rates up to 10 Mbit/s
- Two 12-bit analog-to-digital converters (ADCs)
  - 16 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADCs conversion with timer and PWM
- Sine wave generator (D/A with low pass filter)
- On-chip CAN/UART bootstrap loader
- Single 3.0 V to 3.6 V voltage supply
- Ambient temperature range –40 °C to 125 °C
- Junction temperature range –40 °C to 150 °C

1.5 Feature details

1.5.1 High-performance e200z4d core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs

- Extensive system development and tracing support via Nexus debug port

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processing channel.

1.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processing channel.

1.5.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow block for test, censorship device and user option bits
- Wait states:
  - 3 wait states for frequencies =< 120 MHz
  - 2 wait states for frequencies =< 80 MHz
  - 1 wait state for frequencies =< 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The SPC56ELx/SPC564Lx SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 128 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - 1 wait state for frequencies =< 120 MHz
  - 0 wait states for frequencies =< 80 MHz

1.5.7 Platform flash memory controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.
- Single-cycle read responses (0 AHB data-phase wait states) for hits in the buffers. The buffers implement a least-recently-used replacement algorithm to maximize performance.
- Programmable response for read-while-write sequences including support for stall-while-write, optional stall notification interrupt, optional flash operation abort, and optional abort notification interrupt.
- Separate and independent configurable access timing (on a per bank basis) to support use across a wide range of platforms and frequencies.
- Support of address-based read access timing for emulation of other memory types.
- Support for reporting of single- and multi-bit error events.
- Typical operating configuration loaded into programming model by system reset.

The platform flash controller is replicated for each processor.

1.5.8 Platform Static RAM Controller (SRAMC)

The SRAMC module is the platform SRAM array controller, with integrated error detection and correction.

The main features of the SRAMC provide connectivity for the following interfaces:

- XBAR Slave Port (64-bit data path)
- ECSM (ECC Error Reporting, error injection and configuration)
- SRAM array

The following functions are implemented:

- ECC encoding (32-bit boundary for data and complete address bus)
- ECC decoding (32-bit boundary and entire address)
- Address translation from the AHB protocol on the XBAR to the SRAM array

The platform SRAM controller is replicated for each processor.

1.5.9 Memory subsystem access time

Every memory access, that the CPU performs, requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed is not parked on the requesting master in the crossbar.

Table 2 shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. Platform memory access time summary

AHB transfer	Data phase wait states	Description
e200z4d instruction fetch	0	Flash memory prefetch buffer hit (page hit)
e200z4d instruction fetch	3	Flash memory prefetch buffer miss (based on 4-cycle random flash array access time)
e200z4d data read	0–1	SRAM read
e200z4d data write	0	SRAM 32-bit write
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

1.5.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for SRAM

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

1.5.13 System clocks and clock generation

The following list summarizes the system clock and clock generation on this device:

- Lock status continuously monitored by lock detect circuitry
- Loss-of-clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and fewer external components required)
- Programmable output clock divider of system clock (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and as many as three eTimer modules running on an auxiliary clock independent from system clock (with max frequency 120 MHz)
- On-chip crystal oscillator with automatic level control
- Dedicated internal 16 MHz internal RC oscillator for rapid start-up
  - Supports automated frequency trimming by hardware during device startup and by user application
- Auxiliary clock domain for motor control periphery (FlexPWM, eTimer, CTU, ADC, and SWG)

1.5.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Each device has two FMPLLs.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Output divider (ODF) for reduced frequency operation without re-lock
- 3 modes of operation
  - Bypass mode
  - Normal FMPLL mode with crystal reference (default)
  - Normal FMPLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

1.5.15 Main oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

1.5.16 Internal Reference Clock (RC) oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the FMPLL
- RC oscillator is used as the default system clock during startup and can be used as back-up input source of FMPLL(s) in case XOSC fails

1.5.17 Clock, reset, power, mode and test control modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)

These modules provide the following:

- Clock gating and clock distribution control
- Halt, stop mode control
- Flexible configurable system and auxiliary clock dividers
- Various execution modes
  - HALT and STOP mode as reduced activity low power mode
  - Reset, Idle, Test, Safe
  - Various RUN modes with software selectable powered modules
  - No stand-by mode implemented (no internal switchable power domains)

1.5.18 Periodic Interrupt Timer Module (PIT)

The PIT module implements the following features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Can be used for software tick or DMA trigger operation

1.5.19 System Timer Module (STM)

The STM implements the following features:

- Up-counter with 4 output compare registers
- OS task protection and hardware tick implementation per AUTOSAR[(a)] requirement

The STM is replicated for each processor.

1.5.20 Software Watchdog Timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

a. Automotive Open System Architecture.

The SWT module is replicated for each processor.

1.5.21 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ, Functional Reset, Destructive Reset, or Safe mode entered)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.5.22 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.5.23 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

1.5.24 Boot Assist Module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System Status and Configuration Module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification

- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO
- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction