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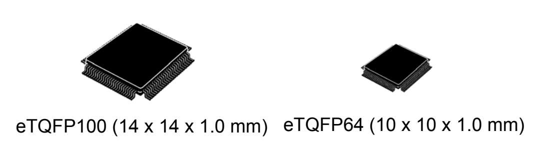
SPC570S40E1, SPC570S40E3, SPC570S50E1, SPC570S50E3

32-bit Power Architecture® microcontroller for automotive ASILD applications

Datasheet - production data



Features

- High performance e200z0h dual core
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 80 MHz
  - Single issue 4-stage pipeline in-order execution core
  - Variable Length Encoding (VLE)
- Up to 544 KB (512 KB code + 32 KB data, suitable for EEPROM emulation) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- Up to 48 KB on-chip general-purpose SRAM
- Multi-channel direct memory access controller (eDMA paired in lockstep) with 16 channels
- Comprehensive new generation ASILD safety concept
  - Safety of bus masters (core+INTC, DMA) by delayed lockstep approach
  - Safety of storage (Flash, SRAM) by mainly ECC
  - Safety of the data path to storage and periphery by mainly End-to-End EDC (E2E EDC)
  - Clock and power, generation and distribution, supervised by dedicated monitors
  - Fault Collection and Control Unit (FCCU) for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Boot time MBIST and LBIST for latent faults
  - Check of safety mechanisms availability and error reaction path functionality by dedicated mechanisms
  - Safety of the periphery by application-level measures supported by replicated peripheral bridges and by LBIST
  - Further measures on dedicated peripherals (e.g. ADC supervisor)
  - Junction temperature sensor
  - 8-region system memory protection unit (SMPU) with process ID support (tasks isolation)
  - Enhanced SW watchdog
  - Cyclic redundancy check (CRC) unit
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus Class 3 debug and trace interface
- Communication interfaces
  - 2 LINFlexD modules
  - 3 deserial serial peripheral interface (DSPI) modules
  - Up to 2 FlexCAN interfaces with 32 message buffers each
- On-chip CAN/UART Bootstrap loader with Boot Assisted Flash (BAF). Physical Interface (PHY) can be
  - UART
  - CAN
- 2 enhanced 12-bit SAR analog converters
  - 1.5 µs conversion time (12 MHz)
  - 16 physical channels (fully shared between the 2 SARADC units)
  - Supervisor ADC concept
  - Programmable Cross Triggering Unit (CTU)
- Single 3.3 V or 5 V voltage supply
- 4 general purpose eTimer units (6 channels each)
- Junction temperature range -40 °C to 150 °C

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The SPC570Sx is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC570Sx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of Chassis and Safety electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 80 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. SPC570Sx device feature summary (Family Superset Configuration)

Feature		Description
Process		55 nm
Main processor	Core	e200z0h
	Number of main cores	1
	Number of checker cores	1
	VLE	Yes
	Main processor frequency	80 MHz(1)
Interrupt controllers (including interrupt controller checker)		1
Software watchdog timer		1
System timers		1 AUTOSAR® STM 1 PIT with four 32-bit channels
DMA (including DMA checker)		1
DMA channels		16
SMPU		Yes (8 regions)(2)
System SRAM		48 KB
Code flash memory		512 KB
Data flash memory (suitable for EEPROM emulation)		32 KB

Table 1. SPC570Sx device feature summary (Family Superset Configuration)

Feature		Description
UTEST flash memory		8 KB
Boot assist flash (BAF)		8 KB
CRC		1
LINFlexD		2
FlexCAN		2
DSPI		3
eTimer		4 x 6 channels
ADC (SAR)		2(3)
CTU (Cross Triggering Unit)		1
Temperature sensor		1
Self-test control unit (memory and logic BIST)		1
FCCU		1
MEMU		1
PLL		Dual PLL with FM
Nexus		3(4)
Sequence processing unit (SPU)		1
External power supplies		5 V(5) 3.3 V(5)
Junction temperature		–40 to 150 °C
Packages	Device SPC570SxxE3	eTQFP100
	Device SPC570SxxE1	eTQFP64

1. Includes user programmable CPU core and one safety core. The two e200z0h processors in the lockstep pair run at 80 MHz. The e200z0h is compatible with the Power Architecture embedded specification.
2. SMPU with process ID support extension
3. One ADC can be used as supervisor ADC
4. Including trace for the crossbar masters (data & instruction trace on core and data trace on eDMA). 4 MDO pin Nexus trace port
5. All I/Os can be supplied at 3.3 V or 5 V (mutually exclusive)

Table 2. SPC570S40Ex, SPC570S50Ex device configuration differences

	SPC570S40 **(full option configuration)**	**SPC570S50** **(full option configuration)**
Flash	256 KB(1)	512 KB
RAM	32 KB(2)	48 KB
CAN	1(3)	2
Others	aligned to the *SPC570Sx device feature summary (Family Superset Configuration)* described in *Table 1*	

1. Flash blocks excluded on SPC570S40:
   128K Block 0 [0x0100_0000 … 0x0101_FFFF]
   128K Block 1 [0x0102_0000 … 0x0103_FFFF]
2. SRAM area excluded on SPC570S40
   [0x4000_8000…0x4000_BFFF]
3. FlexCAN1 excluded on SPC570S40

1.3 Feature overview

On-chip modules within the SPC570Sx include the following features:

- 2 main CPUs, single-issue, 32-bit CPU core complexes (e200z0h), running in lockstep
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
- Up to 544 KB (512 KB code + 32 KB data, suitable for EEPROM emulation) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- Up to 48 KB on-chip general-purpose SRAM
- Multi-channel direct memory access controller (eDMA paired in lockstep)
  - 16 channels per eDMA
- Interrupt controller (INTC) with dedicated interrupt source channels, including software interrupts and 32 priority levels
- Dual phase-locked loops with stable clock domain for peripherals and frequency modulation domain for computational shell
- Crossbar switch architecture for concurrent access to peripherals, flash memory, or SRAM from multiple bus masters with end-to-end ECC
- System integration unit lite (SIUL2)
- Boot Assist Flash (BAF) supports factory programming using serial bootload through ‘UART Serial Boot Mode Protocol’. Physical Interface (PHY) can be
  - UART / LIN
  - CAN
- Enhanced analog-to-digital converter system
  - 2 separate 12-bit SAR analog converters
  - 1.5 µs conversion time (at 12 MHz)
  - 16 physical channels
- Temperature sensor
  - Range –40 to +150 °C
  - Sensitivity approximately 5.14 mV/°C
- STCU2
  - Support for Logic BIST and Memory BIST at power on
  - ASIL D
- 3 deserial serial peripheral interface (DSPI) modules
- 2 LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 (master/slave)
  - LINFlexD_1 (master)
- Up to 2 FlexCAN modules
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with partial support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller manages the supply voltage down to 1.2 V for core logic

2 Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. Block diagram

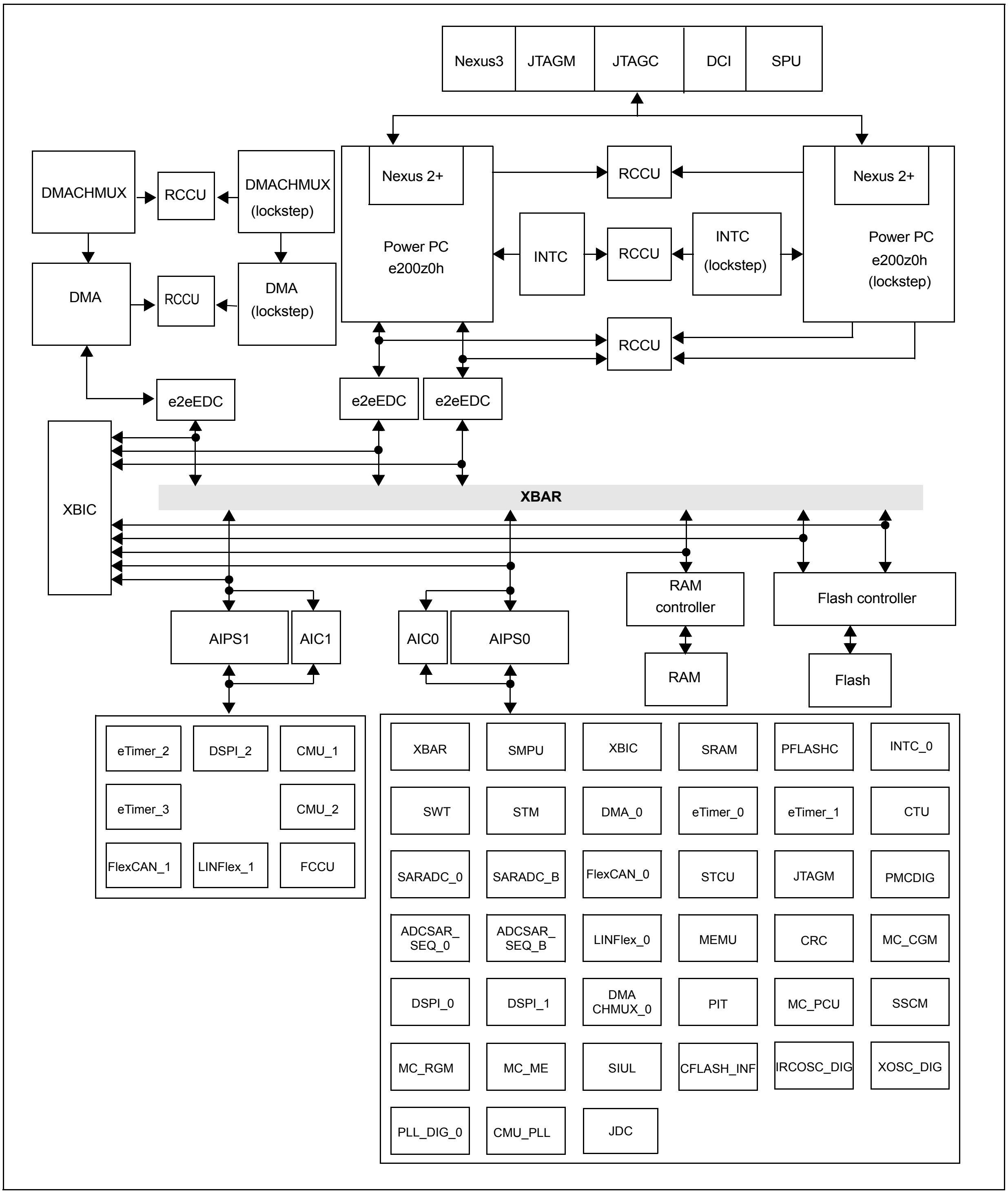


Table 3 summarizes the functions of all blocks present in the SPC570Sx series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Table 3. SPC570Sx series block summary

Block	Function
e200z0 CPU	Allows single clock instruction execution
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to-digital converter
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via 16 programmable channels.
DMACHMUX	Allows to route a defined number of DMA peripheral sources to the DMA channels
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
PLL0	Output independent of core clock frequency
Frequency-modulated phase-locked loop (PLL1)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
AIPS	System bus to peripheral bus interface
RAM controller	Acts as an interface between the system bus and the integrated system RAM
System RAM	Supports read/write accesses mapped to the SRAM memory from any master
Flash memory controller	Acts as an interface between the system bus and the Flash memory module
Flash memory	Up to 512 KB of programmable, non-volatile Flash memory for code and 32 KB for data
IRCOSC	Controls the internal 16 MHz RC oscillator system
XOSC	Controls the on-chip oscillator (XOSC) and provides the register interface for the programmable features
JTAG Master	Provides software the option to write data for driving JTAG
JTAG Data Communication Module	Provides the capability to move register data between the IPS and JTAG domains
PASS	Programs a set of Flash memory access protections, based on user programmable passwords
Sequence Processing Unit	Provides an on-device trigger functions similar to those found on a logic analyzer
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load

Table 3. SPC570Sx series block summary (continued)

Block	Function
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
MC_PMC	Contains registers that enable/disable the various voltage monitors
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
eTimer	Has six 16-bit general purpose counter, where each counter can be used as input capture or output compare function
FCCU	Collects fault event notification from the rest of the system and translates them into internal and/or external system reactions
RCCU	Compares input signals and issues an alarm in the case of a mismatch
MEMU	Collects and reports error events associated with ECC (Error Correction Code) logic used on SRAM, DMA RAM and Flash memory
XBIC	Verifies the integrity of the attribute information for crossbar transfers and signals the Fault Collection and Control Unit (FCCU) when an error is detected
STCU2	Handles the BIST procedure
CRC	Controls the computation of CRC, off-loading this work from the CPU
RegProt	Protects several registers against accidental writing, locking their value till the next reset phase
Temperature sensor	Monitors the device temperature
Debug Control Interface	Provides debug features for the MCU
Nexus Port Controller	Monitor a variety of signals including addresses, data, control signals, status signals, etc.
Nexus Multimaster Trace Client	Monitors the system bus and provides real-time trace information to debug or development tools
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
System integration unit (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code

Table 3. SPC570Sx series block summary (continued)

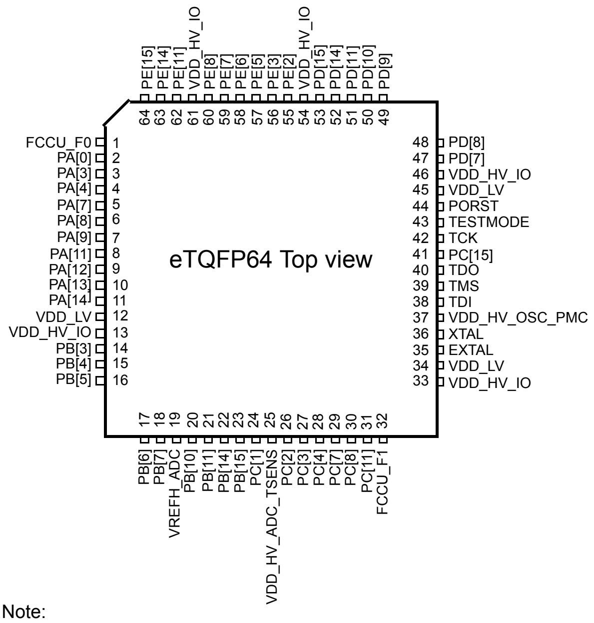
Block	Function
Wakeup unit (WKPU)	The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available eTQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to the device reference manual.

Figure 2. eTQFP 64-pin configuration[a]



Note:

Availability of port pin alternate functions depends on product selection.

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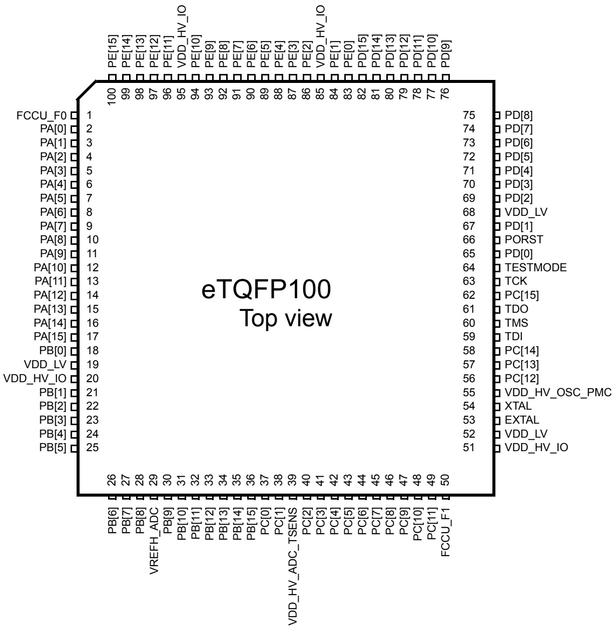
a. All eTQFP64 information is indicative and must be confirmed during silicon validation.

Figure 3. eTQFP 100-pin configuration



Note:

Availability of port pin alternate functions depends on product selection.

3.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC570Sx devices.

For information on the signal descriptions and related information about the functionality and configuration of the SPC570Sx devices, refer to the "Signal description" chapter in the devices' reference manual.

3.3 Package pads/pins

Table 4 shows the eTQFP64 and eTQFP100 pinouts. The default reset state for all the pins associated with a programmable alternate function is GPIO.

Note: Nexus pins can be enabled via JTAG during the reset phase

Table 4. eTQFP64 and eTQFP100 pinout

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
—	FCCU_F0	1	1	IO	FCCU_F0(1)			
PA[0]	PAD[0]	2	2	IO	DSPI 0 - CS 0	Ext. INT 0	DSPI 1 - CS 1	Timer 0 - ch. 0
PA[1]	PAD[1]	—	3	IO	DSPI 1 - CS 1	Timer 0 - ch. 0	Nexus EVTI	Timer 1 - ch. 0
PA[2]	PAD[2]	—	4	IO	DSPI 2 - CS 1	DSPI 0 - CS 4	Nexus EVTO	Timer 1 - ch. 1
PA[3]	PAD[3]	3	5	IO	DSPI 0 - CLK	Ext. INT 1	Timer 0 - ch. 0	DSPI 1 - CLK
PA[4]	PAD[4]	4	6	IO	DSPI 0 - Serial Data	NMI	Timer 0 - ch. 1	DSPI 1 - Serial Data
PA[5]	PAD[5]	—	7	IO	LINFlex 1 - TX	Timer 0 - ch. 1	Nexus MCK 0	Timer 1 - ch. 2
PA[6]	PAD[6]	—	8	IO	LINFlex 1 - RX	Timer 0 - ch. 2	Nexus MDO 0	Timer 1 - ch. 3
PA[7]	PAD[7]	5	9	IO	DSPI 0 - Serial Data	—	Timer 0 - ch. 2	DSPI 1 - Serial Data
PA[8]	PAD[8]	6	10	IO	DSPI 0 - CS 1	DSPI 2 - CS 0	LINFlex 1 - TX	Timer 0 - ch. 1
PA[9]	PAD[9]	7	11	IO	DSPI 0 - CS 2	DSPI 0 - CS 7	LINFlex 1 - RX	Timer 0 - ch. 2
PA[10]	PAD[10]	—	12	IO	—	DSPI 1 - CS 1	Nexus MDO 1	Ext. INT 3

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PA[11]	PAD[11]	8	13	IO	DSPI 0 - CS 3	DSPI 0 - CS 5	Timer 0 - ch. 3	Ext. INT 4
PA[12]	PAD[12]	9	14	IO	LINFlex 0 - RX	FlexCAN 1 - RX	LINFlex 1 - RX	Timer 0 - ch. 3
PA[13]	PAD[13]	10	15	IO	LINFlex 0 - TX	FlexCAN 1 - TX	LINFlex 1 - TX	Timer 0 - ch. 4
PA[14]	PAD[14]	11	16	IO	Timer 0 - ch. 4	DSPI 1 - CS 1	Ext. INT 3	Timer 0 - ch. 5
PA[15]	PAD[15]	—	17	IO	FlexCAN 1 - RX	Timer 1 - ch. 0	Nexus MDO 2	Timer 1 - ch. 4
PB[0]	PAD[16]	—	18	IO	FlexCAN 1 - TX	Timer 1 - ch. 1	Nexus MDO 3	Timer 1 - ch. 5
—	VDD_LV	12	19	PW	—			
—	VDD_HV_IO	13	20	PWB20	—			
PB[1]	PAD[17]	—	21	IO	Timer 1 - ch. 5	DSPI 0 - CS 6	Nexus MSEO 0	DSPI 1 - CS 0
PB[2]	PAD[18]	—	22	IN/ANA	Timer 0 - ch. 4	ADC ch. 15	Ext. INT 3	FlexCAN 0 - RX
PB[3]	PAD[19]	14	23	IN/ANA	Timer 0 - ch. 0	ADC ch. 9	Timer 1 - ch. 0	DSPI 0 - Serial Data
PB[4]	PAD[20]	15	24	IN/ANA	Timer 0 - ch. 1	ADC ch. 8	Timer 1 - ch. 1	DSPI 1 - Serial Data
PB[5]	PAD[21]	16	25	IN/ANA	Timer 0 - ch. 2	ADC ch. 7	Timer 1 - ch. 2	DSPI 2 - Serial Data
PB[6]	PAD[22]	17	26	IN/ANA	Timer 0 - ch. 3	ADC ch. 6	Timer 1 - ch. 3	—
PB[7]	PAD[23]	18	27	IN/ANA	Ext. INT 0	ADC ch. 5	Timer 0 - ch. 4	Timer 1 - ch. 4
PB[8]	PAD[24]	—	28	IN/ANA	Timer 0 - ch. 5	ADC ch.14	Ext. INT 4	FlexCAN 1 - RX
—	VREFH_ADC	19	29	REF	—			
PB[9]	PAD[25]	—	30	IN/ANA	Timer 2 - ch. 3	ADC ch. 13	Ext. INT 5	LINFlex 0 - RX
PB[10]	PAD[26]	20	31	IN/ANA	Ext. INT 1	ADC ch. 4	Timer 0 - ch. 5	Timer 1 - ch. 5
PB[11]	PAD[27]	21	32	IN/ANA	Ext. INT 2	ADC ch. 3	Timer 1 - ch. 4	Timer 0 - ch. 4

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PB[12]	PAD[28]	—	33	IN/ANA	Timer 2 - ch. 4	ADC ch. 12	Timer 1 - ch. 5	LINFlex 1 - RX
PB[13]	PAD[29]	—	34	IN/ANA	Timer 2 - ch. 5	ADC ch. 11	Timer 3 - ch. 0	NMI
PB[14]	PAD[30]	22	35	IN/ANA	Timer 2 - ch. 0	ADC ch. 2	Timer 3 - ch. 1	Timer 2 - ch. 1
PB[15]	PAD[31]	23	36	IN/ANA	Timer 2 - ch. 1	ADC ch. 1	Timer 3 - ch. 2	Timer 2 - ch. 2
PC[0]	PAD[32]	—	37	IN/ANA	Timer 1 - ch. 0	ADC ch. 10	Timer 3 - ch. 3	Ext. INT 0
PC[1]	PAD[33]	24	38	IN/ANA	Timer 2 - ch. 2	ADC ch. 0	Timer 3 - ch. 4	Timer 2 - ch. 4
—	VDD_HV_ADC_TSENS	25	39	PW	—			
PC[2]	PAD[34]	26	40	IO	Timer 0 - ch. 5	DSPI 2 - CS 1	FlexCAN 1 - RX	FlexCAN 0 - RX
PC[3]	PAD[35]	27	41	IO	Timer 1 - ch. 0	DSPI 2 - CS 2	FlexCAN 1 - TX	FlexCAN 0 - TX
PC[4]	PAD[36]	28	42	IO	Timer 1 - ch. 1	DSPI 1 - CS 0	Ext. INT 1	FlexCAN 1 - RX
PC[5]	PAD[37]	—	43	IO	DSPI 1 - CS 0	Timer 1 - ch. 2	Nexus RDY	FlexCAN 1 - TX
PC[6]	PAD[38]	—	44	IO	DSPI 1 - Serial Data	Timer 1 - ch. 3	DSPI 2 - CS 4	DSPI 0 - Serial Data
PC[7]	PAD[39]	29	45	IO	Timer 1 - ch. 2	DSPI 1 - Serial Data	DSPI 2 - CS 5	DSPI 0 - CS 0
PC[8]	PAD[40]	30	46	IO	Timer 1 - ch. 3	DSPI 1 - Serial Data	DSPI 2 - CS 6	DSPI 0 - CS 1
PC[9]	PAD[41]	—	47	IO	DSPI 1 - Serial Data	Timer 1 - ch. 4	DSPI 2 - CS 7	DSPI 0 - Serial Data
PC[10]	PAD[42]	—	48	IO	DSPI 1 - CLK	Timer 1 - ch. 5	—	DSPI 0 - CLK
PC[11]	PAD[43]	31	49	IO	Timer 1 - ch. 4	DSPI 1 - CLK	—	DSPI 0 - CS 2
—	FCCU_F1	32	50	IO	FCCU_F1			
—	VDD_HV_IO	33	51	PWB51	—			
—	VDD_LV	34	52	PW	—			
—	EXTAL	35	53	ANA	—			

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
—	XTAL	36	54	ANA	—			
—	VDD_HV_OSC_PMC	37	55	PW	—			
PC[12]	PAD[44]	—	56	IO	Timer 0 - ch. 0	DSPI 1 - CS 3	—	LINFlex 0 - RX
PC[13]	PAD[45]	—	57	IO	Timer 0 - ch. 1	DSPI 1 - CS 4	—	LINFlex 0 - TX
PC[14]	PAD[46]	—	58	IO	Timer 0 - ch. 2	DSPI 1 - CS 5	—	DSPI 0 - CS 3
—	TDI	38	59	IO	—			
—	TMS	39	60	IO	—			
—	TDO	40	61	IO	—			
PC[15]	PAD[47]	41	62	IO	NMI	DSPI 1 - CS 2	Ext. INT 4	Timer 2 - ch. 0
—	TCK	42	63	IO	—			
—	TESTMODE	43	64	IO	—			
PD[0]	PAD[48]	—	65	IO	DSPI 1 - CS 6	Ext. INT 0	—	Timer 2 - ch. 1
—	PORST	44	66	IO	—			
PD[1]	PAD[49]	—	67	IO	Timer 0 - ch. 3	DSPI 1 - CS 7	—	DSPI 0 - CS 4
—	VDD_LV	45	68	PW	—			
PD[2]	PAD[50]	—	69	IO	Timer 2 - ch. 0	DSPI 2 - CS 1	DSPI 1 - CS 6	Timer 3 - ch. 0
PD[3]	PAD[51]	—	70	IO	Timer 2 - ch. 1	DSPI 2 - CS 2	DSPI 1 - CS 4	Timer 3 - ch. 1
PD[4]	PAD[52]	—	71	IO	Timer 2 - ch. 2	DSPI 2 - CS 3	DSPI 1 - CS 7	Timer 3 - ch. 2
—	VDD_HV_IO	46	—	PWB51	—			
PD[5]	PAD[53]	—	72	IO	DSPI 2 - CS 0	Timer 2 - ch. 1	DSPI 1 - CS 6	Timer 3 - ch. 3
PD[6]	PAD[54]	—	73	IO	DSPI 2 - Serial Data	Timer 2 - ch. 2	DSPI 1 - CS 5	DSPI 0 - CS 5
PD[7]	PAD[55]	47	74	IO	Timer 3 - ch. 0	CTU trg_inp	DSPI 1 - CS 2	LINFlex 1 - RX
PD[8]	PAD[56]	48	75	IO	Timer 3 - ch. 1	CTU trg_outp	DSPI 1 - CS 6	LINFlex 1 - TX

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PD[9]	PAD[57]	49	76	IO	FlexCAN 0 - RX	DSPI 2 - CS 1	FlexCAN 1 - RX	Timer 2 - ch. 2
PD[10]	PAD[58]	50	77	IO	FlexCAN 0 - TX	—	FlexCAN 1 - TX	Timer 2 - ch. 3
PD[11]	PAD[59]	51	78	IO	Timer 3 - ch. 2	DSPI 2 - CLK	DSPI 1 - CS 7	—
PD[12]	PAD[60]	—	79	IO	DSPI 2 - Serial Data	Timer 2 - ch. 3	DSPI 2 - CS 2	—
PD[13]	PAD[61]	—	80	IO	DSPI 2 - CLK	Timer 2 - ch. 4	DSPI 2 - CS 3	—
PD[14]	PAD[62]	52	81	IO	Timer 2 - ch. 3	DSPI 2 - Serial Data	Timer 3 - ch. 3	—
PD[15]	PAD[63]	53	82	IO	Timer 2 - ch. 4	DSPI 2 - Serial Data	Timer 3 - ch. 4	—
PE[0]	PAD[64]	—	83	IO	Timer 3 - ch. 3	Ext. INT 2	—	Timer 2 - ch. 4
PE[1]	PAD[65]	—	84	IO	Timer 3 - ch. 4	—	—	Timer 2 - ch. 5
—	VDD_HV_IO	54	85	PWB85	—			
PE[2]	PAD[66]	55	86	IO	Timer 2 - ch. 5	DSPI 2 - CS 0	DSPI 0 - CS 3	—
PE[3]	PAD[67]	56	87	IO	Nexus MSEO(2)	—	DSPI 0 - CS 4	DSPI 2 - CLK
PE[4]	PAD[68]	—	88	IO	Timer 3 - ch. 5	DSPI 2 - CS 2	Timer 2 - ch. 4	—
PE[5]	PAD[69]	57	89	IO	Nexus MDO 3(2)	—	CLOCKOUT	DSPI 2 - Serial Data
PE[6]	PAD[70]	58	90	IO	Nexus MDO 2(2)	—	DSPI 0 - CS 6	DSPI 2 - Serial Data
PE[7]	PAD[71]	59	91	IO	Nexus MDO 1(2)	—	DSPI 0 - CS 7	Timer 3 - ch. 4
PE[8]	PAD[72]	60	92	IO	Nexus MDO 0(2)	DSPI 0 - CS 0	Ext. INT 3	Timer 3 - ch. 5
PE[9]	PAD[73]	—	93	IO	—	Timer 3 - ch. 2	Ext. INT 4	DSPI 2 - CS 1
PE[10]	PAD[74]	—	94	IO	—	Timer 3 - ch. 3	DSPI 0 - CS 5	DSPI 2 - CS 2
—	VDD_HV_IO	61	95	PW	—			

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PE[11]	PAD[75]	62	96	IO	Nexus MCK0[2]	DSPI 0 - CLK	DSPI 0 - CS 1	DSPI 1 - CS 3
PE[12]	PAD[76]	—	97	IO	—	Timer 3 - ch. 4	DSPI 2 - CS 0	DSPI 1 - CS 2
PE[13]	PAD[77]	—	98	IO	—	Timer 3 - ch. 5	DSPI 2 - CS 1	DSPI 1 - CS 1
PE[14]	PAD[78]	63	99	IO	Nexus EVTO [2]	DSPI 0 - Serial Data	DSPI 0 - CS 2	DSPI 2 - CS 3
PE[15]	PAD[79]	64	100	IO	Nexus EVTI[2]	DSPI 0 - Serial Data	DSPI 1 - CS 3	—

1. Cannot be changed
2. Can be enabled via JTAG during the reset phase

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 5* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 5. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 Absolute maximum ratings

Table 6. Absolute maximum ratings (1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	T	Lifetime power cycles	—	—	1000k	—
V_{SS}	C	Ground voltage	—	—	—	—
V_{DD_LV}	C	1.2 V core supply voltage	—	-0.3	1.5	V
$V_{DD\_HV\_IO}$	C	I/O supply voltage(2)	—	-0.3	6.0	V
$V_{DD\_HV\_OSC\_PMC}$	C	Power management unit and OSC power supply	—	-0.3	6.0	V
$V_{DD\_HV\_ADC\_TSENS}$	C	ADC & TSENS power supply	—	-0.3	6.0	V
V_{REFH_ADC}	C	ADC reference supply	—	0	$V_{DD\_HV\_ADC\_TSENS}$	V
V_{IN}	C	I/O input voltage range(3)	—	-0.3	6.0	V
			Relative to V_{SS}	-0.3	—	
			Relative to $V_{DD\_HV\_IO}$	—	0.3	
I_{INJD}	T	Maximum DC injection current for digital pad during overload condition	Per pin, applies to all digital pins	-3	3	mA
I_{INJA}	T	Maximum DC injection current for analog pad during overload condition	Per pin, applies to all analog pins	-3	3	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	-7	8	mA
			Strong	-10	10	
			Very strong	-11	11	
I_{MAXSEG}	SR	Maximum current per power segment(4)	—	-90	90	mA
T_{STG}	SR	Storage temperature range and non-operating times	—	-55	175	°C
STORAGE	SR	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range -40 °C to 85 °C	—	20	years
T_{SDR}	SR	Maximum solder temperature(5) Pb-free package	—	—	260	°C
MSL	SR	Moisture sensitivity level(6)	—	—	3	—
t_{XRAY}	SR	X-ray screen time	At 80÷130 KV; 20÷50 µA; max 1 Gy dose	—	200	ms

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device. During overload conditions ($V_{IN} > V_{DD\_HV\_IO}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

2. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C remaining time at or below 5.5 V.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
4. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
5. Solder profile per IPC/JEDEC J-STD-020D
6. Moisture sensitivity per JEDEC test method A112

4.4 Electromagnetic compatibility (EMC)

Table 7 describes the EMC characteristics of the device.

Table 7. Radiated emissions testing specification(1),(2)

Coupling structure	Test setup	Function	Functional configuration	BISS radiated emissions limit
Entire IC	(G) TEM	Reference test	C1-S3	18 dBµV
		Reference test with SSCG	C1-S3	18 dBµV
		Memory copy	C4-S2	18 dBµV
		Memory copy with SSCG	C4-S2	18 dBµV

1. Reference “BISS Generic IC EMC Test Specification”, version 1.2, section 9.3, “Emission test configuration for ICs with CPU”.
2. The EMC parameters are classified as "T", validated on testbench.

4.5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 8. ESD ratings(1),(2)

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(3)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(4)	T	All pins	500	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”
3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

4.6 Operating conditions

Table 9. Device operating conditions[(1)]

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Frequency								
f_{SYS}	SR		Device operating frequency[(2)]	-40 °C < T_J < 150 °C	—	—	80	MHz
Temperature								
T_J	SR	P	Operating temperature range - junction	—	-40.0	—	150.0	°C
T_A (T_L to T_H)	SR	P	Ambient operating temperature range	—	-40.0	—	125.0	°C
Voltage								
$V_{DD\_HV\_IO}$	SR	P	I/O supply voltage	LVD290/HVD400 enabled	2.97	—	3.63	V
		C		LVD290 enabled HVD400 disabled[(3),(4)]	2.97	—	5.5	
$V_{DD\_HV\_OSC\_PMC}$	SR	P	PMC and OSC supply voltage	LVD290/HVD400 enabled	2.97	—	3.63	V
		C		LVD290 enabled HVD400 disabled	2.97	—	5.5	
$V_{DD\_HV\_ADC\_TSENS}$	SR	D	SAR ADC supply voltage	LVD400 enabled	4.5	—	5.5	V
		C		LVD400 disabled[(3),(5)]	3.0	—	3.6	
V_{REFH_ADC}	SR	P	SAR ADC reference voltage	—	2.0	—	$V_{DD\_HV\_ADC\_TSENS}$	V
V_{REFH_ADC} - $V_{DD\_HV\_ADC\_TSENS}$	SR	D	SAR ADC reference differential voltage	—	—	—	25	mV
V_{RAMP}	SR	D	Slew rate on power supply pins	—	—	—	0.5	V/µs
V_{IN}	SR	C	I/O input voltage range	—	0	—	5.5	V
Injection current								
I_{IC}	SR	T	DC injection current (per pin)[(6),(7),(8)]	Digital pins and analog pins	-3	—	3	mA
I_{MAXSEG}	SR	D	Maximum current per power segment[(9)]	—	-80	—	80	mA