Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

**NXP Semiconductors**
Data Sheet: Technical Data

Document Number MPC5744P
Rev. 6.1, 11/2017

# MPC5744P

# MPC5744P Data Sheet

## 32-bit MCU suitable for ISO26262 ASIL-D chassis and safety applications

### Features

- The MPC5744P microcontroller is based on the Power Architecture® developed by NXP. It targets chassis and safety applications and other applications requiring a high Automotive Safety Integrity Level (ASIL). The MPC5744P is a SafeAssure solution.
- This document provides electrical specifications, pin assignments, and package diagram information for the MPC5744P series of microcontroller units (MCUs). For functional characteristics and the programming model, see the MPC5744P Reference Manual.
- Junction temperature: The upper limit is 150°C or 165°C depending on the device marking.

# Table of Contents

# 1 Introduction

## 1.1 Features

The following table summarizes the features of the MPC5744P.

**Table 1. MPC5744P feature summary**

| Feature | Details |
|---|---|
| **CPU** | |
| Power Architecture | 2 x e200z4 in delayed lock step |
| Architecture | Harvard |
| Execution speed | 0 MHz to 200 MHz (+2% FM) |
| Embedded FPU | Yes |
| Core MPU | 24 regions |
| Instruction Set PPC | No |
| Instruction Set VLE | Yes |
| Instruction cache | 8 KB, EDC |
| Data cache | 4 KB, EDC |
| Data local memory | 64 KB, ECC |
| System MPU | Yes (16 regions) |
| **Buses** | |
| Core bus | AHB, 32-bit address, 64-bit data, e2e ECC |
| Internal periphery bus | 32-bit address, 32-bit data |
| **Crossbar** | |
| Master x slave ports | 4 x 5 |
| **Memory**—see Table 2 for additional details | |
| Code/data flash memory | **2.5 MB**, ECC, RWW |
| Data flash memory | Supported with RWW |
| SRAM | **384 KB**, ECC |
| Overlay access to SRAM from Flash Memory Controller | Yes |
| **Modules** | |
| Interrupt controller | 32 interrupt priority levels, 16 SW programmable interrupts |
| PIT | 1 module with 4 channels |
| System Timer Module (STM) | 1 module with 4 channels |
| Software Watchdog Timer (SWT) | Yes |
| eDMA | 32 channels, in delayed lock step |
| FlexRay | 1 module with 64 message buffer, dual channel |
| FlexCAN | 3 modules with 64 message buffer |
| LINFlexD (UART and LIN with DMA support) | 2 modules |

*Table continues on the next page...*

## Table 1. MPC5744P feature summary (continued)

| Feature | Details |
|---|---|
| Clockout | Yes |
| Fault Control and Collection Unit (FCCU) | Yes |
| Cross Triggering Unit (CTU) | 2 modules |
| eTimer | 3 modules with 6 channels |
| FlexPWM | 2 modules with 4 x (2+1) channels |
| Analog-to-digital converter (ADC) | 4 modules with 12-bit ADC, each with 16 channels (25 external channels including shared channels plus internal channels) |
| Sine-wave generator (SGEN) | 32 point |
| SPI | 4 modules<br>As many as 8 chip selects |
| CRC Unit | Yes |
| SENT | 2 modules with 2 channels |
| Interprocessor serial link interface (SIPI) | Yes |
| Junction temperature sensor | Yes (replicated module) |
| Digital I/Os | ≥ 16 |
| Peripheral register protection | Yes |
| Ethernet | Yes |
| Error Injection Module (EIM) | Yes |
| **Supply** | |
| Device Power Supply | 3.3 V with external ballast transistor<br>3.3 V with external 1.25 V low drop-out (LDO) regulator |
| ADC Analog Reference voltage | 3.15 V to 5.5 V |
| **Clocking** | |
| Phase Lock Loop (PLL) | 1 x PLL and 1 coupled FMPLL |
| Internal RC Oscillator | 16 MHz |
| External Crystal Oscillator | 8 MHz to 40 MHz |
| **Low power modes** | |
| HALT and STOP | Yes |
| **Debug** | |
| Nexus | Level 3+, MDO and Aurora interface |
| **Package** | |
| LQFP | 144 pins, 0.5 mm pitch, 20 mm x 20 mm outline |
| MAPBGA | 257 MAPBGA, 0.8 mm pitch, 14 mm x 14 mm outline |
| **Temperature** | |
| Temperature range (junction) | -40°C to +150°C, option for 165°C |
| Ambient temperature range (LQFP) | -40°C to +125°C, 135°C option (with 165°C junction option) |
| Ambient temperature range (BGA) | -40°C to +125°C, 135°C option (with 165°C junction option) |

**Table 2. Flash memory and SRAM sizes of MPC5744P, MPC5743P, MPC5742P, and MPC5741P**

| Part number | Flash memory | SRAM |
|---|---|---|
| MPC5744P | 2.5 MB | 384 KB |
| MPC5743P | 2.0 MB | 256 KB |
| MPC5742P | 1.5 MB | 192 KB |
| MPC5741P | 1.0 MB | 128 KB |

## 1.2 Block Diagram

The following figure is a top-level diagram that shows the functional organization of the system.

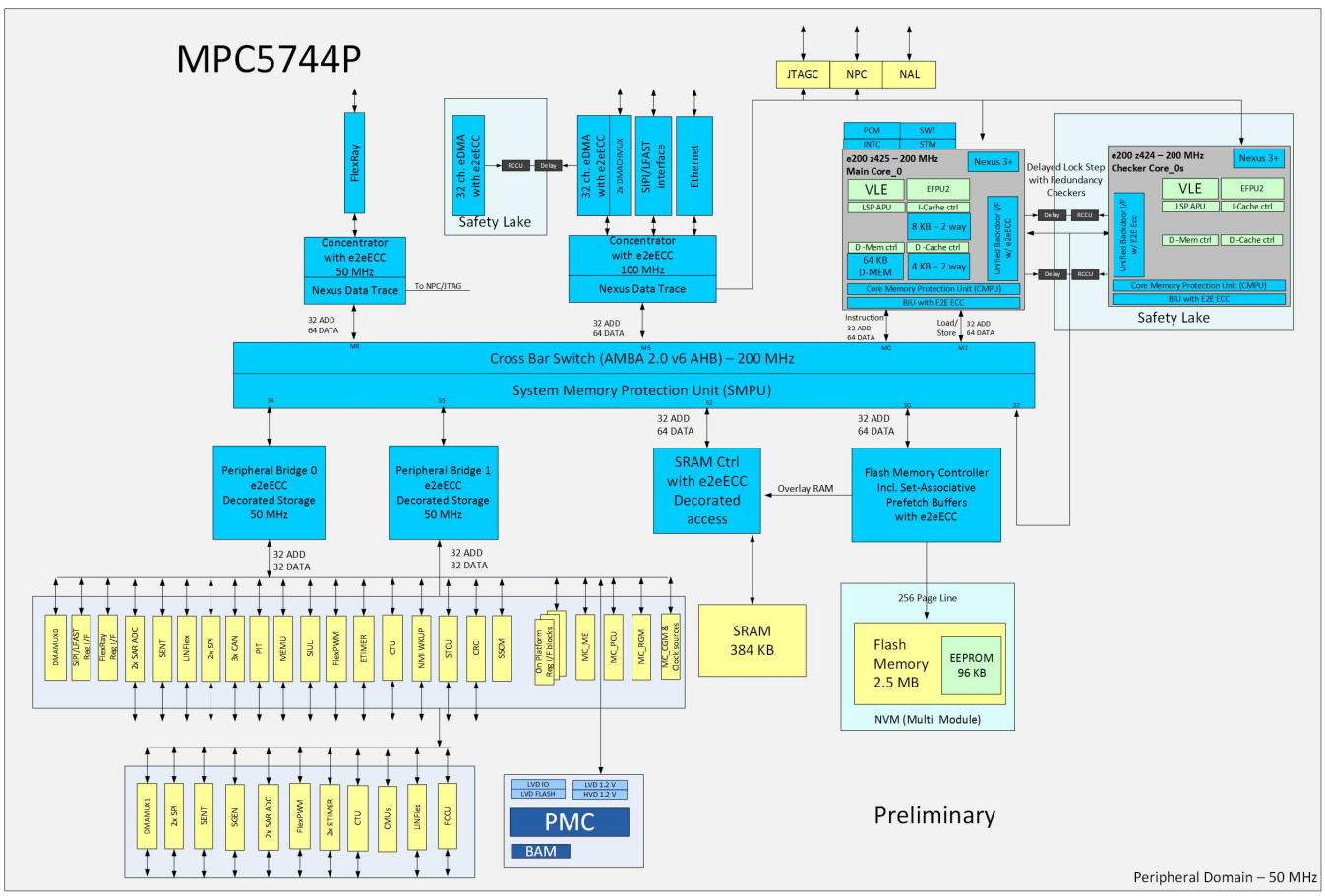



**Figure 1. System Block Diagram**

# 2 Pinouts

## 2.1 Package pinouts and ballmap

The following figures show the LQFP pinout and the BGA ballmap.

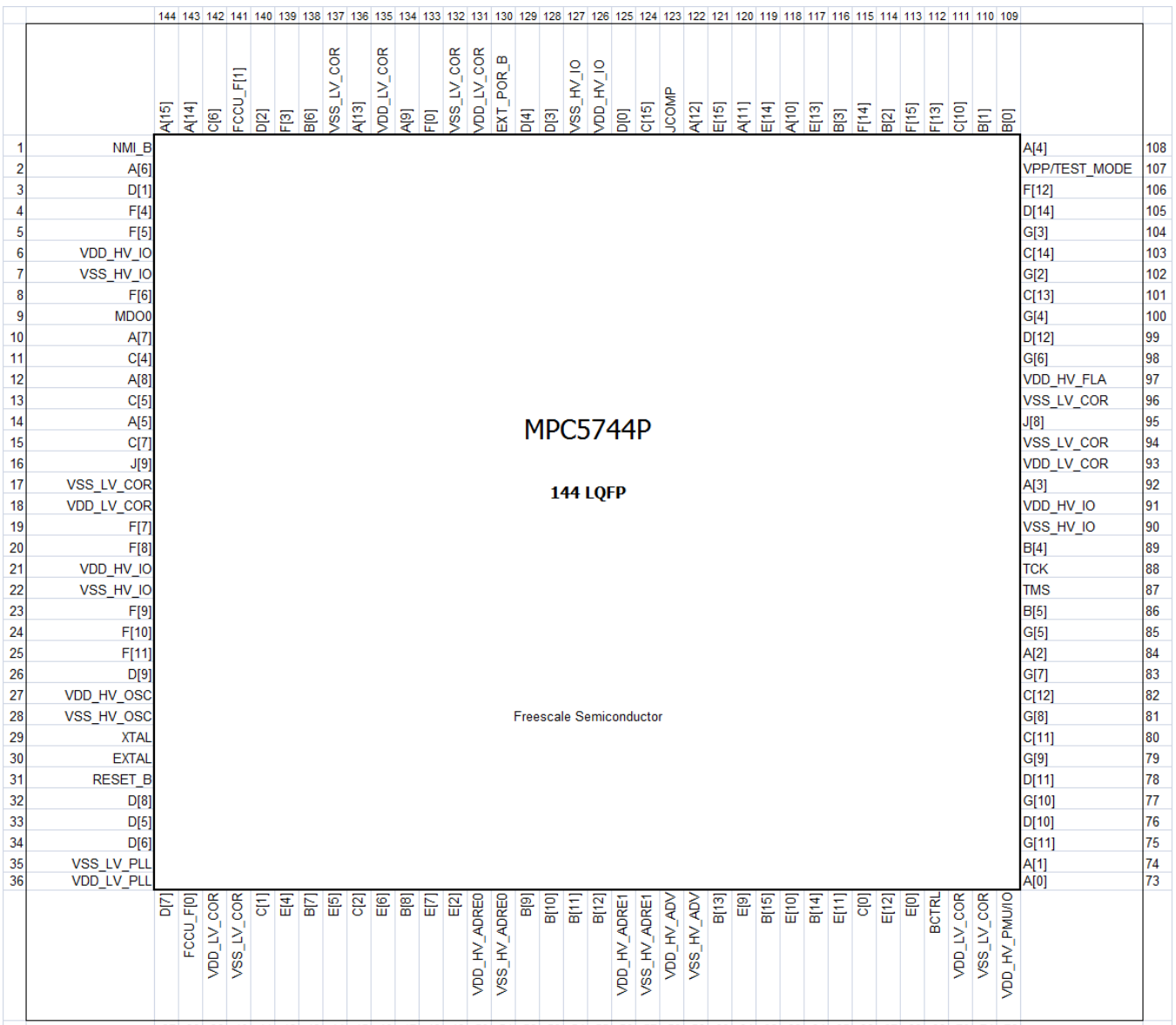
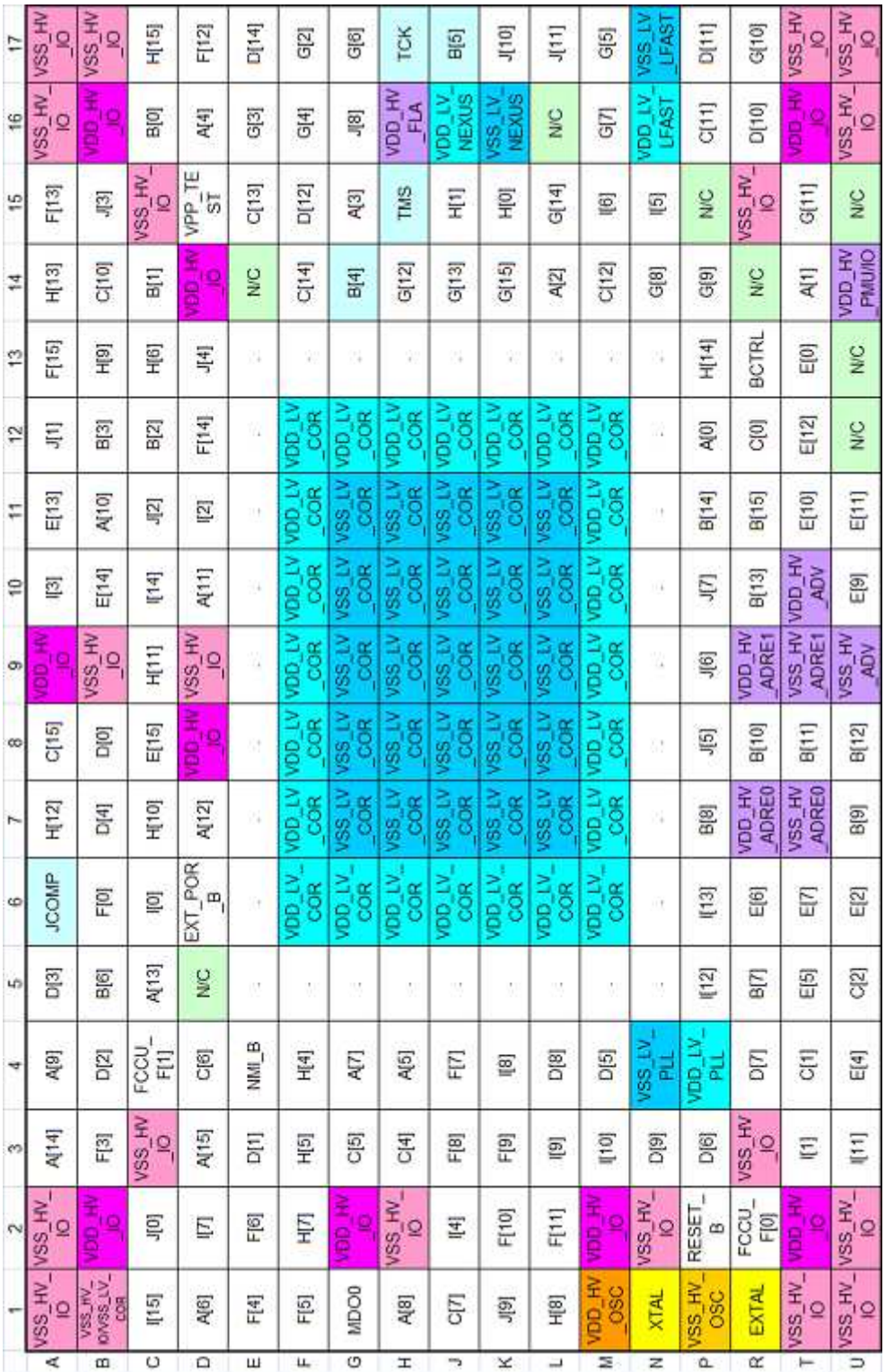



**Figure 2. 144LQFP pinout**



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS_HV_IO | VSS_HV_IO | A[14] | A[9] | D[3] | JCOMP | H[12] | C[15] | VDD_HV_IO | I[3] | E[13] | J[1] | F[15] | H[13] | F[13] | VSS_HV_IO | VSS_HV_IO |
| B | VSS_HV_IO/VSS_LV_COR | VDD_HV_IO | F[3] | D[2] | B[6] | F[0] | D[4] | D[0] | VSS_HV_IO | E[14] | A[10] | B[3] | H[9] | C[10] | J[3] | VDD_HV_IO | VSS_HV_IO |
| C | I[15] | J[0] | VSS_HV_IO | FCCU_F[1] | A[13] | I[0] | H[10] | E[15] | H[11] | I[14] | J[2] | B[2] | H[6] | B[1] | VSS_HV_IO | B[0] | H[15] |
| D | A[6] | I[7] | A[15] | C[6] | N/C | EXT_POR_B | A[12] | VDD_HV_IO | VSS_HV_IO | A[11] | I[2] | F[14] | J[4] | VDD_HV_IO | VPP_TEST | A[4] | F[12] |
| E | F[4] | F[6] | D[1] | NMI_B | . | . | . | . | . | . | . | . | . | N/C | C[13] | G[3] | D[14] |
| F | F[5] | H[7] | H[5] | H[4] | . | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | . | C[14] | D[12] | G[4] | G[2] |
| G | MDO0 | VDD_HV_IO | C[5] | A[7] | . | VDD_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VDD_LV_COR | . | B[4] | A[3] | J[8] | G[6] |
| H | A[8] | VSS_HV_IO | C[4] | A[5] | . | VDD_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VDD_LV_COR | . | G[12] | TMS | VDD_HV_FLA | TCK |
| J | C[7] | I[4] | F[8] | F[7] | . | VDD_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VDD_LV_COR | . | G[13] | H[1] | VDD_LV_NEXUS | B[5] |
| K | J[9] | F[10] | F[9] | I[8] | . | VDD_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VDD_LV_COR | . | G[15] | H[0] | VSS_LV_NEXUS | J[10] |
| L | H[8] | F[11] | I[9] | D[8] | . | VDD_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VSS_LV_COR | VDD_LV_COR | . | A[2] | G[14] | N/C | J[11] |
| M | VDD_HV_OSC | VDD_HV_IO | I[10] | D[5] | . | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | VDD_LV_COR | . | C[12] | I[6] | G[7] | G[5] |
| N | XTAL | VSS_HV_IO | D[9] | VSS_LV_PLL | . | . | . | . | . | . | . | . | . | G[8] | I[5] | VDD_LV_LFAST | VSS_LV_LFAST |
| P | VSS_HV_OSC | RESET_B | D[6] | VDD_LV_PLL | I[12] | I[13] | B[8] | J[5] | J[6] | J[7] | B[14] | A[0] | H[14] | G[9] | N/C | C[11] | D[11] |
| R | EXTAL | FCCU_F[0] | VSS_HV_IO | D[7] | B[7] | E[6] | VDD_HV_ADRE0 | B[10] | VDD_HV_ADRE1 | B[13] | B[15] | C[0] | BCTRL | N/C | VSS_HV_IO | D[10] | G[10] |
| T | VSS_HV_IO | VDD_HV_IO | I[1] | C[1] | E[5] | E[7] | VSS_HV_ADRE0 | B[11] | VSS_HV_ADRE1 | VDD_HV_ADV | E[10] | E[12] | E[0] | A[1] | G[11] | VDD_HV_IO | VSS_HV_IO |
| U | VSS_HV_IO | VSS_HV_IO | I[11] | E[4] | C[2] | E[2] | B[9] | B[12] | VSS_HV_ADV | E[9] | E[11] | N/C | N/C | VDD_HV_PMU/IO | N/C | VSS_HV_IO | VSS_HV_IO |

**Figure 3. 257MAPBGA ballmap**

## 2.2 Pin/ball descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the device. Note that this section is under development.

### 2.2.1 Pin/ball startup and reset states

The following table provides startup state and reset state information for device pins/balls.

The startup state and subsequent states of the following pins/balls cannot be configured by the user:

- JCOMP
- TMS
- TCK
- XTAL/EXTAL
- FCCU_F[0] and FCCU_F[1]
- EXT_POR_B
- RESET_B

The user can configure the state after reset of the following pins/balls by programming the applicable MSCRs/IMCRs:

- GPIOs
- Analog inputs
- TDI
- TDO
- NMI_B
- FAB
- ABS[0]
- ABS[2]

**Table 3. Pin/ball startup and reset states**

| Pin/ball | Startup state[1], [2] | State during reset | State after reset | 144LQFP | 257MAPBGA |
|---|---|---|---|---|---|
| GPIOs | hi-z | hi-z | hi-z | Note[3] | Note[3] |
| Analog inputs[4] | hi-z | hi-z | hi-z | Note[3] | Note[3] |
| JCOMP (TRST) | hi-z | input, weak pull-down | input, weak pull-down | Note[5] | Note[5] |
| TDI | hi-z | input, weak pull-up | input, weak pull-up | Note[5] | Note[5] |
| TDO | hi-z | output, hi-z | output, hi-z | Note[5] | Note[5] |
| TMS[6] | hi-z | input, weak pull-up | input, weak pull-up | Note[5] | Note[5] |

*Table continues on the next page...*

**Table 3. Pin/ball startup and reset states (continued)**

| Pin/ball | Startup state[1], [2] | State during reset | State after reset | 144LQFP | 257MAPBGA |
|---|---|---|---|---|---|
| TCK[6] | hi-z | input, weak pull-up | input, weak pull-up | Note[5] | Note[5] |
| XTAL/EXTAL | hi-z | hi-z | hi-z | Note[5] | Note[5] |
| FCCU_F[0][6] | hi-z | input, hi-z | output/input, hi-z | 38 | R2 |
| FCCU_F[1][6] | hi-z | input, hi-z | output/input, hi-z | 141 | C4 |
| EXT_POR_B | hi-z | input, weak pull-down | input, weak pull-down | Note[5] | Note[5] |
| RESET_B | hi-z | input, weak pull-down | input, weak pull-down | Note[5] | Note[5] |
| NMI_B | hi-z | input, weak pull-up | input,weak pull-up | Note[5] | Note[5] |
| FAB | hi-z | input, weak pull-down | input, weak pull-down | Note[5] | Note[5] |
| ABS[2] | hi-z | input, weak pull-down | input, weak pull-down | Note[5] | Note[5] |
| ABS[0] | hi-z | input, weak pull-down | input, weak pull-down | Note[5] | Note[5] |

1. Startup state is exited when the core and high-voltage supplies reach minimum levels.
2. Pads marked “high impedance” for POR will be in either high-impedance or weak low drive state when VDD_LV_CORE is off and HV_VDD_IO is below 1.5 V.
3. See Generic pins/balls.
4. Not all non-supply or reference pins on the device are explicitly defined in this table.
5. See System pins/balls.
6. This pin/ball is dedicated to and directly connected to a peripheral module pin.

## 2.2.2 Power supply and reference voltage pins/balls

**Table 4. Power supply and reference voltage pins/balls**

| Supply | | | Package | |
|---|---|---|---|---|
| Symbol | Type | Description | 144LQFP | 257MAPBGA |
| $V_{DD\_LV\_COR}$ | Power | Low voltage power Supply | 18 | F6 |
| | | | 39 | F7 |
| | | | 70 | F8 |
| | | | 93 | F9 |
| | | | 131 | F10 |
| | | | 135 | F11 |
| | | | | F12 |
| | | | | G6 |
| | | | | G12 |
| | | | | H6 |
| | | | | H12 |
| | | | | J6 |
| | | | | J12 |
| | | | | K6 |
| | | | | K12 |

*Table continues on the next page...*

## Table 4. Power supply and reference voltage pins/balls (continued)

| Supply | | | Package | |
|---|---|---|---|---|
| Symbol | Type | Description | 144LQFP | 257MAPBGA |
| | | | | L6 |
| | | | | L12 |
| | | | | M6 |
| | | | | M7 |
| | | | | M8 |
| | | | | M9 |
| | | | | M10 |
| | | | | M11 |
| | | | | M12 |
| $V_{SS\_LV\_COR}$ | Ground | Low voltage ground. PLL Ground is also connected to low voltage ground for core logic on 144LQFP (pin 35). | 17 | B1 |
| | | | 35 | G7 |
| | | | 40 | G8 |
| | | | 71 | G9 |
| | | | 94 | G10 |
| | | | 96 | G11 |
| | | | 132 | H7 |
| | | | 137 | H8 |
| | | | | H9 |
| | | | | H10 |
| | | | | H11 |
| | | | | J7 |
| | | | | J8 |
| | | | | J9 |
| | | | | J10 |
| | | | | J11 |
| | | | | K7 |
| | | | | K8 |
| | | | | K9 |
| | | | | K10 |
| | | | | K11 |
| | | | | L7 |
| | | | | L8 |
| | | | | L9 |
| | | | | L10 |
| | | | | L11 |
| $V_{DD\_LV\_PLL}$ | Power | PLL low voltage Supply | 36 | P4 |
| $V_{SS\_LV\_PLL}$ | Ground | PLL low voltage Ground | 35 | N4 |

*Table continues on the next page...*

## Table 4. Power supply and reference voltage pins/balls (continued)

| Supply | | | Package | |
|---|---|---|---|---|
| **Symbol** | **Type** | **Description** | **144LQFP** | **257MAPBGA** |
| $V_{DD\_HV\_IO}$ | Power | High voltage Power Supply for I/O | 6 | A9 |
| | | | 21 | B2 |
| | | | 72 | B16 |
| | | | 91 | D8 |
| | | | 126 | D14 |
| | | | | G2 |
| | | | | M2 |
| | | | | T2 |
| | | | | T16 |
| | | | | U14 |
| $V_{SS\_HV\_IO}$ | Ground | High voltage Ground Supply for I/O | 7 | A1 |
| | | | 22 | A2 |
| | | | 90 | A16 |
| | | | 127 | A17 |
| | | | | B1 |
| | | | | B9 |
| | | | | B17 |
| | | | | C3 |
| | | | | C15 |
| | | | | D9 |
| | | | | H2 |
| | | | | N2 |
| | | | | R3 |
| | | | | R15 |
| | | | | T1 |
| | | | | T17 |
| | | | | U1 |
| | | | | U2 |
| | | | | U16 |
| | | | | U17 |
| $V_{DD\_HV\_PMU}$<br>$V_{DD\_HV\_PMU\_AUX}$ | Power | PMU high voltage Supply | 72 | U14 |
| $V_{DD\_HV\_OSC}$ | Power | Power Supply for the oscillator | 27 | M1 |
| $V_{SS\_HV\_OSC}$ | Ground | Ground Supply for the oscillator | 28 | P1 |
| $V_{DD\_HV\_FLA}$ | Power | Power Supply and decoupling pin for flash memory | 97 | H16 |
| $V_{DD\_HV\_ADV}$ | Power | High voltage Supply for ADC, TSENS, SGEN (3.3 V) | 58 | T10 |
| $V_{SS\_HV\_ADV}$ | Ground | High voltage Ground for ADC | 59 | U9 |

*Table continues on the next page...*

**Table 4. Power supply and reference voltage pins/balls (continued)**

| Supply | | | Package | |
|---|---|---|---|---|
| **Symbol** | **Type** | **Description** | **144LQFP** | **257MAPBGA** |
| $V_{DD\_HV\_ADRE0}$ | Supply | High voltage Supply for digital portion of ADC pads<br>Voltage reference of ADC/TSENS<br>High voltage Supply for ADC0 pads and shared pads for ADC0/1. | 50 | R7 |
| $V_{SS\_HV\_ADRE0}$ | Ground | High voltage Ground for digital portion of ADC pads<br>Voltage reference Ground of ADC/TSENS<br>High voltage Ground for ADC0 pads and shared pads for ADC0/1. | 51 | T7 |
| $V_{DD\_HV\_ADRE1}$ | Supply | High voltage Supply for digital portion of ADC pads<br>Voltage reference of ADC/TSENS<br>High voltage Supply for ADC1 pads, shared pads for ADC1/3, and shared pads for ADC2/3. | 56 | R9 |
| $V_{SS\_HV\_ADRE1}$ | Ground | High voltage Ground for digital portion of ADC pads<br>Voltage reference Ground of ADC/TSENS<br>High voltage Ground for ADC1 pads, shared pads for ADC1/3, and shared pads for ADC2/3. | 57 | T9 |
| $V_{DD\_LV\_LFAST}$ | Supply | LFAST PLL low voltage Supply | — | N16 |
| $V_{SS\_LV\_LFAST}$ | Ground | LFAST PLL low voltage Ground | — | N17 |
| $V_{DD\_LV\_NEXUS}$ | Supply | Aurora LVDS Supply | — | J16 |
| $V_{SS\_LV\_NEXUS}$ | Ground | Aurora LVDS Ground | — | K16 |

## 2.2.3 System pins/balls

The following table contains information about system pin functions for the devices.

**Table 5. System pins/balls**

| Symbol | Type | Description | 144LQFP | 257MAPBGA |
|---|---|---|---|---|
| NMI_B | Input | Non-maskable Interrupt | 1 | E4 |
| XTAL | Output | Output of the oscillator amplifier circuit | 29 | N1 |
| EXTAL | Input | Crystal oscillator input/external clock input | 30 | R1 |
| RESET_B | Input | Functional Reset | 31 | P2 |
| EXT_POR_B | Input | External Power On Reset | 130 | D6 |
| VPP_TEST[1] | Input | SoC Test Mode | 107 | D15 |
| JCOMP | Input | JTAGC, JTAG Compliance Enable | 123 | A6 |
| TCK | Input | JTAGC, Test Clock Input | 88 | H17 |
| TMS | Input | JTAGC, Test Mode Select | 87 | H15 |
| TDO | Output | JTAGC, Test Data Out | 89 | G14 |

*Table continues on the next page...*

**Table 5. System pins/balls (continued)**

| Symbol | Type | Description | 144LQFP | 257MAPBGA |
|---|---|---|---|---|
| TDI | Input | JTAGC, Test Data Input | 86 | J17 |
| MDO[0] | Output | NEXUS, Message data out pins; reflects the state of the internal power on reset signal until RESET is negated | 9 | G1 |
| MDO[3:1] | Output | NEXUS, Message data out pins | 4,5,8 | E1, F1, E2 |
| EVTO | Output | NEXUS, Event Out Pin | 24 | K2 |
| EVTI | Input | NEXUS, Event In Pin | 25 | L2 |
| MCKO | Output | NEXUS, Message clock out pin | 19 | J4 |
| MSEO[1:0] | Output | NEXUS, Message Start/End out pin | 20, 23 | J3, K3 |
| RDY_B | Output | NEXUS, Read/Write Transfer completed | — | J2 |
| | | | 16 | K1 |
| BCTRL | Output | Base control signal of external npn ballast | 69 | R13 |
| J[11], J[10] | -- | FSL Factory Test[2] | — | L17, K17 |

1. VPP_TEST must be connected to ground.
2. Do not connect on the board.

## 2.2.4 LVDS pins/balls

The following tables contain information on LVDS pin functions for the devices.

**Table 6. SIPI LFAST LVDS pin descriptions**

| Functional block | Port pin | Signal | Signal description | Direction | 257MAPBGA |
|---|---|---|---|---|---|
| SIPI LFAST[1, 2] | I[5] | LFAST_TXN | SIPI/ LFAST, LVDS Transmit Negative Terminal | O | N15 |
| | C[12][3] | LFAST_TXP | SIPI/ LFAST, LVDS Transmit Positive Terminal | O | M14 |
| | I[6] | LFAST_RXN | SIPI/ LFAST, LVDS Receive Negative Terminal | I | M15 |
| | G[7][3] | LFAST_RXP | SIPI/ LFAST, LVDS Receive Positive Terminal | I | M16 |

1. DRCLK and TCK/DRCLK usage for SIPI LFAST are described in the reference manual's SIPI LFAST chapters.
2. For the MSCR SSS value of the port pin, see Table 1.
3. The 144LQFP package has G[7] and C[12] but no SIPI LFAST functionality.

**CAUTION**

SIPI LFAST pins are muxed with GPIOs. Do not use GPIO and SIPI LFAST functionality in parallel.

**Table 7. Aurora LVDS pin descriptions**

| Functional block | Pad | Signal | Signal description | Direction | 257MAPBGA[1] |
|---|---|---|---|---|---|
| Nexus Aurora High Speed Trace | G[12] | TX0P | Nexus Aurora High Speed Trace Lane 0, LVDS Positive Terminal | O | H14 |
| | G[13] | TX0N | Nexus Aurora High Speed Trace Lane 0, LVDS Negative Terminal | O | J14 |
| | G[14] | TX1P | Nexus Aurora High Speed Trace Lane 1, LVDS Positive Terminal | O | L15 |
| | G[15] | TX1N | Nexus Aurora High Speed Trace Lane 1, LVDS Negative Terminal | O | K14 |
| | H[0] | CLKP | Nexus Aurora High Speed Trace Clock, LVDS Positive Terminal | I | K15 |
| | H[1] | CLKN | Nexus Aurora High Speed Trace Clock, LVDS Negative Terminal | I | J15 |

1. Nexus Aurora High Speed Trace is available only on the 257MAPBGA.

## 2.2.5 Generic pins/balls

The I/O signal descriptions for the device are in the following table. It contains the port definition, multiplexing, direction, pad type, and package pin/ball numbers for each I/O pin on the device.

MSCR registers are used for alternative (ALT) mode selection and programming of pad control options.

IMCR registers are used to configure input muxing by peripheral. See Peripheral input muxing for details.

For the pins which have Nexus functionality muxed with GPIO or other functions, the Nexus functionality of such pins is automatically set when the Nexus tool is connected to the device. The value in MSCR register may have value that does not correspond to Nexus functionality.

**Table 8. Pin muxing**

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| A[0] | MSCR[0] | 0000 (Default)[2] | GPIO[0] | SIUL2-GPIO[0] | General Purpose IO A[0] | I/O | 73 | P12 |
| | | 0001 | ETC0 | eTimer_0 | eTimer_0 Input/Output Data Channel 0 | I/O | | |
| | | 0010 | SCK | DSPI2 | DSPI 2 Input/Output Serial Clock | I/O | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[48] | 0001 | SCK | DSPI2 | DSPI 2 Input Serial Clock | I | | |
| | IMCR[59] | 0010 | ETC0 | eTimer_0 | eTimer_0 Input Data Channel 0 | I | | |
| | IMCR[173] | 0001 | REQ0 | SIUL2 | SIUL2 External Interrupt 0 | I | | |
| A[1] | MSCR[1] | 0000 (Default) | GPIO[1] | SIUL2-GPIO[1] | General Purpose IO A[1] | I/O | 74 | T14 |
| | | 0001 | ETC1 | eTimer_0 | eTimer_0 Input/Output Data Channel 1 | I/O | | |
| | | 0010 | SOUT | DSPI2 | DSPI 2 Serial Data Out | O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[60] | 0010 | ETC1 | eTimer_0 | eTimer_0 Input Data Channel 1 | I | | |
| | IMCR[174] | 0001 | REQ1 | SIUL2 | SIUL2 External Interrupt Source 1 | I | | |
| A[2] | MSCR[2] | 0000 (Default) | GPIO[2] | SIUL2-GPIO[2] | General Purpose IO A[2] | I/O | 84 | L14 |
| | | 0001 | ETC2 | eTimer_0 | eTimer_0 Input/Output Data Channel 2 | I/O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0011 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[169] | 0000 (Default) | ABS0 | MC_RGM | RGM external boot mode 1 | I | | |
| | IMCR[47] | 0010 | SIN | DSPI2 | DSPI 2 Serial Data Input | I | | |
| | IMCR[61] | 0010 | ETC2 | eTimer_0 | eTimer_0 Input Data Channel 2 | I | | |
| | IMCR[97] | 0001 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input 3 | I | | |
| | IMCR[175] | 0001 | REQ2 | SIUL2 | SIUL2 External Interrupt Source 2 | I | | |
| A[3] | MSCR[3] | 0000 (Default) | GPIO[3] | SIUL2-GPIO[3] | General Purpose IO A[3] | I/O | 92 | G15 |
| | | 0001 | ETC3 | eTimer_0 | eTimer_0 Input/Output Data Channel 3 | I/O | | |
| | | 0010 | CS0 | DSPI2 | DSPI 2 Peripheral Chip Select 0 | I/O | | |
| | | 0011 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[171] | 0000 (Default) | ABS2 | MC_RGM | RGM external boot mode 2 | I | | |
| | IMCR[62] | 0010 | ETC3 | eTimer_0 | eTimer_0 Input Data Channel 3 | I | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[49] | 0001 | CS0 | DSPI2 | DSPI 2 Peripheral Chip Select 0 | I | | |
| | IMCR[98] | 0001 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input 3 | I | | |
| | IMCR[176] | 0001 | REQ3 | SIUL2 | SIUL2 External Interrupt Source 3 | I | | |
| A[4] | MSCR[4] | 0000 (Default) | GPIO[4] | SIUL2-GPIO[4] | General Purpose IO A[4] | I/O | 108 | D16 |
| | | 0001 | ETC0 | eTimer_1 | eTimer_1 Input/Output Data Channel 0 | I/O | | |
| | | 0010 | CS1 | DSPI2 | DSPI 2 Peripheral Chip Select 1 | O | | |
| | | 0011 | ETC4 | eTimer_0 | eTimer_0 Input/Output Data Channel 4 | I/O | | |
| | | 0100 | A2 | FlexPWM_1 | FlexPWM_1 Channel A Input/ Output 2 | I/O | | |
| | | 0101-1111 | — | Reserved | — | — | | |
| | IMCR[112] | 0001 | A2 | FlexPWM_1 | FlexPWM_1 Channel A Input 2 | I | | |
| | IMCR[177] | 0001 | REQ4 | SIUL2 | SIUL2 External Interrupt Source 4 | I | | |
| | IMCR[172] | 0000 (Default) | FAB | MC_RGM | RGM Force Alternate Boot Mode | I | | |
| | IMCR[65] | 0001 | ETC0 | eTimer_1 | eTimer_1 Input Data Channel 0 | I | | |
| | IMCR[63] | 0011 | ETC4 | eTimer_0 | eTimer_0 Input Data Channel 4 | I | | |
| A[5] | MSCR[5] | 0000 (Default) | GPIO[5] | SIUL2-GPIO[5] | General Purpose IO A[5] | I/O | 14 | H4 |
| | | 0001 | CS0 | DSPI1 | DSPI 1 Peripheral Chip Select 0 | I/O | | |
| | | 0010 | ETC5 | eTimer_1 | eTimer_1 Input/Output Data Channel 5 | I/O | | |
| | | 0011 | CS7 | DSPI0 | DSPI 0 Peripheral Chip Select 7 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[70] | 0001 | ETC5 | eTimer_1 | eTimer_1 Input Data Channel 5 | I | | |
| | IMCR[178] | 0001 | REQ5 | SIUL2 | SIUL2 External Interrupt Source 5 | I | | |
| A[6] | MSCR[6] | 0000 (Default) | GPIO[6] | SIUL2-GPIO[6] | General Purpose IO A[6] | I/O | 2 | D1 |
| | | 0001 | SCK | DSPI1 | DSPI 1 Input/Output Serial Clock | I/O | | |
| | | 0010 | ETC2 | eTimer_2 | eTimer_2 Input/Output Data Channel 2 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[73] | 0001 | ETC2 | eTimer_2 | eTimer_2 Input Data Channel 2 | I | | |
| | IMCR[179] | 0001 | REQ6 | SIUL2 | SIUL2 External Interrupt Source 6 | I | | |
| A[7] | MSCR[7] | 0000 (Default) | GPIO[7] | SIUL2-GPIO[7] | General Purpose IO A[7] | I/O | 10 | G4 |
| | | 0001 | SOUT | DSPI1 | DSPI 1 Serial Data Out | O | | |
| | | 0010 | ETC3 | eTimer_2 | eTimer_2 Input/Output Data Channel 3 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[74] | 0001 | ETC3 | eTimer_2 | eTimer_2 Input Data Channel 3 | I | | |
| | IMCR[180] | 0001 | REQ7 | SIUL2 | SIUL2 External Interrupt Source 7 | I | | |
| A[8] | MSCR[8] | 0000 (Default) | GPIO[8] | SIUL2-GPIO[8] | General Purpose IO A[8] | I/O | 12 | H1 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | ETC4 | eTimer_2 | eTimer_2 Input/Output Data Channel 4 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[44] | 0001 | SIN | DSPI1 | DSPI 1 Serial Data Input | I | | |
| | IMCR[75] | 0001 | ETC4 | eTimer_2 | eTimer_2 Input Data Channel 4 | I | | |
| | IMCR[181] | 0001 | REQ8 | SIUL2 | SIUL2 External Interrupt Source 8 | I | | |
| A[9] | MSCR[9] | 0000 (Default) | GPIO[9] | SIUL2-GPIO[9] | General Purpose IO A[9] | I/O | 134 | A4 |
| | | 0001 | CS1 | DSPI2 | DSPI 2 Peripheral Chip Select 1 | O | | |
| | | 0010 | ETC5 | eTimer_2 | eTimer_2 Input/Output Data Channel 5 | I/O | | |
| | | 0011 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[76] | 0001 | ETC5 | eTimer_2 | eTimer_2 Input Data Channel 5 | I | | |
| | IMCR[98] | 0010 | B3 | FlexPWM_0 | FlexPWM_0 Channel B Input 3 | I | | |
| | IMCR[83] | 0001 | FAULT0 | FlexPWM_0 | FlexPWM_0 Fault Input 0 | I | | |
| | IMCR[206] | 0011 | SENT_RX[1] | SENT_0 | SENT 0 Receiver channel 1 | I | | |
| A[10] | MSCR[10] | 0000 (Default) | GPIO[10] | SIUL2-GPIO[10] | General Purpose IO A[10] | I/O | 118 | B11 |
| | | 0001 | CS0 | DSPI2 | DSPI 2 Peripheral Chip Select 0 | O | | |
| | | 0010 | B0 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 0 | I/O | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0011 | X2 | FlexPWM_0 | FlexPWM_0 Auxiliary Input/ Output 2 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[49] | 0010 | CS0 | DSPI2 | DSPI 2 Peripheral Chip Select 0 | I/O | | |
| | IMCR[89] | 0001 | B0 | FlexPWM_0 | FlexPWM_0 Channel B Input 0 | I | | |
| | IMCR[96] | 0001 | X2 | FlexPWM_0 | FlexPWM_0 Auxiliary Input 2 | I | | |
| | IMCR[182] | 0001 | REQ9 | SIUL2 | SIUL2 External Interrupt Source 9 | I | | |
| | IMCR[214] | 0011 | SENT_RX[1] | SENT_1 | SENT 1 Receiver channel 1 | I | | |
| A[11] | MSCR[11] | 0000 (Default) | GPIO[11] | SIUL2-GPIO[11] | General Purpose IO A[11] | I/O | 120 | D10 |
| | | 0001 | SCK | DSPI2 | DSPI 2 Input/Output Serial Clock | I/O | | |
| | | 0010 | A0 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 0 | I/O | | |
| | | 0011 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 2 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[48] | 0010 | SCK | DSPI2 | DSPI 2 Input Serial Clock | I | | |
| | IMCR[88] | 0001 | A0 | FlexPWM_0 | FlexPWM_0 Channel A Input 0 | I | | |
| | IMCR[94] | 0001 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input 2 | I | | |
| | IMCR[183] | 0001 | REQ10 | SIUL2 | SIUL2 External Interrupt Source 10 | I | | |
| A[12] | MSCR[12] | 0000 (Default) | GPIO[12] | SIUL2-GPIO[12] | General Purpose IO A[12] | I/O | 122 | D7 |
| | | 0001 | SOUT | DSPI2 | DSPI 2 Serial Data Out | O | | |
| | | 0010 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 2 | I/O | | |
| | | 0011 | B2 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 2 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[94] | 0010 | A2 | FlexPWM_0 | FlexPWM_0 Channel A Input 2 | I | | |
| | IMCR[95] | 0001 | B2 | FlexPWM_0 | FlexPWM_0 Channel B Input 2 | I | | |
| | IMCR[184] | 0001 | REQ11 | SIUL2 | SIUL2 External Interrupt Source 11 | I | | |
| A[13] | MSCR[13] | 0000 (Default) | GPIO[13] | SIUL2-GPIO[13] | General Purpose IO A[13] | I/O | 136 | C5 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | B2 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 2 | I/O | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[83] | 0010 | FAULT0 | FlexPWM_0 | FlexPWM_0 Fault Input 0 | I | | |
| | IMCR[95] | 0010 | B2 | FlexPWM_0 | FlexPWM_0 Channel B Input 2 | I | | |
| | IMCR[47] | 0001 | SIN | DSPI2 | DSPI 2 Serial Data Input | I | | |
| | IMCR[185] | 0001 | REQ12 | SIUL2 | SIUL2 External Interrupt Source 12 | I | | |
| A[14] | MSCR[14] | 0000 (Default) | GPIO[14] | SIUL2-GPIO[14] | General Purpose IO A[14] | I/O | 143 | A3 |
| | | 0001 | TXD | CAN1 | CAN 1 Transmit Pin | O | | |
| | | 0010 | ETC4 | eTimer_1 | eTimer_1 Input/Output Data Channel 4 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[69] | 0001 | ETC4 | eTimer_1 | eTimer_1 Input Data Channel 4 | I | | |
| | IMCR[186] | 0001 | REQ13 | SIUL2 | SIUL2 External Interrupt Source 13 | I | | |
| A[15] | MSCR[15] | 0000 (Default) | GPIO[15] | SIUL2-GPIO[15] | General Purpose IO A[15] | I/O | 144 | D3 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | ETC5 | eTimer_1 | eTimer_1 Input/Output Data Channel 5 | I/O | | |
| | | 0011-1111 | — | Reserved | — | — | | |
| | IMCR[32] | 0001 | RXD | CAN0 | CAN 0 Receive Pin | I | | |
| | IMCR[33] | 0001 | RXD | CAN1 | CAN 1 Receive Pin | I | | |
| | IMCR[70] | 0010 | ETC5 | eTimer_1 | eTimer_1 Input Data Channel 5 | I | | |
| | IMCR[187] | 0001 | REQ14 | SIUL2 | SIUL2 External Interrupt Source 14 | I | | |
| B[0] | MSCR[16] | 0000 (Default) | GPIO[16] | SIUL2-GPIO[16] | General Purpose IO B[0] | I/O | 109 | C16 |
| | | 0001 | TXD | CAN0 | CAN 0 Transmit Pin | O | | |
| | | 0010 | ETC2 | eTimer_1 | eTimer_1 Input/Output Data Channel 2 | I/O | | |
| | | 0011 | DEBUG0 | SSCM | SSCM Debug Output 0 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[67] | 0001 | ETC2 | eTimer_1 | eTimer_1 Input Data Channel 2 | I | | |
| | IMCR[188] | 0001 | REQ15 | SIUL2 | SIUL2 External Interrupt Source 15 | I | | |
| B[1] | MSCR[17] | 0000 (Default) | GPIO[17] | SIUL2-GPIO[17] | General Purpose IO B[1] | I/O | 110 | C14 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | ETC3 | eTimer_1 | eTimer_1 Input/Output Data Channel 3 | I/O | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | | 0011 | DEBUG1 | SSCM | SSCM Debug Output 1 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[32] | 0010 | RXD | CAN0 | CAN 0 Receive Pin | I | | |
| | IMCR[33] | 0010 | RXD | CAN1 | CAN 1 Receive Pin | I | | |
| | IMCR[68] | 0001 | ETC3 | eTimer_1 | eTimer_1 Input Data Channel 3 | I | | |
| | IMCR[189] | 0001 | REQ16 | SIUL2 | SIUL2 External Interrupt Source 16 | I | | |
| B[2] | MSCR[18] | 0000 (Default) | GPIO[18] | SIUL2-GPIO[18] | General Purpose IO B[2] | I/O | 114 | C12 |
| | | 0001 | TXD | LIN0 | LINFlexD 0 Transmit Pin | O | | |
| | | 0010 | CS4 | DSPI0 | DSPI 0 Peripheral Chip Select 4 | O | | |
| | | 0011 | DEBUG2 | SSCM | SSCM Debug Output 2 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[190] | 0001 | REQ17 | SIUL2 | SIUL2 External Interrupt Source 17 | I | | |
| B[3] | MSCR[19] | 0000 (Default) | GPIO[19] | SIUL2-GPIO[19] | General Purpose IO B[3] | I/O | 116 | B12 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | CS5 | DSPI0 | DSPI 0 Peripheral Chip Select 5 | O | | |
| | | 0011 | DEBUG3 | SSCM | SSCM Debug Output 3 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[165] | 0001 | RXD | LIN0 | LIN 0 Receive Pin | I | | |
| B[4] | MSCR[20] | 0 | GPIO[20] | SIUL2-GPIO[20] | General Purpose IO B[4] | I/O | 89 | G14 |
| | | 0001 (Default) | TDO | NPC_HNDSHK | NPC_HNDSHK Test Data Out (TDO) | O | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[5] | MSCR[21] | 0000 (Default) | GPIO[21] | SIUL2-GPIO[21] | JTAGC Test Data In (TDI)[3]<br>General Purpose IO B[5] | I/O | 86 | J17 |
| | | 0001 | CS7 | DSPI0 | DSPI 0 Peripheral Chip Select 7 | O | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[6] | MSCR[22] | 0000 (Default) | GPIO[22] | SIUL2-GPIO[22] | General Purpose IO B[6] | I/O | 138 | B5 |
| | | 0001 | CLK_OUT | MC_CGM | CGM Clock out for off-chip use and observation | O | | |
| | | 0010 | CS2 | DSPI2 | DSPI 2 Peripheral Chip Select 2 | O | | |
| | | 0011-1111 | — | Reserved | — | — | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[191] | 0001 | REQ18 | SIUL2 | SIUL2 External Interrupt Source 18 | I | | |
| B[7] | MSCR[23] | 0000 (Default) | GPI[23][4] ADC0_AN[0] | SIUL2-GPI[23] | General Purpose Input B[7] | I | 43 | R5 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[165] | 0010 | RXD | LIN0 | LIN 0 Receive Pin | I | | |
| B[8] | MSCR[24] | 0 | GPI[24][4] ADC0_AN[1] | SIUL2-GPI[24] | General Purpose Input B[8] | I | 47 | P7 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[64] | 0001 | ETC5 | eTimer_0 | eTimer_0 Input Data Channel 5 | I | | |
| B[9] | MSCR[25] | 0000 (Default) | GPI[25][4] ADC0_ADC1_AN[11] | SIUL2-GPI[25] | General Purpose Input B[9] | I | 52 | U7 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[10] | MSCR[26] | 0000 (Default) | GPI[26][4] ADC0_ADC1_AN[12] | SIUL2-GPI[26] | General Purpose Input B[10] | I | 53 | R8 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[11] | MSCR[27] | 0000 (Default) | GPI[27][4] ADC0_ADC1_AN[13] | SIUL2-GPI[27] | General Purpose Input B[11] | I | 54 | T8 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[12] | MSCR[28] | 0000 (Default) | GPI[28][4] ADC0_ADC1_AN[14] | SIUL2-GPI[28] | General Purpose Input B[12] | I | 55 | U8 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| B[13] | MSCR[29] | 0000 (Default) | GPI[29][4] ADC1_AN[0] | SIUL2-GPI[29] | General Purpose Input B[13] | I | 60 | R10 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[166] | 0001 | RXD | LIN1 | LIN 1 Receive Pin | I | | |
| B[14] | MSCR[30] | 0000 (Default) | GPI[30][4] ADC1_AN[1] | SIUL2-GPI[30] | General Purpose Input B[14] | I | 64 | P11 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[63] | 0001 | ETC4 | eTimer_0 | eTimer_0 Input Data Channel 4 | I | | |
| | IMCR[192] | 0001 | REQ19 | SIUL2 | SIUL2 External Interrupt Source 19 | I | | |
| B[15] | MSCR[31] | 0000 (Default) | GPI[31][4] ADC1_AN[2] | SIUL2-GPI[31] | General Purpose Input B[15] | I | 62 | R11 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| | IMCR[193] | 0001 | REQ20 | SIUL2 | SIUL2 External Interrupt Source 20 | I | | |
| C[0] | MSCR[32] | 0000 (Default) | GPI[32][4] ADC1_AN[3] | SIUL2-GPI[32] | General Purpose Input C[0] | I | 66 | R12 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| C[1] | MSCR[33] | 0000 (Default) | GPI[33][4] ADC0_AN[2] | SIUL2-GPI[33] | General Purpose Input C[1] | I | 41 | T4 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| C[2] | MSCR[34] | 0000 (Default) | GPI[34][4] ADC0_AN[3] | SIUL2-GPI[34] | General Purpose Input C[2] | I | 45 | U5 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010-1111 | — | Reserved | — | — | | |
| C[4] | MSCR[36] | 0000 (Default) | GPIO[36] | SIUL2-GPIO[36] | General Purpose IO C[4] | I/O | 11 | H3 |
| | | 0001 | CS0 | DSPI0 | DSPI 0 Peripheral Chip Select 0 | I/O | | |
| | | 0010 | X1 | FlexPWM_0 | FlexPWM_0 Auxiliary Input/ Output 1 | I/O | | |
| | | 0011 | DEBUG4 | SSCM | SSCM Debug Output 4 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[93] | 0001 | X1 | FlexPWM_0 | FlexPWM_0 Auxiliary Input 1 | I | | |
| | IMCR[195] | 0001 | REQ22 | SIUL2 | SIUL2 External Interrupt Source 22 | I | | |
| C[5] | MSCR[37] | 0000 (Default) | GPIO[37] | SIUL2-GPIO[37] | General Purpose IO C[5] | I/O | 13 | G3 |
| | | 0001 | SCK | DSPI0 | DSPI 0 Input/Output Serial Clock | I/O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0011 | DEBUG5 | SSCM | SSCM Debug Output 5 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[86] | 0001 | FAULT3 | FlexPWM_0 | FlexPWM_0 Fault Input 3 | I | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[196] | 0001 | REQ23 | SIUL2 | SIUL2 External Interrupt Source 23 | I | | |
| C[6] | MSCR[38] | 0000 (Default) | GPIO[38] | SIUL2-GPIO[38] | General Purpose IO C[6] | I/O | 142 | D4 |
| | | 0001 | SOUT | DSPI0 | DSPI 0 Serial Data Out | O | | |
| | | 0010 | B1 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 1 | I/O | | |
| | | 0011 | DEBUG6 | SSCM | SSCM Debug Output 6 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[92] | 0001 | B1 | FlexPWM_0 | FlexPWM_0 Channel B Input 1 | I | | |
| | IMCR[197] | 0001 | REQ24 | SIUL2 | SIUL2 External Interrupt Source 24 | I | | |
| C[7] | MSCR[39] | 0000 (Default) | GPIO[39] | SIUL2-GPIO[39] | General Purpose IO C[7] | I/O | 15 | J1 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | A1 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 1 | I/O | | |
| | | 0011 | DEBUG7 | SSCM | SSCM Debug Output 7 | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[41] | 0001 | SIN | DSPI0 | DSPI 0 Serial Data Input | I | | |
| | IMCR[91] | 0001 | A1 | FlexPWM_0 | FlexPWM_0 Channel A Input 1 | I | | |
| C[10] | MSCR[42] | 0000 (Default) | GPIO[42] | SIUL2-GPIO[42] | General Purpose IO C[10] | I/O | 111 | B14 |
| | | 0001 | CS2 | DSPI2 | DSPI 2 Peripheral Chip Select 2 | O | | |
| | | 0010 | — | Reserved | — | — | | |
| | | 0011 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 3 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[84] | 0001 | FAULT1 | FlexPWM_0 | FlexPWM_0 Fault Input 1 | I | | |
| | IMCR[97] | 0010 | A3 | FlexPWM_0 | FlexPWM_0 Channel A Input 3 | I | | |
| C[11] | MSCR[43] | 0000 (Default) | GPIO[43] | SIUL2-GPIO[43] | General Purpose IO C[11] | I/O | 80 | P16 |
| | | 0001 | ETC4 | eTimer_0 | eTimer_0 Input/Output Data Channel 4 | I/O | | |
| | | 0010 | CS2 | DSPI2 | DSPI 2 Peripheral Chip Select 2 | O | | |
| | | 0011 | TX_ER | ENET_0 | Ethernet transmit Data Error | O | | |
| | | 0100 | CS0 | DSPI3 | DSPI 3 Peripheral Chip Select 0 | I/O | | |
| | | 0101-1111 | — | Reserved | — | — | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| | IMCR[52] | 0001 | CS0 | DSPI3 | DSPI 3 Peripheral Chip Select 0" | I | | |
| | IMCR[63] | 0100 | ETC4 | eTimer_0 | eTimer_0 Input Data Channel 4 | I | | |
| C[12][5] | MSCR[44] | 0000 (Default) | GPIO[44] | SIUL2-GPIO[44] | General Purpose IO C[12] | I/O | 82 | M14 |
| | | 0001 | ETC5 | eTimer_0 | eTimer_0 Input/Output Data Channel 5[6] | I/O | | |
| | | 0010 | CS3 | DSPI2 | DSPI 2 Peripheral Chip Select 3 | O | | |
| | | 0011 | LFAST_TXP | LFAST | SIPI/LFAST LVDS transmit positive terminal | O | | |
| | | 0100 | CS1 | DSPI3 | DSPI 3 Peripheral Chip Select 1 | O | | |
| | | 0101-1111 | — | Reserved | — | — | | |
| | IMCR[213] | 0100 | SENT_RX[0] | SENT1 | SENT 1 Receiver Channel 0 | I | | |
| | IMCR[64] | 0011 | ETC5 | eTimer_0 | eTimer_0 Input Data Channel 5 | I | | |
| C[13] | MSCR[45] | 0000 (Default) | GPIO[45] | SIUL2-GPIO[45] | General Purpose IO C[13] | I/O | 101 | E15 |
| | | 0001 | ETC1 | eTimer_1 | eTimer_1 Input/Output Data Channel 1 | I/O | | |
| | | 0010-0011 | — | Reserved | — | — | | |
| | | 0100 | A0 | FlexPWM_1 | FlexPWM_1 Channel A Input/ Output 0 | I/O | | |
| | | 0101-1111 | — | Reserved | — | — | | |
| | IMCR[38] | 0001 | EXT_IN | CTU_0 | CTU 0 External Trigger Input | I | | |
| | IMCR[66] | 0001 | ETC1 | eTimer_1 | eTimer_1 Input Data Channel 1 | I | | |
| | IMCR[87] | 0001 | EXT_SYNC | FlexPWM_0 | FlexPWM_0 External Trigger Input | I | | |
| | IMCR[105] | 0001 | A0 | FlexPWM_1 | FlexPWM_1 Channel A Input 0 | I | | |
| C[14] | MSCR[46] | 0000 (Default) | GPIO[46] | SIUL2-GPIO[46] | General Purpose IO C[14] | I/O | 103 | F14 |
| | | 0001 | ETC2 | eTimer_1 | eTimer_1 Input/Output Data Channel 2 | I/O | | |
| | | 0010 | EXT_TGR | CTU_0 | CTU0 External Trigger Output | O | | |
| | | 0011 | CS7 | DSPI1 | DSPI 1 Peripheral Chip Select 7 | O | | |
| | | 0100 | B0 | FlexPWM_1 | FlexPWM_1 Channel B Input/ Output 0 | I/O | | |
| | | 0101-1111 | — | Reserved | — | — | | |
| | IMCR[67] | 0010 | ETC2 | eTimer_1 | eTimer_1 Input Data Channel 2 | I | | |
| | IMCR[106] | 0001 | B0 | FlexPWM_1 | FlexPWM_1 Channel B Input 0 | I | | |

*Table continues on the next page...*

## Table 8. Pin muxing (continued)

| Port Pin | SIUL2 MSCR/ IMCR Number | MSCR/ IMCR SSS Value[1] | Signal | Module | Short Signal Description | Dir | LQFP144 | BGA257 |
|---|---|---|---|---|---|---|---|---|
| C[15] | MSCR[47] | 0000 (Default) | GPIO[47] | SIUL2-GPIO[47] | General Purpose IO C[15] | I/O | 124 | A8 |
| | | 0001 | FR_A_TXEN | FLEXRAY | FlexRay Transmit Enable Channel A | O | | |
| | | 0010 | ETC0 | eTimer_1 | eTimer_1 Input/Output Data Channel 0 | I/O | | |
| | | 0011 | A1 | FlexPWM_0 | FlexPWM_0 Channel A Input/ Output 1 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[38] | 0010 | EXT_IN | CTU_0 | CTU 0 External Trigger Input | I | | |
| | IMCR[65] | 0010 | ETC0 | eTimer_1 | eTimer_1 Input Data Channel 0 | I | | |
| | IMCR[87] | 0010 | EXT_SYNC | FlexPWM_0 | FlexPWM_0 External Sync Input | I | | |
| | IMCR[91] | 0010 | A1 | FlexPWM_0 | FlexPWM_0 Channel A Input 1 | I | | |
| D[0] | MSCR[48] | 0000 (Default) | GPIO[48] | SIUL2-GPIO[48] | General Purpose IO D[0] | I/O | 125 | B8 |
| | | 0001 | FR_A_TX | FLEXRAY | FlexRay Transmit Data Channel A | O | | |
| | | 0010 | ETC1 | eTimer_1 | eTimer_1 Input/Output Data Channel 1 | I/O | | |
| | | 0011 | B1 | FlexPWM_0 | FlexPWM_0 Channel B Input/ Output 1 | I/O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[66] | 0010 | ETC1 | eTimer_1 | eTimer_1 Input Data Channel 1 | I | | |
| | IMCR[92] | 0010 | B1 | FlexPWM_0 | FlexPWM_0 Channel B Input 1 | I | | |
| D[1] | MSCR[49] | 0000 (Default) | GPIO[49] | SIUL2-GPIO[49] | General Purpose IO D[1] | I/O | 3 | E3 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | ETC2 | eTimer_1 | eTimer_1 Input/Output Data Channel 2 | I/O | | |
| | | 0011 | EXT_TGR | CTU_0 | CTU 0 External Trigger Output | O | | |
| | | 0100-1111 | — | Reserved | — | — | | |
| | IMCR[67] | 0011 | ETC2 | eTimer_1 | eTimer_1 Input Data Channel 2 | I | | |
| | IMCR[136] | 0001 | FR_A_RX | FLEXRAY | FlexRay Channel A Receive Pin | I | | |
| D[2] | MSCR[50] | 0000 (Default) | GPIO[50] | SIUL2-GPIO[50] | General Purpose IO D[2] | I/O | 140 | B4 |
| | | 0001 | — | Reserved | — | — | | |
| | | 0010 | ETC3 | eTimer_1 | eTimer_1 Input/Output Data Channel 3 | I/O | | |
| | | 0011 | X3 | FlexPWM_0 | FlexPWM_0 Auxiliary Input/ Output 3 | I/O | | |

*Table continues on the next page...*