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SPEAr300

Embedded MPU with ARM926 core, flexible memory support, powerful connectivity features and human machine interface

Features

- ARM926EJ-S core up to 333 MHz
- High-performance 8-channel DMA
- Dynamic power-saving features
- Configurable peripheral functions on 102 shared I/Os (please refer to *Table 11: PL_GPIO multiplexing scheme*)
- Memory
  - 32 KB ROM and 56 KB internal SRAM
  - LPDDR-333/DDR2-666 external memory interface (up to 1 GB addressable memory)
  - SDIO/MMC card interface
  - Serial Flash memory interface (SMI)
  - Flexible static memory controller (FSMC) up to 16-bit data bus width, supporting external SRAM, NAND/NOR Flash and FPGAs
  - Serial SPI Flash interface
- Connectivity
  - 2 x USB 2.0 Host
  - USB 2.0 Device
  - Fast Ethernet (MII port)
  - 1x SSP Synchronous serial peripheral (SPI, Microwire or TI protocol)
  - 1x I^2C
  - 1x I^2S,
  - 1x fast IrDA interface
  - 1x UART interface
  - TDM bus (512 timeslots)
  - Up to 8 additional I^2C/SPI chip selects
- Security
  - C3 cryptographic accelerator
- Peripherals supported
  - Camera interface (ITU-601/656 and CSI2 support)
  - TFT/STN LCD controller (resolution up to 1024 x 768 and up to 24 bpp)

LFBGA289 (15 x 15 x 1.7 mm)

  - Touchscreen support (using the ADC)
  - 9 x 9 keyboard controller
  - Glueless management of up to 8 SLICs/CODECs
- Miscellaneous functions
  - Integrated real time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 Msps
  - 1-bit DAC
  - JPEG codec accelerator
  - Six 16-bit general purpose timers with capture mode and programmable prescaler
  - Up to 62 GPIOs

Applications

- SPEAr300 embedded MPU is configurable in 13 sets of peripheral functions targeting a range of applications:
  - General purpose NAND Flash or NOR Flash based devices
  - Digital photo frames
  - WiFi or IP phones (low end or high end)
  - ATA PABX systems (with or without I^2S)
  - 8-bit or 14-bit camera (with or without LCD)

Table 1. Device summary

Order code	Temp range, °C	Package	Packing
SPEAR300-2	- 40 to 85 °C	LFBGA289 (15x15 mm) pitch 0.8 mm	Tray

Contents

List of tables

List of figures

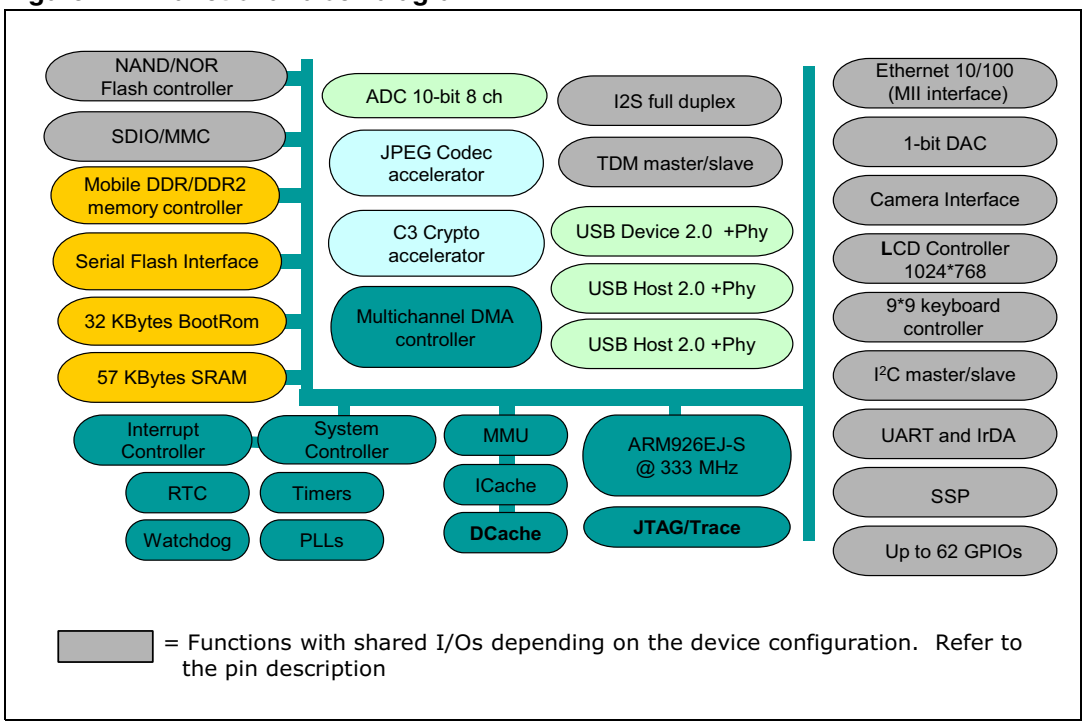
1 Description

The SPEAr300 is a member of the SPEAr family of embedded MPUs for networked devices. It is based on the powerful ARM926EJ-S processor (up to 333 MHz), widely used in applications where high computation performance is required.

In addition, SPEAr300 has an MMU that allows virtual memory management -- making the system compliant with advanced operating systems like Linux. It also offers 16 KB of data cache, 16 KB of instruction cache, JTAG and ETM (embedded trace macro-cell) for debug operations.

A full set of peripherals allows the system to be used in many applications, some typical applications being HMI, Security and VoIP phones.

Figure 1. Functional block diagram



1.1 Main features:

- ARM926EJ-S 32-bit RISC CPU, up to 333 MHz
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, bytecode Java mode (Jazelle™) for direct execution of Java code.
  - AMBA bus interface
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- 16-bit mobile DDR/DDR2 memory controller (up to 333 MHz)
- Serial memory interface
- SDIO/MMC interface supporting SPI, SD1, SD4 and SD8 mode with card detect, write protect, LED
- 8/16-bits NOR Flash/NAND Flash controller
- Boot capability from NAND Flash, serial/parallel NOR Flash, Ethernet and UART
- Boot and field upgrade capability from USB
- Multichannel DMA controller
- Color LCD Controller for STN/TFT display panels
  - up to 1024 x 768 resolution
  - 24 bpp true color
- Up to 62 GPIOs (muxed with peripheral I/Os), up to 22 with interrupt capability
- JPEG CODEC accelerator, 1 clock/pixel
- Camera interface ITU-601 with external or embedded synchronization (ITU-656 or CSI2). Picture limit is given by the line length that must be stored in a 2048 x 32 buffer
- C3 Crypto accelerator (DES/3DES/AES/SHA1)
- TDM master/slave
  - Up to 512 timeslots
  - Any input timeslot can be switched to any output timeslot, and/or can be buffered for computation
  - Up to 16 channels of 1 to 4 timeslots buffered during 32 ms
  - Up to 16 buffers can be played in output timeslots
- I^2S interface, full duplex with data buffer for left and right channels allowing up to 64 ms of voice buffer (for 32 bit samples).
- 10-bit ADC, 1 Msps, 8 inputs/1-bit DAC
- 9 x 9 keyboard controller
- Ethernet MAC 10/100 Mbps (MII PHY interface)
- Two USB2.0 host (high-full-low speed) with integrated PHY transceiver
- One USB2.0 device (high-full-low speed) with integrated PHY transceiver
- SSP master/slave (Motorola SPI, Texas instruments, National semiconductor protocols) up to 50 Mbps
- I^2C (slow- fast-high speed, up to 1.2 Mb/s) master/slave
- I/O peripherals
  - UART (speed rate up to 3 Mbps)
  - IrDA (FIR/MIR/SIR) 9.6 kbps to 4 Mbps speed-rate

- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes
  - CPU clock with software-programmable frequency
  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bit general purpose timers with programmable prescaler.
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1
- Boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x15 mm, pitch 0.8 mm)

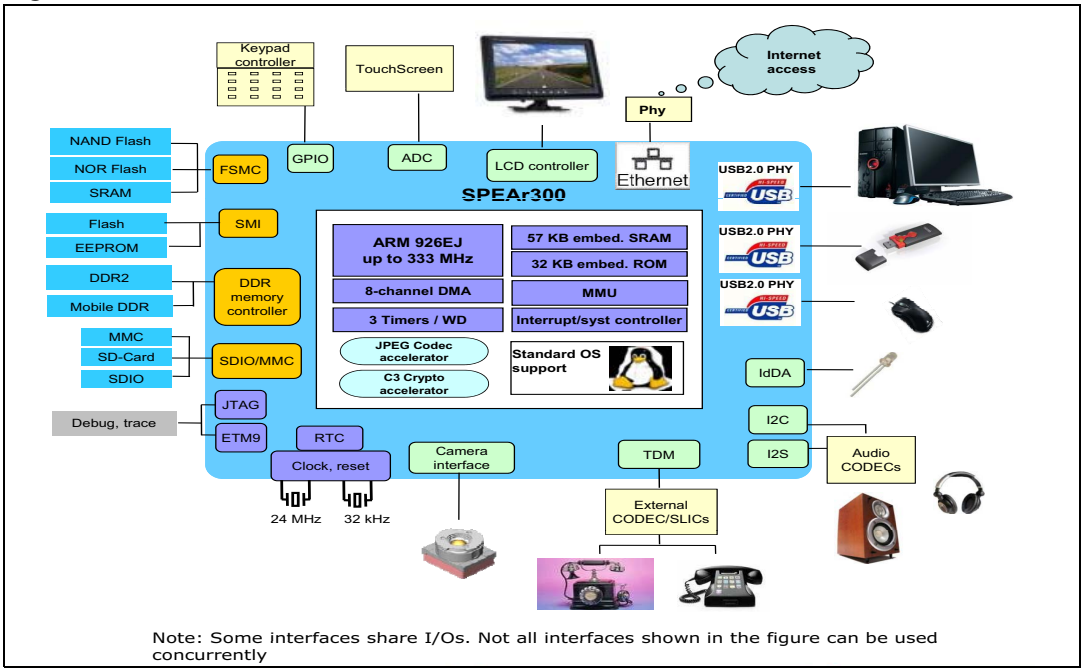
2 Architecture overview

The SPEAr300 internal architecture is based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix.

The switch matrix structure allows different subsystem dataflow to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

Figure 2. SPEAr300 overview



Note: Some interfaces share I/Os. Not all interfaces shown in the figure can be used concurrently

2.1 ARM926EJ-S CPU

The core of the SPEAr300 is an ARM926EJ-S reduced instruction set computer (RISC) processor.

It supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

The ARM CPU and is clocked at a frequency up to 333 MHz. It has a 16-Kbyte instruction cache, a 16-Kbyte data cache, and features a memory management unit (MMU) which makes it fully compliant with Linux and WindowsCE operating systems.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

2.2 System controller

The System Controller provides an interface for controlling the operation of the overall system.

Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable
- Remap control
- General purpose peripheral control r
- System and peripheral clock control and status

2.2.1 Clock and reset system

The clock system is a fully programmable block that generates all the clocks for the SPEAr300.

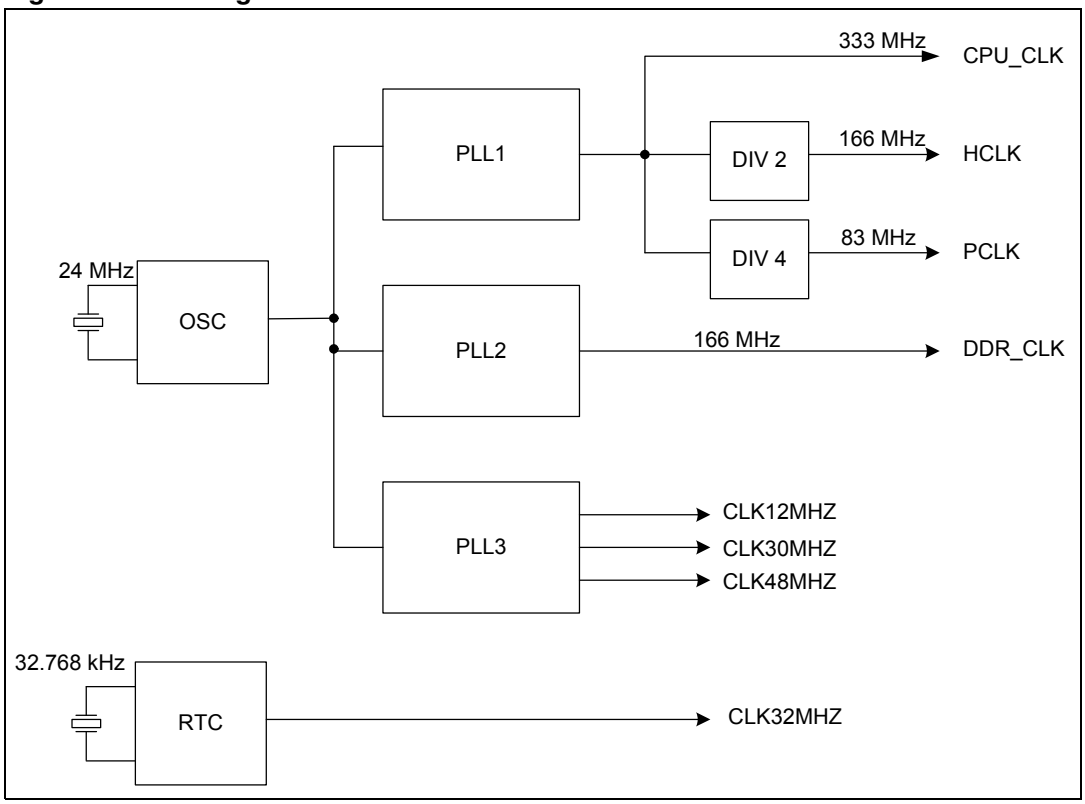
The default operating clock frequencies are:

- CPU_CLK @ 333 MHz for the CPU.
- HCLK @ 166 MHz for AHB bus and AHB peripherals.
- PCLK @ 83 MHz for, APB bus and APB peripherals.
- DDR_CLK @ 100-333 MHz for DDR memory interface.

The above frequencies are the maximum allowed values. The clock frequencies can be modified by programming the clock system registers.

The clock system consists of 2 main parts: a multi clock generator block and two internal PLLs.

Figure 3. Clock generator overview



The multi clock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr300 according to dedicated programmable registers.

Each PLL uses an oscillator input of 24 MHz to generate a clock signal at a frequency corresponding to the highest of the group. This is the reference signal used by the multi clock generator block to obtain all the other required clocks for the group. Its main feature is electromagnetic interference reduction capability.

The user can set up the PLL in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

In sleep mode the SPEAr300 runs with the PLL disabled so the available frequency is 24 MHz or a sub-multiple (/2, /4, /8).

2.2.2 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr300 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode**: In this mode the system clocks, HCLK and CPU_CLK, are disabled and the System Controller clock is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters

DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.

- **DOZE mode**: In this mode the system clocks, HCLK and CPU_CLK, and the System Controller clock are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

2.3 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

2.4 General purpose timers

SPEAr300 provides three general purpose timers (GPTs) acting as APB slaves.

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through SPEAr300 configuration registers (frequencies ranging from 3.96 Hz to 48 MHz can be synthesized).

Two different modes of operation are available:

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

2.5 Watchdog timer

The watchdog timer consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

2.6 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

2.7 Multichannel DMA controller

Within its basic subsystem, SPEAr300 provides an DMA controller (DMAC) able to service up to 8 independent DMA channels for sequential data transfers between single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).

Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

2.8 Embedded memory units

- 32 Kbytes of BootROM
- Up to 57 Kbytes of SRAM

The size of available SRAM varies according to the peripheral configuration mode See *Table 10*.:

- 57 Kbytes in modes 1 and 2
- 8 Kbytes in modes 3 to 13.

2.9 Mobile DDR/DDR2 memory controller

SPEAr300 integrates a high performances multi-channel memory controller able to support low power Mobile DDR and DDR2 double data rate memory devices. The multi-port architecture ensures memory is shared efficiently among different high-bandwidth client modules.

It has 6 internal ports. One of them is reserved for register access during the controller initialization while the other five are used to access the external memory.

It also include the physical layer (PHY) and some DLLs that allow fine tuning of all the timing parameters to maximize the data valid windows at any frequency in the allowed range.

2.10 Serial memory interface

SPEAr300 provides a serial memory interface (SMI) to SPI-compatible off-chip memories. These serial memories can be used for both data storage and code execution.

Main features:

- Supports the following SPI-compatible Flash and EEPROM devices:
  - STMicroelectronics M25Pxxx, M45Pxxx
  - STMicroelectronics M95xxx, except M95040, M95020 and M95010
  - ATMEL AT25Fxx
  - YMC Y25Fxx
  - SST SST25LFxx
- Acts always as a SPI master and up to 2 SPI slave memory devices are supported (through as many chip select signals), with up to 16 MB address space each
- SMI clock signal (SMICLK) is generated by SMI (and input to all slaves)
- SMICLK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by 7 programmable bits.

2.11 Flexible static memory controller (FSMC)

SPEAr300 provides a Flexible Static Memory Controller (FSMC) which interfaces the AHB bus to external NAND/NOR Flash memories and to asynchronous SRAM memories.

Main features:

- Provides an interface between AHB system bus and external parallel memory devices
- Interfaces static memory-mapped devices including RAM, ROM and synchronous burst Flash.
- For SRAM and Flash 8/16-bit wide, external memory and data paths are provided
- FSMC performs only one access at a time and only one external device is accessed.
- Supports little-endian and big-endian memory architectures
- AHB burst transfer handling to reduce access time to external devices
- Supplies an independent configuration for each memory bank
- Programmable timings to support a wide range of devices
  - Programmable wait states (up to 31)
  - Programmable bus turnaround cycles (up to 15)
  - Programmable output enable and write enable delays (up to 15)
- Provides independent chip select control for each memory bank
- Shares the address bus and the data bus with all the external peripherals. Only the chip selects are unique for each peripheral
- External asynchronous wait control

2.12 UART

Main features:

- Hardware/software flow control
- Modem control signals
- Separate 16 x 8 (16 locations deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps.

2.13 Fast IrDA controller (FIrDA)

The fast IrDA controller is a programmable infrared controller that acts as an interface to an off-chip infrared transceiver. This controller is able to perform the modulation and the demodulation of the infrared signals and the wrapping of the IrDA link access protocol (IrLAP) frames.

Main features:

- Supports IrDA serial infrared physical layer specification (IrPHY), version 1.3
- Supports IrDA link access protocol (IrLAP), version 1.1
- Serial infrared (SIR), with rates 9.6 Kbps, 19.2 Kbps, 38.4 Kbps, 57.6 Kbps and
- 115.2 Kbps
- Medium infrared (MIR), with rates 576 Kbps and 1.152 Mbps
- Fast infrared (FIR), with rate 4 Mbps.
- Transceiver interface compliant with all IrDA transceivers with configurable TX and RX signal polarity.
- Half-duplex infrared frame transmission and reception.
- 16-bit CRC algorithm for SIR and MIR, and 32-bit CRC algorithm for FIR.

2.14 Synchronous serial port (SSP)

SPEAr300 provides one synchronous serial port (SSP) block that offers a master or slave interface for synchronous serial communication with slave or master peripherals

Main features:

- Maximum speed of 41.5 Mbps
- Master and slave mode capability
- Programmable clock bit rate and prescale
- Separate transmit and receive first-in, first-out memory buffers, 16 bits wide, 8 locations deep
- Programmable choice of interface operation:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - TI synchronous serial
- Programmable data frame size from 4 to 16-bit.
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts
- DMA interface

2.15 I2C

The I2C controller, acts as an APB slave interface to the two-wire serial I2C bus.

Main features:

- Compliance to the I2C-bus specification (Philips)
- I^2C v2.0 compatible.
- Operates in three different speed modes:
  - Standard (100 kbps)
  - Fast (400 kbps)
  - High-speed (3.4 Mbps)
- Master and slave mode configuration possible
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Slave bulk data transfer capability.
- Connection with general purpose DMA is provided to reduce the CPU load.
- Interrupt or polled-mode operation

2.16 SPI_I2C multiple slave control

The SPI interface has only one slave select signal, SS0.

The I^2C interface does not allow control of several devices with the same address, which is frequently required for CODECs.

The SPI_I2C extension allows management of up to 8 SPI devices, or 8 I^2C devices at the same address (total SPI+I^2C devices=8).

The SPI extension is made by generating three more slave select signals SS1, SS2 and SS3.

The I^2C extension is done by replicating the I2C_SCL signal if the corresponding pin is set active.Otherwise the pin remains low, so that the start condition is not met.

Each of the 8 pins can reproduce either the SPI SS0 signal, or the I2C_SCL signal. The selection is made through a register.

2.17 TDM interface

The TDM block implements time division multiplexing.

Main features:

- TDM interface with 512 timeslots and up to 16 bufferization channels.
- 32 ms bufferization for 16 channels (of 4 bytes each)
- Supports master and slave mode operation
- Programmable clock and synchronization signal generation in master mode
- Clock & synchronization signal recovery in slave mode
- 8 programmable synchronization signals for CODECs
- Uses 11 pins:
  - SYNC7-0 are dedicated frame syncs for CODECs without timeslot recognition
  - CLK is the TDM clock
  - DIN is the TDM input and receives the data
  - DOUT is the TDM output and transmits the data. It can be high impedance on a unused timeslot
- The TDM interface can be the master or a slave of the CLK or SYNC0 signals.
- Timeslots can be used for switching or bufferization purposes:
  - Switching and bufferization can be used concurrently for different timeslots on the same TDM
  - The only limitation is that an output timeslot can not be switched and bufferized at the same time.
  - Timeslot switching: any of the output time slots can receive any input timeslot of the previous frame. The connection memory is part of the action memory, indicating which timeslot has to be output.
  - Timeslot bufferization: data from DIN is stored in an input buffer and data from an output buffer is played on DOUT. When the number of samples stored/played reaches the buffer size, the processor is interrupted in order to read the input buffer and prepare a new output buffer (or a DMA request is generated).

2.18 I²S interface

The I²S interface is very similar to the TDM block, but the frame sync is limited to Philips I²S definition. It is composed of 4 signals:

- I2S_LRCK; Left and right channels synchronization (Master/slave)
- I2S_CLK: I²S clock (Master/slave)
- I2S_DIN: I²S clock (Master/slave)
- I2S DOUT: I²S output (tri-state)

The DOUT line can be high impedance when out of samples. Data is always stored in 32 bit format in the buffer. A shift left operation is possible to left align the data.

Main features:

- Can be master or slave for the clock and sync signals
- Buffering of up to 1024 samples (512 left and 512 right samples representing 64 ms of voice). Data is stored always on 32 bits.
- Left and right channels are stored in two different buffers.
- Two banks are used to exchange data with the processor.
- In master mode, LRCK can be adjusted for 8, 16 or 32 bits width.
- Data width can be less than LRCK width. Input (received on I2S_DIN) and output (transmitted on DOUT) can be 8, 16 or 32 bits.

2.19 GPIOs

The General Purpose Input/Outputs (GPIOs) provide programmable inputs or outputs.

Main features:

- Individually programmable input/output pins implemented in 3 blocks:
  - Up to 6 base GPIOs in the basic subsystem (basGPIO)
  - Up to 18 GPIOs in the RAS subsystem (G10 and G8)
  - Up to 18 GPIOs in the keyboard controller
  - Up to 8 GPIOs in the independent GPIO block (GPIO[7:0])
- Programmable interrupt generation capability up to 22 pins.
- Base GPIOs and independent GPIOs support bit masking in both read and write operation through address lines.

Up to 62 general purpose I/Os are available in Mode 4 (LEND_IP_ph) (see *Table 10*).

- In this mode the application can use:
  - 10 GPIOs in G10 block
  - 8 GPIOs in G8 block (0 to 3 in output mode only)
  - 18 GPIO (keyboard controller I/Os in GPIO mode)
  - 6 base GPIOs (basGPIO) (enabled as alternate functions (see *Table 11*)
  - 8 IT pins (input only, with interrupt capability)
  - 4 SYNC outputs (SYNC4-7)
  - 8 SPI_I2C outputs

2.20 Keyboard controller

SPEAr300 provides a GPIO/keyboard controller block which is a two-mode input and output port.

Main features:

- The selection between the two modes is an APB Bus programmable bit.
- Keyboard interface uses 18 pins
- 18-bit general-purpose parallel port with input or output single pin programmability
- Pins can be used as general purpose I/O or to drive a 9 x 9 keyboard (81 keys)
- Keyboard scan period can be adjusted between 10 ms and 80 ms
- Supports auto-scanning with debouncing.

2.21 CLCD controller

SPEAr300 has a color liquid crystal display controller (CLCDC) that provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

Main features:

- Resolution programmable up to 1024 x 768
- 16-bpp true-color non-palletized, for color STN and TFT
- 24-bpp true-color non-palletized, for color TFT
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palletized displays for mono STN
- 1, 2, 4 or 8-bpp palletized color displays for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little and big-endian

2.22 Camera interface

The camera interface receives data from a sensor in parallel mode (8 to 14-bits) by storing a full line in a buffer memory, then requesting a DMA transfer or interrupting the processor.

When all the lines of a frame are transferred, a frame sync interrupt is generated.

Main features:

- Supports both hardware synchronization (HSYNC and VSYNC signals) and embedded synchronization (ITU656 or CSI2).
- Data carried by the bus can be:
  - Raw Bayer10 (10-14 bits/pixel – 2 Bytes), Raw Bayer8 (8 bits/pixel – 1 Byte),
  - YCbCr400 (1 Byte/pixel – 1 Byte), YCbCr422 (4 Bytes/ 2 pixels – 2*2 Bytes), YCbCr444 (3 Bytes/ pixel – 4 Bytes)
  - RGB444 (2 Bytes/ pixel – 2 Bytes), RGB565 (2 Bytes/ pixel – 2 Bytes), RGB888 (3 Bytes/ pixel – 4 Bytes)
  - JPEG compressed
- Data is stored in a 2048 x 32 buffer memory
- The camera interface can be assigned to two different set of pins. When using data greater than 8-bits, it is not possible to use the MII interface.
- Max pixel clock frequency is 100 MHz

2.23 SDIO controller/MMC card interface

The SDIO host controller has an AMBA compatible interface and conforms to the SD host controller standard specification version 2.0. It handles SD/SDIO protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness.

Main features:

- Meets the following standard specifications:
  - SD host controller standard specification version 2.0
  - SDIO card specification version 2.0
  - SD memory card specification draft version 2.0
  - SD memory card security specification version 1.01
  - MMC specification version 3.31 and 4.2
- Supports both DMA and non-DMA mode of operation
- Supports MMC plus and MMC mobile
- Card detection (insertion/removal)
- Password protection of cards
- Host clock rate variable between 0 and 48 MHz
- Supports 1-bit, 4-bit and 8-bit SD modes and SPI mode
- Supports Multi Media Card interrupt mode
- Allows card to interrupt host in 1-bit, 4-bit, 8-bit SD modes and SPI mode.
- Up to 100 Mbit/s data rate using 4 parallel data lines (sd4-bit mode)
- Up to 416 Mbit/s data rate using 8-bit parallel data lines (sd8-bit mode)
- Cyclic redundancy check CRC7 for command and CRC16 for data integrity
- Designed to work with I/O cards, read-only cards and read/write cards
- Error correction code (ECC) support for MMC4.2 cards
- Supports read wait control, suspend/resume operation
- Supports FIFO overrun and underrun condition by stopping the SD clock
- Conforms to AMBA specification AHB (2.0)

2.24 Ethernet controller

SPEAr300 provides an Ethernet MAC 10/100 Universal (commonly referred to as GMAC-UNIV), enabling to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard.

Note: GMAC is a hardware block implementing Ethernet MAC layer 2 processing. GMAC is configured for 10/100 Mbps operation on SPEAr3xx family and up to 1 Gbps on SPEAr600.

Main features:

- Compliant with the IEEE 802.3-2002 standard
- Supports the default MII interface to the external PHY
- Supports 10/100 Mbps data transfer rates
- Local FIFO available (4 Kbyte RX, 2 Kbyte TX)
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided for, as well as packet bursting and frame extension at 100 Mbps
- Programmable frame length to support both standard and jumbo Ethernet frames with size up to 16 Kbyte
- A variety of flexible addresses filtering modes are supported
- A set of control and status registers (CSRs) to control MAC core operation
- Native DMA with single-channel transmit and receive engines
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- An AHB slave acting as programming interface to access all CSRs, for both DMA and MAC core subsystems
- An AHB master for data transfer to system memory
- 32-bit AHB master bus width, supporting 32, 64, and 128-bit wide data transactions
- It supports both little and big endian memory architectures

2.25 USB2 host controller

SPEAr300 has a fully independent USB 2.0 host controller, consisting of the following six major blocks:

- An EHCI block for high-speed transfers (HS mode, 480 Mbps)
- 2 OHCI blocks for full and low speed transfers (FS and LS modes, 12 and 1.5 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

This host can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

The Host controller is capable of managing two different devices at a time on its two downstream ports.

- An HS device connected to either of the two ports is managed by the EHCI.
- An FS/LS device connected to port0 is managed by OHCI0.
- An FS/LS device connected to port1 is managed by OHCI1.