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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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SPEAr310

Embedded MPU with ARM926 core, flexible memory support, extended set of powerful connectivity features

Features

- ARM926EJ-S 333 MHz core
- High-performance 8-channel DMA
- Dynamic power-saving features
- Configurable peripheral functions multiplexed on 102 shared I/Os
- Memory:
  - 32 KB ROM and 8 KB internal SRAM
  - LPDDR-333/DDR2-666 external memory interface
  - Serial Flash Memory interface (SMI)
  - Flexible static memory controller (FSMC) up to 16-bit data bus width, supporting NAND Flash
  - External memory interface (EMI) up to 32-bit data bus width, supporting NOR Flash and FPGAs
- Connectivity
  - 2 x USB 2.0 Host
  - USB 2.0 Device
  - 1 x fast Ethernet MII port
  - 4 x fast Ethernet SMII ports
  - 1 x SSP Synchronous serial peripheral (SPI, Microwire or TI protocol) with 4 chip selects
  - 1 x I^2C
  - 1 x fast IrDA interface
  - 6 x UART interface
  - 1x TDM/E1 HDLC interface with 128/32 timeslots per frame respectively
  - 2x RS485 HDLC ports
- Security
  - C3 Cryptographic accelerator
- Miscellaneous functions
  - Integrated real time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 Msps

LFBGA289 (15 x 15 x 1.7 mm)

  - JPEG CODEC accelerator
  - Six 16-bit general purpose timers with programmable prescaler, 4 capture inputs
  - Up to 102 GPIOs with interrupt capability

Applications

The SPEAr310 embedded MPU is configurable for a range of telecom and networking applications such as:

- Routers, switches and gateways
- Remote apparatus control
- Metering concentrators

Table 1. Device summary

Order code	Temp range, °C	Package	Packing
SPEAR310-2	-40 to 85	LFBGA289 (15x15 mm, pitch 0.8 mm)	Tray

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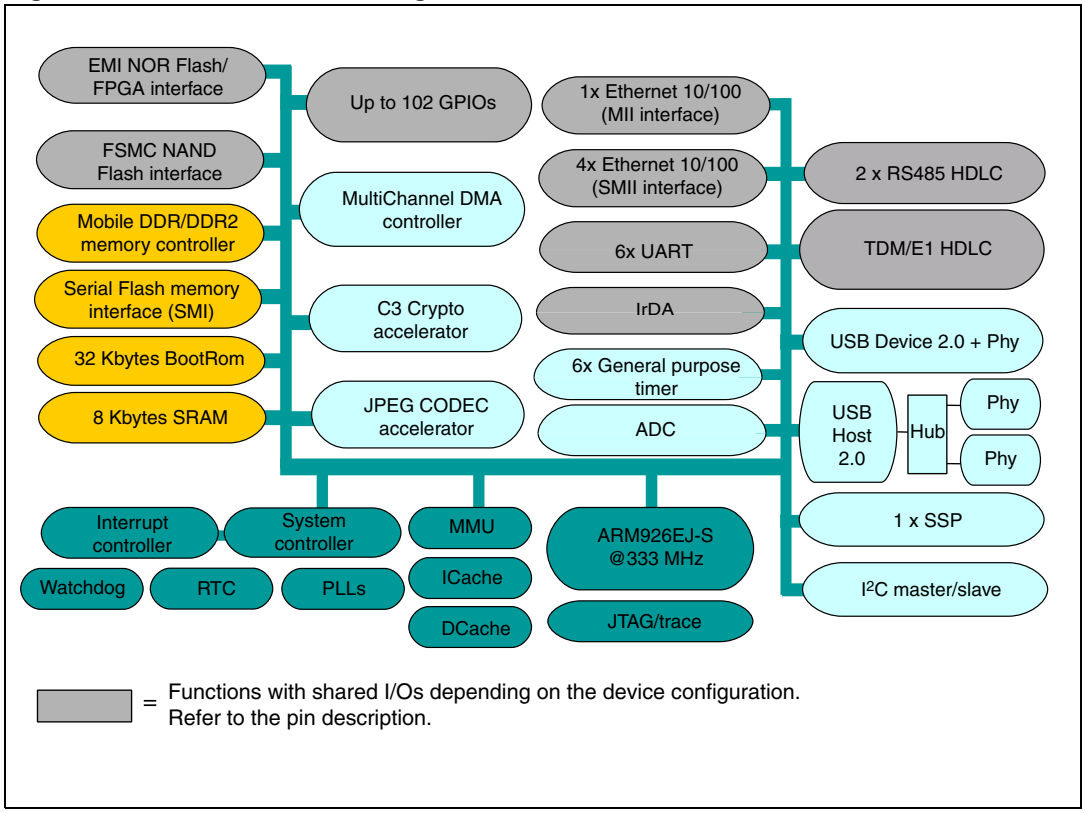
1 Description

The SPEAr310 is a member of the SPEAr family of embedded MPUs, optimized for telecom applications. It is based on the powerful ARM926EJ-S processor (up to 333 MHz), widely used in applications where high computation performance is required.

In addition, SPEAr310 has an MMU that allows virtual memory management -- making the system compliant with advanced operating systems, like Linux. It also offers 16 KB of data cache, 16 KB of instruction cache, JTAG and ETM (embedded trace macro-cell) for debug operations.

A full set of peripherals allows the system to be used in many applications, some typical applications being routers, switches and gateways as well as remote apparatus control and metering concentrators.

Figure 1. Functional block diagram



- ARM926EJ-S 32-bit RISC CPU, up to 333 MHz
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, Java mode (Jazelle™) for direct execution of Java bytecode.
  - AMBA bus interface
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- External DRAM memory interface:
  - 8/16-bit (mobile DDR@166 MHz)
  - 8/16-bit (DDR2@333 MHz)
- Serial memory interface
- 8/16-bits NAND Flash controller (FSMC)
- External memory interface (EMI) for connecting NOR Flash or FPGAs
- Boot capability from NAND Flash, serial/parallel NOR Flash
- Boot and field upgrade capability from USB
- High performance 8-channel DMA controller
- TDM/E1 HDLC, six-signal interface supporting duplex Tx/Rx communication
  - For TDM applications, up to 8 Mbps per Tx/Rx channel
    128 timeslots per frame (125 µs)
  - For E1 applications, up to 2 Mbps per Tx/Rx channel
    32 timeslots per frame (125 µs)
  - Compliant with ISO/IEC13239
  - Standard HDLC frame code/decode
- 2x RS485 HDLC ports:
  - Five interface signals
  - Supports duplex Tx/Rx communication
  - Maximum Tx/Rx data rate 3.88 Mbps
- 4x Ethernet MAC 10/100 Mbps with SMII PHY interface
- 1x Ethernet MAC 10/100 Mbps with MII PHY interface
- Two USB2.0 host (high-full-low speed) with integrated PHY transceiver
- One USB2.0 device (high-full-low speed) with integrated PHY transceiver
- Up to 102 GPIOs with interrupt capability
- Synchronous serial port (SSP), master/slave (supporting SPI, Microwire and TI sync protocols) up to 41.5 Mbps
- I^2C master/slave interface (slow-fast-high speed, up to 1.2 Mb/s)
- 1x UART with hardware flow control (up to 3 Mbps)
- 5x UARTs with software flow control (up to 5 Mbps)
- ADC 10-bit, 1 Msps 8 inputs
- JPEG CODEC accelerator 1 clock/pixel
- C3 Crypto accelerator (DES/3DES/AES/SHA1)
- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes
  - CPU clock with software-programmable frequency

  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bits general purpose timers with programmable prescaler
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1
- Boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x 15 mm, pitch 0.8 mm)

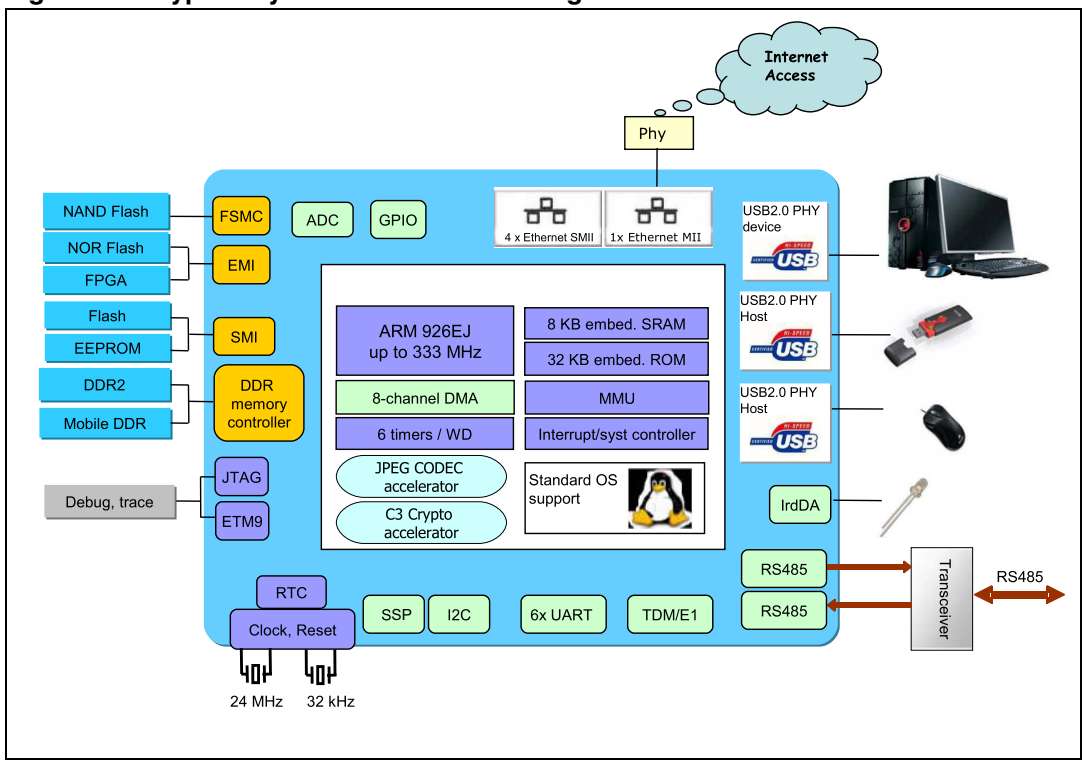
2 Architecture overview

The SPEAr310 internal architecture is based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix.

The switch matrix structure allows different subsystem dataflow to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

Figure 2. Typical system architecture using SPEAr310



2.1 CPU ARM 926EJ-S

The core of the SPEAr310 is an ARM926EJ-S reduced instruction set computer (RISC) processor.

It supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

The ARM CPU is clocked at a frequency up to 333 MHz. It has a 16-Kbyte instruction cache, a 16-Kbyte data cache, and features a memory management unit (MMU) which makes it fully compliant with Linux and WindowsCE operating systems.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

2.2 System controller

The System Controller provides an interface for controlling the operation of the overall system.

Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable

2.2.1 Clock and reset system

The clock system is a fully programmable block that generates all the clocks necessary to the chip (see *Figure 3*).

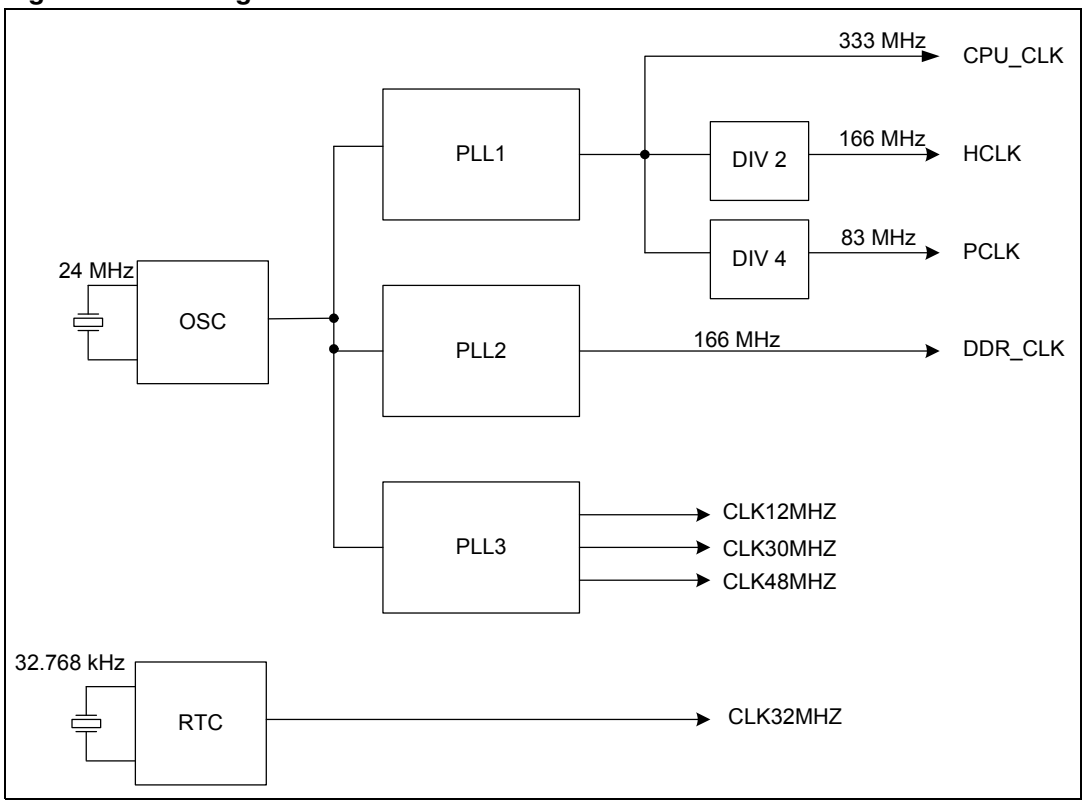
The default operating clock frequencies are:

- CPU_CLK @ 333 MHz for the CPU.
- HCLK @ 166 MHz for AHB bus and AHB peripherals.
- PCLK @ 83 MHz for, APB bus and APB peripherals.
- DDR_CLK @ 100-333 MHz for DDR memory interface.

The default values give the maximum allowed clock frequencies. The clock frequencies are fully programmable through dedicated registers.

The clock system consists of 2 main parts: a multi clock generator block and three internal PLLs.

Figure 3. Clock generator overview



The multi clock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr310 according to dedicated programmable registers.

Each PLL uses an oscillator input of 24 MHz to generate a clock signal at a frequency corresponding at the highest of the group. This is the reference signal used by the multi clock generator block to obtain all the other requested clocks for the group. Its main feature is electromagnetic interference reduction capability.

The user can set up the PLL in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

In sleep mode the SPEAr310 runs with the PLL disabled so the available frequency is 24 MHz or a sub-multiple (/2, /4, /8).

2.2.2 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr310 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode**: In this mode the system clocks, HCLK and CPU_CLK, are disabled and the System Controller clock is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters

DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.

- **DOZE mode**: In this mode the system clocks, HCLK and CPU_CLK, and the System Controller clock are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

2.2.3 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

2.2.4 General purpose timers

SPEAr310 provides three general purpose timers (GPTs) acting as APB slaves. The timers can capture input signals from up to 4 external pins (enabled as PL_GPIO alternate functions).

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through configuration registers (a frequency range from 3.96 Hz to 48 MHz can be synthesized).

Two different modes of operation are available :

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

2.2.5 Watchdog timer

The ARM watchdog module consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

2.2.6 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a

clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

Main features:

- Time-of-day clock in 24 hour mode
- Calendar
- Alarm capability
- Isolation mode, allowing RTC to work even if power is not supplied to the rest of the device.

2.3 Multichannel DMA controller

Within its basic subsystem, SPEAr310 provides an DMA controller (DMAC) able to service up to 8 independent DMA channels for sequential data transfers between single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).

Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

2.4 Embedded memory units

- 32 Kbytes of BootROM
- 8 Kbytes of SRAM

2.5 Mobile DDR/DDR2 memory controller

SPEAr310 integrates a high performance multi-channel memory controller able to support low power Mobile DDR and DDR2 double data rate memory devices. The multi-port architecture ensures memory is shared efficiently among different high-bandwidth client modules.

It has 6 internal ports. One of them is reserved for register access during the controller initialization while the other five are used to access the external memory.

It also includes the physical layer (PHY) and DLLs for fine tuning the timing parameters to maximize the data valid windows at different frequencies.

2.6 Serial memory interface

SPEAr310 provides a serial memory interface (SMI) to SPI-compatible off-chip memories.

These serial memories can be used either as data storage or for code execution.

Main features:

- Supports the following SPI-compatible Flash and EEPROM devices:
  - STMicroelectronics M25Pxxx, M45Pxxx
  - STMicroelectronics M95xxx, except M95040, M95020 and M95010
  - ATMEL AT25Fxx
  - YMC Y25Fxx
  - SST SST25LFxx
- Acts always as a SPI master and up to 2 SPI slave memory devices are supported (with seperate chip select signals), with up to 16 MB address space each
- SMI clock signal (SMICLK) is generated by SMI (and input to all slaves)
- SMICLK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by a programmable 7-bit prescaler allowing up to 127 different clock frequencies.

2.7 External memory interface (EMI)

The EMI Controller provides a simple external memory interface that can be used for example to connect to NOR Flash memory or FPGA devices.

Main features:

- Multiplexed address and data bus.
- EMI bus master
- 32, 16, 8-bit transfers.
- Can access 6 different peripherals using CS#, one at a time.
- Supports single asynchronous transfers.
- Supports peripherals which use Byte Lane procedure

2.8 Flexible static memory controller (FSMC)

SPEAr310 provides a Flexible Static Memory Controller (FSMC) which interfaces the AHB bus to external parallel NAND Flash memories.

Main features:

- 8/16-bit wide data path
- FSMC performs only one access at a time and only one external device is accessed.
- Supports little-endian and big-endian memory architectures.
- AHB burst transfer handling to reduce access time to external devices.
- Supplies an independent configuration for each memory bank.
- Programmable timings to support a wide range of devices.
  - Programmable wait states (up to 31).
  - Programmable bus turnaround cycles (up to 15).
  - Programmable output enable and write enable delays (up to 15).
- Independent chip select control for each memory bank.
- Shares the address bus and the data bus with all the external peripherals.
- Only chips selects are unique for each peripheral.
- External asynchronous wait control.

2.9 UARTs

The SPEAr310 has 5 UARTs featuring software flow control and 1 UART featuring hardware and/or software flow control.

2.9.1 UART with hardware flow control

Main features:

- Separate 16 x 8 (16 locations deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps
- Hardware and/or software flow control

2.9.2 UARTs with software flow control

Main features:

- Separate 16 x 8 (16 location deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 5 Mbps.

2.10 Synchronous serial port (SSP)

SPEAr310 provides one synchronous serial port (SSP) block that offers a master or slave interface to enables synchronous serial communication with slave or master peripherals.

Main features:

- Master or slave operation.
- Programmable clock bit rate and prescale.
- Separate transmit and receive first-in, first-out memory buffers, 16-bits wide, 8 locations deep.
- Programmable choice of interface operation:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - TI synchronous serial.
- Programmable data frame size from 4 to 16-bits.
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts.
- Internal loopback test mode available.
- DMA interface
- 4 chip selects available for non concurrent operations on 4 different devices.

2.11 I2C

Main features:

- Compliance to the I^2C bus specification (Philips)
- Supports three modes:
  - Standard (100 kbps)
  - Fast (400 kbps)
  - High-speed (3.4 Mbps)
- Clock synchronization
- Master and slave mode configuration possible
- Multi-master mode (bus arbitration)
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Slave bulk transfer mode
- Ignores CBUS addresses (predessor to I2C that used to share the I2C bus)
- Transmit and receive buffers
- Interrupt or polled-mode operation
- handles bit and byte waiting at all bus speeds
- Digital filter for the received SDA and SCL lines
- Handles component parameters for configurable software driver support

2.12 TDM/E1 HDLC controller

SPEAr310 features a TDM/E1 HDLC controller which is composed of two main blocks: Time Division Multiplexing (TDM) and High-level Data Link Control (HDLC) engines.

The internal HDLC controller can service up to 128 Tx/Rx channels simultaneously in conventional HDLC mode and supports super-channel configuration. Each channel bit rate is programmable from 4 kbit/s to 64 kbit/s. The maximum bit rate of the TDM interface is 8 Mbps.

2.12.1 TDM interface

Main features:

- Six interface signals
- Duplex Tx/Rx communication
- 128 timeslots per frame (125 µs)
- Up to 8 Mbps per Tx/Rx channel
- Supports any timeslot banding on any Tx/Rx channel
- Tx/Rx Data sending/sampling time is configurable after/on the rising/falling edge of TxCLK/RxCLK.
- Delay between the bit 0 of TS0 and the SYNC signal is configurable (0 - up to 3 Tx/Rx clock cycles delay)
- The TDM/E1 interface is entirely dedicated to the HDLC protocol

2.12.2 E1 interface

Main features:

- Six interface signals
- Duplex Tx/Rx communication
- Up to 2 Mbps per Tx/Rx channel
- 32 timeslots / frame (125 µs)
- Supports any timeslot banding on any Tx/Rx channel
- Tx/Rx Data sending/sampling time is configurable after/on the rising/falling edge of TxCLK/RxCLK.
- Delay between the bit 0 of TS0 and the SYNC signal is configurable (0 - up to 3 Tx/Rx clock cycle delay)

2.13 RS485 HDLC ports

SPEAr310 features two RS485 HDLC ports.

Main features:

- Each RS485 interface has five signals
- Supports duplex Tx/Rx communication
- Maximum Tx/Rx data rate of RS485 HDLC is 3.88 Mbps
- Supports collision detection and automatic frame re-transmission
- Data sending/sampling timing is configurable:
  - Tx Data can be sent out after the rising/falling edge of TxCLK
  - Rx Data are sampled on the rising/falling edge of RxCLK
- No clock duty cycle constraints, data sending/receiving depends only on the rising/falling edge of Tx/Rx clock

2.13.1 HDLC controller

Main features:

- Compliant with ISO/IEC13239
- Standard HDLC frame code/decode
- Opening flag
- One or two bytes for address recognition (reception) and insertion (transmission)
- Payload with bit stuffing
- Frame check sequence: 16 bit CRC with polynomial G(x) = X16+X12+X5+1
- Closing flag

2.14 GPIOs

A maximum of 102 GPIOs are available when part of the embedded IPs are not needed (see "Pin description" table).

Within its basic subsystem, SPEAr310 provides twelve General Purpose Input/Output (GPIO) block. Each GPIO block provides 8 programmable inputs or outputs.

Main features of the GPIO are:

- Eight individually programmable input/output pins (default to input at reset)
- An APB slave acting as control interface in "software mode"
- Programmable interrupt generation capability on any number of pins.
- Hardware control capability of GPIO lines for different system configurations.
- Bit masking in both read and write operation through address lines.

2.15 8-channel ADC

Main features:

- Successive approximation conversion method
- 10-bit resolution @1 Msps
- Hardware supporting up to 13.5 bits resolution at 8 ksps by oversampling and accumulation
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- INL ± 1 LSB, DNL ± 1 LSB
- Programmable conversion speed, (min. conversion time is 1 µs)
- Programmable averaging of results from 1 (No averaging) up to 128
- Programmable auto scan for all the eight channels.

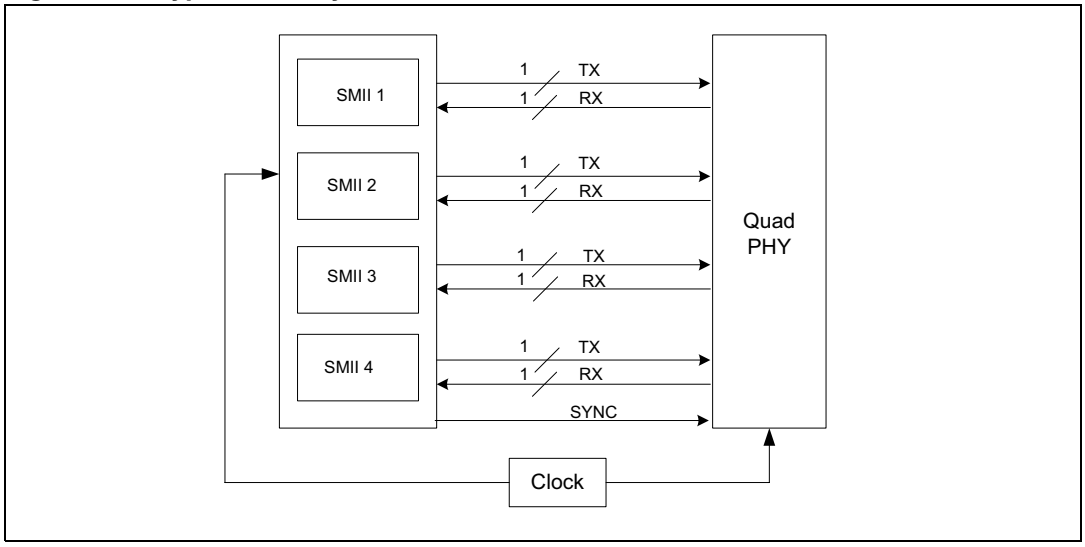
2.16 SMII Ethernet controller

SPEAr310 features four Ethernet MACs providing SMII interfaces.

Each MAC channel has dedicated TX/RX signals while synchronization and clock signals are common for PHY connection.

Figure 4 shows the typical SMII configuration (a generic example with four ports):

Figure 4. Typical SMII system



Each Ethernet port provides the following features:

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full and half duplex operation
- Statistics counter registers for RMON/MIB
- Interrupt generation to signal receive and transmit completion
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- External address matching of received frames
- Physical layer management through MDIO interface
- Supports serial network interface operation
- Half duplex flow control by forcing collisions on incoming frames
- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Wake on LAN support
- Jumbo frames of up to 10240 bytes supported
- Configurable Endianess for the DMA Interface (AHB Master)

2.17 MII Ethernet controller

SPEAr310 provides an Ethernet MAC 10/100 Universal (commonly referred to as GMAC-UNIV), enabling to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard.

Note: GMAC is a hardware block implementing Ethernet MAC layer 2 processing. GMAC is configured for 10/100 Mbps operation on SPEAr3xx family and up to 1 Gbps on SPEAr600.

Main features:

- Supports the default Media Independent Interface (MII) defined in the IEEE 802.3 specifications.
- Supports 10/100 Mbps data transfer rates
- Local FIFO available (4 Kbyte RX, 2 Kbyte TX)
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided
- Programmable frame length to support both standard and jumbo Ethernet frames with size up to 16 Kbyte
- A variety of flexible address filtering modes are supported
- A set of control and status registers (CSRs) to control MAC core operation
- Native DMA with single-channel transmit and receive engines
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- An AHB slave acting as programming interface to access all CSRs, for both DMA and MAC core subsystems
- A 32-bit AHB master for data transfer to system memory
- It supports both big-endian and little-endian.

2.18 USB2 host controller

SPEAr310 has two fully independent USB 2.0 hosts. Each consists of 5 major blocks:

- EHCI capable of managing high-speed transfers (HS mode, 480 Mbps)
- OHCI that manages the full and the low speed transfers (12 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

Both hosts can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

One host controller at time can perform high speed transfer.

2.19 USB2 device controller

Main features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the 1.5 Mbps low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, configurable as different logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared among all the endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug (UPD) detects the connection of a cable.

2.20 Cryptographic co-processor (C3)

SPEAr310 has an embedded Channel Control Coprocessor (C3). C3 is a high-performance instruction driven DMA based co-processor. It executes instruction flows generated by the host processor. After it has been set-up by the host it runs in a completely autonomous way (DMA data in, data processing, DMA data out), until the completion of all the requested operations.

C3 has been used to accelerate the processing of cryptographic, security and network security applications. It can be used for other types of data intensive applications as well.

Hardware cryptographic co-processor features are listed below:

- Supported cryptographic algorithms:
  - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes.
  - Data encryption standard (DES) cipher in ECB and CBC modes.
  - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests.
- Instruction driven DMA based programmable engine.
- AHB master port for data access from/to system memory.
- AHB slave port for co-processor register accesses and initial engine-setup.
- The co-processor is fully autonomous (DMA input reading, cryptographic operation execution, DMA output writing) after being set up by the host processor.
- The co-processor executes programs written by the host in memory, it can execute an unlimited list of programs.
- The co-processor supports hardware chaining of cryptographic blocks for optimized execution of data-flow requiring multiple algorithms processing over the same set of data (for example encryption + hashing on the fly).

2.21 JPEG CODEC

SPEAr310 provides a JPEG CODEC with header processing (JPGC), able to decode (or encode) image data contained in the SPEAr310 RAM, from the JPEG (or MCU) format to the MCU (or JPEG) format.

Main features:

- Compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- Single-clock per pixel encoding/decoding
- Support for up to four channels of component color
- 8-bit/channel pixel depths
- Programmable quantization tables (up to four)
- Programmable Huffman tables (two AC and two DC)
- Programmable minimum coded unit (MCU)
- Configurable JPEG header processing
- Support for restart marker insertion
- Use of two DMA channels and of two 8 x 32-bits FIFO's (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the CODEC core.