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SPEAr320

Embedded MPU with ARM926 core, optimized for factory automation and consumer applications

Features

- ARM926EJ-S 333 MHz core
- High-performance 8-channel DMA
- Dynamic power-saving features
- Configurable peripheral functions on 102 shared I/Os.
- Memory:
  - 32 KB ROM and 8 KB internal SRAM
  - LPDDR-333/DDR2-666 external memory interface
  - SDIO/MMC card interface
  - Serial Flash memory interface (SMI)
  - Flexible static memory controller (FSMC) up to 16-bit data bus width, supporting NAND Flash
  - External memory interface (EMI) up to 16-bit data bus width, supporting NOR Flash and FPGAs
- Security
  - Cryptographic accelerator
- Connectivity
  - 2 x USB 2.0 Host
  - 1 x USB 2.0 Device
  - 2 x Fast Ethernet ports (for external MII/SMII PHY)
  - 2 x CAN interface
  - 3 x SSP Synchronous serial port (SPI, Microwire or TI protocol)
  - 2 x I^2C
  - 1 x fast IrDA interface
  - 3 x UART interface
  - 1 x standard parallel device port
- Peripherals supported
  - TFT/STN LCD controller (resolution up to 1024 x 768 and up to 24 bpp)
  - Touchscreen support

LFBGA289 (15 x 15 x 1.7 mm)

- Miscellaneous functions
  - Integrated real time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 Msps
  - 4 x PWM timers
  - JPEG CODEC accelerator
  - 6x 16-bit general purpose timers with programmable prescaler, 4 capture inputs
  - Up to 102 GPIOs with interrupt capability

Applications

The SPEAr320 embedded MPU is configurable for a range of industrial and consumer applications such as:

- Programmable logic controllers
- Factory automation
- Printers

Table 1. Device summary

Order code	Temp range, °C	Package	Packing
SPEAR320-2	-40 to 85	LFBGA289 (15x15 mm, pitch 0.8 mm)	Tray

Contents

List of tables

List of figures

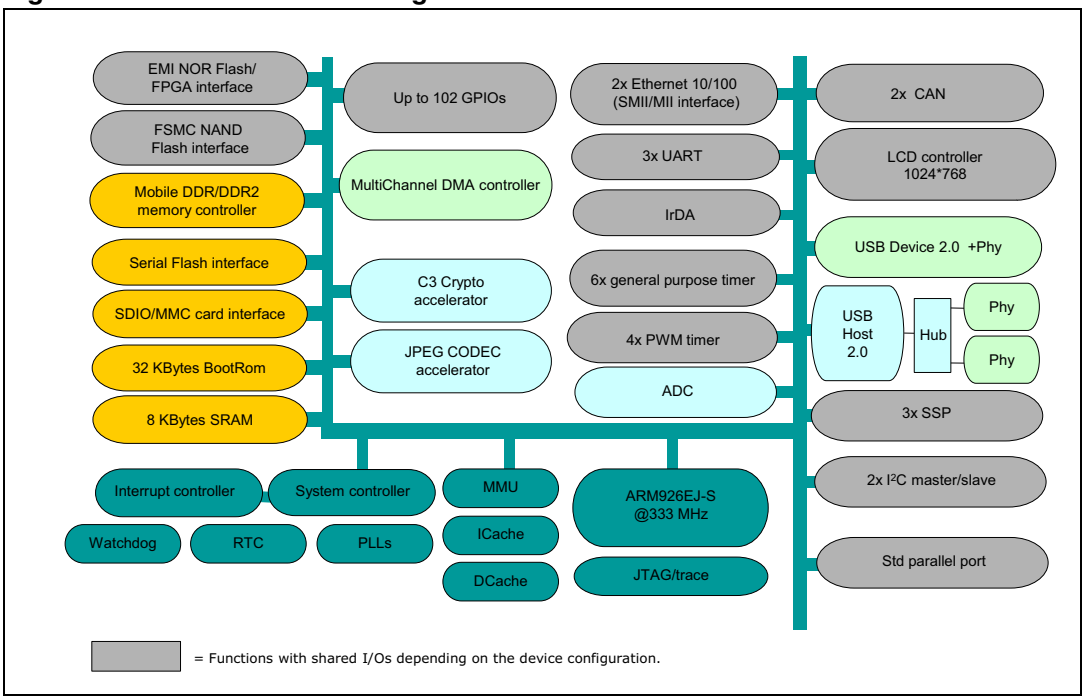
1 Description

The SPEAr320 is a member of the SPEAr family of embedded MPUs, optimized for industrial automation and consumer applications. It is based on the powerful ARM926EJ-S processor (up to 333 MHz), widely used in applications where high computation performance is required.

In addition, SPEAr320 has an MMU that allows virtual memory management - making the system compliant with Linux operating system. It also offers 16 KB of data cache, 16 KB of instruction cache, JTAG and ETM (Embedded Trace Macrocell™) for debug operations.

A full set of peripherals allows the system to be used in many applications, some typical applications being factory automation, printer and consumer applications.

Figure 1. Functional block diagram



2 Main features

- ARM926EJ-S 32-bit RISC CPU, up to 333 MHz
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, byte Java mode (Jazelle™) for direct execution of Java code.
  - Tightly Coupled Memory
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- External DRAM memory interface:
  - 8/16-bit (mobile DDR@166 MHz)
  - 8/16-bit (DDR2@333 MHz)
- Serial memory interface
- SDIO interface supporting SPI, SD1, SFD4 and SD8 modes
- 8/16-bits NAND Flash controller (FSMC)
- External memory interface (EMI) for connecting NOR Flash or FPGAs
- Boot capability from NAND Flash, serial/parallel NOR Flash
- Boot and field upgrade capability from USB
- High performance 8-channel DMA controller
- 3x Ethernet controllers (up to 2 operating concurrently)
- Two USB2.0 Host (high-full-low speed) with integrated PHY transceiver
- One USB2.0 Device (high-full-low speed) with integrated PHY transceiver
- 2x CAN 2.0 interfaces
- Up to 102 GPIOs with interrupt capability
- Up to 4 PWM outputs
- 3x SSP master/slave (supporting Motorola, Texas instruments, National semiconductor protocols) up to 41.5 Mbps
- Standard parallel port (SPP device implementation)
- 2 x I^2C master/slave interface (slow-fast-high speed, up to 1.2 Mb/s)
- 3x UART:
  - UART0 (up to 3 Mbps) with hardware flow control and modem interface
  - UART1 (up to 7 Mbps) with hardware flow control (in some operating modes)
  - UART2 (up to 7 Mbps) with software flow control
- ADC 10-bit, 1 Msps 8 inputs
- JPEG CODEC accelerator 1 clock/pixel
- Color LCD interface (up to 1024X768, 24-bits CLCD controller, TFT and STN panels)
- Touchscreen support
- Crypto accelerator (DES/3DES/AES/SHA1)

- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes CPU clock with software-programmable frequency
  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bit general purpose timers with programmable prescaler
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1 boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x 15 mm, pitch 0.8 mm)

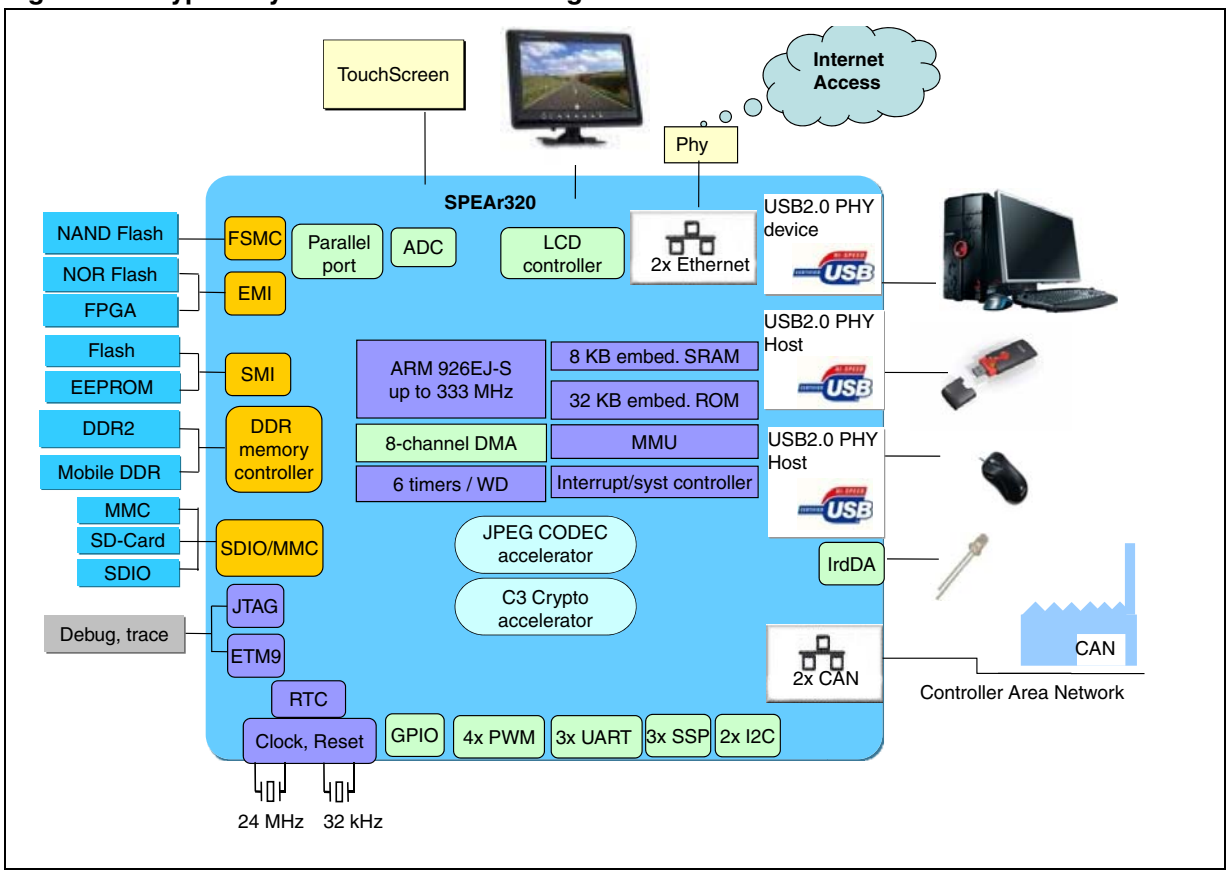
3 Architecture overview

The SPEAr320 internal architecture is based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix.

The switch matrix structure allows different subsystem dataflow to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

Figure 2. Typical system architecture using SPEAr320



3.1 CPU ARM 926EJ-S

The core of the SPEAr320 is an ARM926EJ-S reduced instruction set computer (RISC) processor.

It supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

The ARM CPU and is clocked at a frequency up to 333 MHz. It has a 16-Kbyte instruction cache, a 16-Kbyte data cache, and features a memory management unit (MMU) which makes it fully compliant with Linux and VxWorks operating systems.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

3.2 Embedded memory units

- 32 Kbytes of BootROM
- 8 Kbytes of SRAM

3.2.1 BootROM

BootROM is small firmware program that is executed just after the SPEAr320 exits from reset.

It supports the following boot modes:

- Boot from NOR serial Flash
- Boot from NAND Flash
- Boot from NOR parallel Flash
- Boot / Upgrade from USB

The first three modes support different ways of booting the application software, they require a second-level boot software (Xloader) to be located in Flash.

USB boot mode can be used for software maintenance or upgrade, if booting from any of the Flash memories is not possible.

The BootROM selects the boot mode from the boot pin settings (see *Section 4.3.4: Boot pins*). A setting is available to allow the BootROM to be bypassed.

3.3 Mobile DDR/DDR2 memory controller

SPEAr320 integrates a high performance multi-channel memory controller able to support low power Mobile DDR and DDR2 double data rate memory devices. The multi-port architecture ensures memory is shared efficiently among different high-bandwidth client modules.

It has 6 internal ports. One of them is reserved for register access during the controller initialization while the other five are used to access the external memory.

It also includes the physical layer (PHY) and DLLs for fine tuning the timing parameters to maximize the data valid windows at different frequencies.

3.4 Serial memory interface

SPEAr320 provides a serial memory interface (SMI), acting as an AHB slave interface (32-, 16- or 8-bit) to SPI-compatible off-chip memories.

These serial memories can be used either as data storage or for code execution.

Main features:

- Supports SPI-compatible Flash and EEPROM devices
- Acts always as a SPI master and up to 2 SPI slave memory devices are supported (with separate chip select signals), with up to 16 MB address space each
- SMI clock signal (SMICLK) is generated by SMI (and input to all slaves) using a clock provided by the AHB bus
- SMICLK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by a programmable 7-bit prescaler allowing up to 127 different clock frequencies.

3.5 External memory interface (EMI)

The EMI Controller provides a simple external memory interface that can be used for example to connect to NOR Flash memory or FPGA devices.

Main features:

- EMI bus master
- 16 and 8-bit transfers
- Can access 4 different peripherals using CS#, one at a time.
- Supports single asynchronous transfers.
- Supports peripherals which use Byte Lane procedure

3.6 SDIO controller/MMC card interface

The SDIO host controller conforms to the SD host Controller Standard Specification Version 2.0. It handles SDIO/SD Protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit and checking for transaction format correctness. The host controller provides programmed I/O and DMA data transfer method.

Main features:

- Meets the following specifications:
  - SD Host Controller Standard Specification Version 2.0
  - SDIO card specification version 2.0
  - SD Memory Card Specification Draft version 2.0
  - SD Memory Card Security Specification version 1.01
  - MMC Specification version 3.31 and 4.2
- Supports both DMA and Non-DMA mode of operation
- Supports MMC Plus and MMC Mobile
- Card Detection (Insertion / Removal)
- Card password protection
- Host clock rate variable between 0 and 48 MHz
- Supports 1 bit, 4 bit and 8 bit SD modes and SPI mode
- Supports Multi Media Card Interrupt mode
- Allows card to interrupt host in 1 bit, 4 bit, 8 bit SD modes and SPI mode.
- Up to 100 Mbits per second data rate using 4 parallel data lines (SD4 bit mode)

- Up to 416 Mbits per second data rate using 8 bit parallel data lines (SD8 bit mode)
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
- Designed to work with I/O cards, Read-only cards and Read/Write cards
- Error Correction Code (ECC) support for MMC4.2 cards
- Supports Read wait Control, Suspend/Resume operation
- Supports FIFO Overrun and Underrun condition by stopping SD clock

3.7 Flexible static memory controller (FSMC)

SPEAr320 provides a Flexible Static Memory Controller (FSMC) which interfaces to external parallel NAND Flash memories.

Main features:

- 8/16-bit wide data path
- FSMC performs only one access at a time and only one external device is accessed
- Supports little-endian and big-endian memory architectures
- AHB burst transfer handling to reduce access time to external devices
- Supplies an independent configuration for each memory bank
- Programmable timings to support a wide range of devices
  - Programmable wait states (up to 31)
  - Programmable bus turnaround cycles (up to 15)
  - Programmable output enable and write enable delays (up to 15)
- Independent chip select control for each memory bank
- Shares the address bus and the data bus with all the external peripherals
- Only chips selects are unique for each peripheral
- External asynchronous wait control
- Boot memory bank configurable at reset using external control pins

3.8 Multichannel DMA controller

Within its basic subsystem, SPEAr320 provides a DMA controller (DMAC) able to service up to 8 independent DMA channels for serial data transfers between single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).

Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

3.9 Ethernet controllers

SPEAr320 features three multiplexed Ethernet MACs, supporting up to two ports concurrently.

The three controllers are named:

- MII0
- SMII0
- SMII1/MII1

Table 2. Ethernet port multiplexing

Configuration mode (see *Section 4.3.2: Configuration modes*)	Available interfaces	Interface name
Mode 1 or Mode 4	2 x SMII	SMII0 + SMII1
Mode 1 or Mode 4 with MII0 alternate I/O functions enabled	1 x SMII + 1 x MII	SMII0+ MII0
Mode 2 with MII0 alternate I/O functions enabled	2 x MII	MII1 + MII0
Mode 3	1 x SMII	SMII0
Mode 3 with MII0 alternate I/O functions enabled	1 x MII	MII0

3.9.1 MII0 Ethernet controller

Main features:

- Supports the default Media Independent Interface (MII) defined in the IEEE 802.3 specifications.
- Supports 10/100 Mbps data transfer rates
- Local FIFO available (4 Kbyte RX, 2 Kbyte TX)
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided
- Programmable frame length to support both standard and jumbo Ethernet frames with size up to 16 Kbytes
- 32/64/128-bit data transfer interface on system-side.
- A variety of flexible address filtering modes are supported
- A set of control and status registers (CSRs) to control GMAC core operation
- Native DMA with single-channel transmit and receive engines, providing 32/64/128-bit data transfers
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- An AHB slave acting as programming interface to access all CSRs, for both DMA and GMAC core subsystems
- An AHB master for data transfer to system memory
- 32-bit AHB master bus width, supporting 32, 64, and 128-bit wide data transactions
- It supports both big-endian and little-endian.

3.9.2 SMII0/SMII1/MII1 Ethernet controllers

The two Ethernet controllers called SMII0 and SMII1/MII1 each have dedicated TX/RX signals while synchronization and clock signals are common for PHY connection.

Each of the two ports provides the following features:

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full and half duplex operation
- Statistics counter registers for RMON/MIB
- Interrupt generation to signal receive and transmit completion
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory

- Hash matching of unicast and multicast destination addresses
- External address matching of received frames
- Physical layer management through MDIO interface
- Supports serial network interface operation
- Half duplex flow control by forcing collisions on incoming frames
- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Wake on LAN support
- Jumbo frames of up to 10240 bytes supported
- Configurable Endianess for the DMA Interface (AHB Master)

3.10 CAN controller

SPEAr320 has two CAN controllers for interfacing CAN 2.0 networks.

Main features:

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 16 message objects(136 X 16 message RAM)
- Each message object has its own identifier mask
- Maskable interrupt
- Programmable loop-back mode for self-test operation
- Disabled automatic retransmission mode for time triggered CAN applications

3.11 USB2 Host controller

SPEAr320 has two fully independent USB 2.0 Hosts. Each consists of 5 major blocks:

- EHCI capable of managing high-speed transfers (HS mode, 480 Mbps)
- OHCI that manages the full and the low speed transfers (12 and 1.5 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

Both Hosts can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

One Host controller at time can perform high speed transfer.

3.12 USB2 Device controller

Main features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, configurable as different logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared among all the endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug (UPD) detects the connection of a cable.

3.13 CLCD controller

SPEAr320 has a color liquid crystal display controller (CLCDC) that provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

Main features:

- Resolution programmable up to 1024 x 768
- 16-bpp true-color non-palletized, for color STN and TFT
- 24-bpp true-color non-palletized, for color TFT
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palletized displays for mono STN
- 1, 2, 4 or 8-bpp palletized color displays for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little and big-endian

3.14 GPIOs

A maximum of 102 GPIOs (PL_GPIOs) are available when part of the embedded IPs are not needed (see *Section 4.3: Shared I/O pins (PL_GPIOs)*).

Within its basic subsystem, SPEAr320 provides a base General Purpose Input/Output (GPIO) block (basGPIO). The base GPIO block provides 6 programmable inputs or outputs. Each input/output can be controlled in two distinct modes:

- Software mode, through an APB interface.
- Hardware mode, through a hardware control interface.

Main features of the base GPIO block are:

- Six individually programmable input/output pins (default to input at reset)
- An APB slave acting as control interface in "software mode"
- Programmable interrupt generation capability on any number of pins.
- Hardware control capability of GPIO lines for different system configurations.
- Bit masking in both read and write operation through address lines.

Other GPIO blocks are present in the reconfigurable array subsystem.

3.15 Parallel port

Main features:

- Slave mode device interface for standard parallel port host
- Supports unidirectional 8-bit data transfer from host to slave
- Supports 9th bit for parity/data/command etc.
- Maskable interrupts for data, device reset, auto line feed
- APB input clock frequency required is 83 MHz for acknowledgement timings

3.16 Synchronous serial ports (SSP)

SPEAr320 provides three synchronous serial ports (SSP) that offer a master or slave interface to enable synchronous serial communication with slave or master peripherals

Main features:

- Master or slave operation.
- Programmable clock bit rate and prescale.
- Separate transmit and receive first-in, first-out memory buffers, 16-bits wide, 8 locations deep.
- Programmable choice of interface operation:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - TI synchronous serial.
- Programmable data frame size from 4 to 16-bits.
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts.
- Internal loopback test mode available.
- DMA interface

3.17 I2C

The SPEAr320 has 2 I2C interfaces:

Main features:

- Compliance to the I^2C bus specification (Philips)
- Supports three modes:
  - Standard (100 kbps)
  - Fast (400 kbps)
  - High-speed
- Clock synchronization
- Master and slave mode configuration possible
- Multi-master mode (bus arbitration)
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers

- Slave bulk transfer mode
- Ignores CBUS addresses (predessor to I2C that used to share the I2C bus)
- Transmit and receive buffers
- Interrupt or polled-mode operation
- Handles bit and byte waiting at all bus speeds
- Digital filter for the received SDA and SCL lines
- Handles component parameters for configurable software driver support
- Supports APB data bus widths of 8, 16 and 32 bits.

3.18 UARTs

The SPEAr320 has 3 UARTs with different capabilities.

3.18.1 UART0

Main features:

- Separate 16 x 8 (16 locations deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps
- Hardware and/or software flow control
- Modem interface signals

3.18.2 UART1

Main features:

- Separate 16 x 8 (16 location deep x 8-bit wide) transmit and 16x12 receive FIFOs to reduce CPU interrupts
- Speed up to 7 Mbps
- Hardware flow control (in Small Printers and Automation Expansion modes only) and/or software flow control

3.18.3 UART2

Main features:

- Separate 16x8 (16 location deep x 8-bit wide) transmit and 16x12 receive FIFOs to reduce CPU interrupts
- Speed up to 7 Mbps
- Software flow control

3.19 JPEG CODEC

SPEAr320 provides a JPEG CODEC with header processing (JPGC), able to decode (or encode) image data contained in the SPEAr320 RAM, from the JPEG (or MCU) format to the MCU (or JPEG) format.

Main features:

- Compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- Single-clock per pixel encoding/decoding
- Support for up to four channels of component color
- 8-bit/channel pixel depths
- Programmable quantization tables (up to four)
- Programmable Huffman tables (two AC and two DC)
- Programmable minimum coded unit (MCU)
- Configurable JPEG header processing
- Support for restart marker insertion
- Use of two DMA channels and of two 8 x 32-bits FIFO's (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the CODEC core.

3.20 Cryptographic co-processor (C3)

SPEAr320 has an embedded Channel Control Coprocessor (C3). C3 is a high-performance instruction driven DMA based co-processor. It executes instruction flows generated by the host processor. After it has been set-up by the host it runs in a completely autonomous way (DMA data in, data processing, DMA data out), until the completion of all the requested operations.

C3 has been used to accelerate the processing of cryptographic, security and network security applications. It can be used for other types of data intensive applications as well.

Main features:

- Supported cryptographic algorithms:
  - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes.
  - Data encryption standard (DES) cipher in ECB and CBC modes.
  - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests.
- Instruction driven DMA based programmable engine.
- AHB master port for data access from/to system memory.
- AHB slave port for co-processor register accesses and initial engine-setup.
- The co-processor is fully autonomous (DMA input reading, cryptographic operation execution, DMA output writing) after being set up by the host processor.
- The co-processor executes programs written by the host in memory, it can execute an unlimited list of programs.
- The co-processor supports hardware chaining of cryptographic blocks for optimized execution of data-flow requiring multiple algorithms processing over the same set of data (for example encryption + hashing on the fly).

3.21 8-channel ADC

Main features:

- Successive approximation conversion method
- 10-bit resolution @1 Msps
- Hardware supporting up to 13.5 bits resolution at 8 ksps by oversampling and accumulation
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- INL ± 1 LSB, DNL ± 1 LSB
- Programmable conversion speed, (min. conversion time is 1 µs)
- Programmable averaging of results from 1 (No averaging) up to 128
- Programmable auto scan for all the eight channels.

3.22 System controller

The System Controller provides an interface for controlling the operation of the overall system.

Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable

3.22.1 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr320 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode**: In this mode the system clocks, HCLK and CLK, are disabled and the System Controller clock SCLK is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.
- **DOZE mode**: In this mode the system clocks, HCLK and CLK, and the System Controller clock SCLK are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

3.22.2 Clock and reset system

The clock system is a fully programmable block that generates all the clocks necessary to the chip.

The default operating clock frequencies are:

- Clock @ 333 MHz for the CPU.
- Clock @ 166 MHz for AHB bus and AHB peripherals.
- Clock @ 83 MHz for, APB bus and APB peripherals.
- Clock @ 333 MHz for DDR memory interface.

The default values give the maximum allowed clock frequencies. The clock frequencies are fully programmable through dedicated registers.

The clock system consists of 2 main parts: a multi clock generator block and two internal PLLs.

The multi clock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr320 according to dedicated programmable registers.

Each PLL uses an oscillator input of 24 MHz to generate a clock signal at a frequency corresponding at the highest of the group. This is the reference signal used by the multi clock generator block to obtain all the other requested clocks for the group. Its main feature is electromagnetic interference reduction capability.

The user can set up the PLL in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

In sleep mode the SPEAr320 runs with the PLL disabled so the available frequency is 24 MHz or a sub-multiple (/2, /4, /8).

3.23 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

3.24 General purpose timers

SPEAr320 provides 6 general purpose timers (GPTs) acting as APB slaves.

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through configuration registers (a frequency range from 3.96 Hz to 48 MHz can be synthesized).

Two different modes of operation are available :

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

3.25 PWM timers

SPEAr320 provides 4 PWM timers.

Main features:

- Prescaler to define the input clock frequency to each timer
- Programmable duty cycle from 0% to 100%
- Programmable pulse length
- APB slave interface for register programming

3.26 Watchdog timer

The ARM watchdog module consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

3.27 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

Main features:

- Time-of-day clock in 24 hour mode
- Calendar
- Alarm capability
- Isolation mode, allowing RTC to work even if power is not supplied to the rest of the device.