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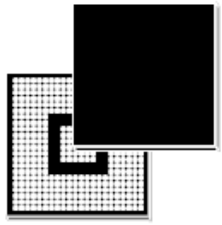
SPEAr600

Embedded MPU with dual ARM926 core, flexible memory support, powerful connectivity features and programmable LCD interface

Datasheet – production data

Features

- Dual ARM926EJ-S core up to 333 MHz:
  - Each with 16 Kbytes instruction cache + 16 Kbytes data cache
- High performance 8-channel DMA
- Dynamic power saving features
- Up to 733 DMIPS
- Memory:
  - External DRAM interface: 8/16-bit DDR1-333 / DDR2 - 666
  - 32 Kbytes BootROM / 8 Kbytes internal SRAM
  - Flexible static memory controller (FSMC) supporting parallel NAND Flash memory interface, ONFI 1.0 support, internal 1-bit ECC or external 4-bit ECC
  - Serial NOR Flash Memory interface
- Connectivity:
  - 2 x USB 2.0 Host
  - USB 2.0 Device
  - Giga Ethernet (GMII port)
  - I^2C and fast IrDA interfaces
  - 3 x SSP Synchronous serial peripheral (SPI, Microwire or TI protocol) ports
  - 2 x UART interfaces
- Peripherals supported:
  - TFT/STN LCD controller (resolution up to 1024 x 768 and colors up to 24 bpp)
  - Touchscreen support
- Miscellaneous functions
  - Integrated real-time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 Msps
  - JPEG codec accelerator
  - 10 GPIO bidirectional signals with interrupt capability
  - 10 independent 16-bit timers with programmable prescaler
- 32-bit width External local bus (EXPI interface).



PBGA420 (23 x 23 x 2.06 mm)

- 3 x I^2S interfaces for audio features:
  - One stereo input and two stereo outputs (audio 3.1 configuration capable)
- Customizable logic with 600 Kgate standard cell array
- Software:
  - System compliant with all operating systems (including Linux)

Applications

- The SPEAr® embedded MPU family targets networked devices used for communication, display and control. This includes diverse consumer, business, industrial and life science applications such as:
  - IP phones, thin client computers, printers, programmable logic controllers, PC docking stations,
  - Medical lab/diagnostics equipment, wireless access devices, home appliances, residential control and security systems, digital picture frames, and bar-code scanners/readers.

Table 1. Device summary

Order code	Temp. range	Package	Packing
SPEAR600-2	-40 to 85 °C	PBGA420 (23 x 23 x 2.06 mm)	Tray

Contents

1 Description 8

1.1 Main features 9

2 Architecture overview 11

2.1 Embedded memory units 13

2.2 DDR/DDR2 memory controller 13

2.3 Serial memory interface 13

2.4 Flexible static memory controller 14

2.5 Multichannel DMA controller 15

2.6 LCD controller 15

2.7 GPIOs 15

2.8 JPEG codec 16

2.9 8-channel ADC 16

2.10 Ethernet controller 16

2.11 USB2 host controller 17

2.12 USB2 device controller 17

2.13 Synchronous Serial Peripheral (SSP) 18

2.14 I2C 18

2.15 UARTs 18

2.16 Fast IrDA controller 19

2.17 I^2S audio block 19

2.18 System controller 19

2.18.1 Power saving system mode control 20

2.19 Clock and reset system 20

2.20 Vectored interrupt controller (VIC) 21

2.21 General purpose timers 21

2.22 Watchdog timer 22

2.23 RTC oscillator 22

2.24 Reconfigurable array subsystem connectivity (RAS) 22

2.25 External Port Controller (EXPI I/F) 23

3 Pin description 24

3.1 Required external components 24

3.2 Pin descriptions listed by functional block 24

3.3 Configuration modes 41

3.3.1 Full features 41

3.3.2 Disable NAND Flash 41

3.3.3 Disable LCD ctr 41

3.3.4 Disable GMAC ctr 42

3.3.5 Self cfg_4 42

3.3.6 Self cfg_5 42

3.3.7 All processors disabled 42

4 Memory map 53

5 Electrical characteristics 55

5.1 Absolute maximum ratings 55

5.2 Maximum power consumption 55

5.3 DC electrical characteristics 56

5.4 Overshoot and undershoot 56

5.5 3.3V I/O characteristics 57

5.6 DDR2 pin characteristics 57

5.7 Power up sequence 58

5.8 Power on reset (MRESET) 58

5.9 ADC electrical parameters 59

6 Timing characteristics 60

6.1 DDR2 timing characteristics 60

6.1.1 DDR2 read cycle timings 60

6.1.2 DDR2 write cycle timings 61

6.1.3 DDR2 command timings 63

6.2 EXPI timing characteristics 65

6.2.1 Pad delay disabled 66

6.2.2 Pad delay enabled 68

6.3 CLCD timing characteristics 71

6.3.1 CLCD timing characteristics direct clock 71

6.3.2 CLCD timing characteristics divided clock 72
6.4 I2C timing characteristics 73
6.5 FSMC timing characteristics 76
6.5.1 8-bit NAND Flash configuration 76
6.5.2 16-bit NAND Flash configuration 78
6.6 Ether MAC 10/100/1000 Mbps (GMAC-Univ) timing characteristics 80
6.6.1 GMII Transmit timing specifications 80
6.6.2 MII transmit timing specifications 81
6.6.3 GMII-MII Receive timing specifications 82
6.6.4 MDIO timing specifications 83
6.7 SMI timing characteristics 84
6.7.1 SMI timing specifications 84
6.8 SSP timing characteristics 86
6.8.1 SPI master mode timings (CPHA = 0) 87
6.8.2 SPI master mode timings (CPHA = 1) 88

7 Package information 90
7.1 Package mechanical data 91

8 Revision history 94

List of tables

Table 1. Device summary . . . 1
Table 2. System reset, master clock, RTC and configuration pins . . . 24
Table 3. Power supply pins . . . 25
Table 4. Debug pins . . . 27
Table 5. SMI, SSP, UART, FIRDA and I2C pins . . . 27
Table 6. USB pins . . . 29
Table 7. Ethernet pins . . . 30
Table 8. GPIO pins . . . 31
Table 9. ADC pins . . . 31
Table 10. NAND Flash I/F pins . . . 32
Table 11. DDR I/F pins . . . 33
Table 12. LCD I/F pins . . . 35
Table 13. LVDS I/F pins . . . 36
Table 14. EXPI/I2S pins . . . 37
Table 15. EXPI pins . . . 38
Table 16. Multiplexing scheme . . . 43
Table 17. Table shading . . . 52
Table 18. Memory map . . . 53
Table 19. Absolute maximum ratings . . . 55
Table 20. Maximum current and power consumption . . . 55
Table 21. Recommended operating conditions . . . 56
Table 22. Overshoot and undershoot specifications . . . 56
Table 23. Low voltage TTL DC input specification (3 V< V_{DD} <3.6 V) . . . 57
Table 24. Low voltage TTL DC output specification (3 V< V_{DD} <3.6 V) . . . 57
Table 25. Pull-up and pull-down characteristics . . . 57
Table 26. DC characteristics . . . 57
Table 27. Driver characteristics . . . 57
Table 28. On die termination . . . 58
Table 29. Reference voltage . . . 58
Table 30. ADC characteristics . . . 59
Table 31. DDR2 read cycle path timings without pad delay . . . 60
Table 32. DDR2 read cycle timings without pad delay . . . 60
Table 33. DDR2 write cycle path timings without pad delay . . . 62
Table 34. DDR2 write cycle timings without pad delay . . . 62
Table 35. DDR2 command timings without pad delay . . . 64
Table 36. EXPI - pad signal assignment . . . 65
Table 37. EXPI clock and reset parameters . . . 67
Table 38. SOC-master . . . 67
Table 39. SOC-slave . . . 67
Table 40. Clock and Reset . . . 69
Table 41. SOC-master . . . 69
Table 42. SOC-slave . . . 69
Table 43. CLCD timings with CLCP direct . . . 71
Table 44. CLCD timings with CLCP divided . . . 72
Table 45. Timing characteristics for I^2C in high-speed mode . . . 74
Table 46. Timing characteristics for I^2C in fast-speed mode . . . 74
Table 47. Timing characteristics for I^2C in standard-speed mode . . . 74
Table 48. Timing characteristics for 8-bit NAND Flash configuration . . . 77

Table 49. Timing characteristics for 16-bit NAND Flash configuration 79
Table 50. GMII TX timing 80
Table 51. MII TX timings 81
Table 52. GMII-MII RX timings 82
Table 53. MDC/MDIO timing 83
Table 54. SMI timings in default configuration 84
Table 55. SMI Timings of SMI_CS_3 in non-default configurations 85
Table 56. Timing requirements for SSP (all modes) 86
Table 57. Timing requirements for SPI mode on MISO pad [CPHA = 0] 87
Table 58. Timing requirements for SPI mode on MOSI pad [CPHA = 0] 87
Table 59. Timing requirements for SPI mode on MISO pad [CPHA = 1] 88
Table 60. Timing requirements for SPI mode on MOSI pad [CPHA = 1] 89
Table 61. PBGA420 (23 x 23 x 2.06 mm) mechanical data 91
Table 62. SPEAr600 **PBGA420** thermal resistance characteristics 93
Table 63. Document revision history 94

List of figures

Figure 1. Functional block diagram . . . 8
Figure 2. Typical system architecture using SPEAr600 . . . 11
Figure 3. Power on reset timing diagram . . . 58
Figure 4. DDR2 read cycle waveforms . . . 60
Figure 5. DDR2 read cycle path . . . 60
Figure 6. DDR2 write cycle waveforms . . . 61
Figure 7. DDR2 write cycle path . . . 62
Figure 8. DDR2 command waveforms . . . 63
Figure 9. DDR2 command path . . . 63
Figure 10. AHB EXPI transfer waveforms . . . 65
Figure 11. Pad delay disabled block diagram . . . 66
Figure 12. EXPI signal timing waveforms . . . 67
Figure 13. EXPI pad delay enabled block diagram . . . 68
Figure 14. EXPI signal timing waveforms . . . 69
Figure 15. CLCD waveform with CLCP direct . . . 71
Figure 16. CLCD block diagram with CLCP direct . . . 71
Figure 17. CLCD waveform with CLCP divided . . . 72
Figure 18. CLCD block diagram with CLCP divided . . . 72
Figure 19. I^2C output pads . . . 73
Figure 20. I^2C input pads . . . 73
Figure 21. Output signal waveforms for I^2C signals . . . 74
Figure 22. RC delay circuit . . . 75
Figure 23. Output pads for 8-bit NAND Flash configuration . . . 76
Figure 24. Input pads for 8-bit NAND Flash configuration . . . 76
Figure 25. Output command signal waveforms for 8-bit NAND Flash configuration . . . 76
Figure 26. Output address signal waveforms for 8-bit NAND Flash configuration . . . 77
Figure 27. In/out data address signal waveforms for 8-bit NAND Flash configuration . . . 77
Figure 28. Output pads for 16-bit NAND Flash configuration . . . 78
Figure 29. Input pads for 16-bit NAND Flash configuration . . . 78
Figure 30. Output command signal waveforms 16-bit NAND Flash configuration . . . 78
Figure 31. Output address signal waveforms 16-bit NAND Flash configuration . . . 79
Figure 32. In/out data signal waveforms for 16-bit NAND Flash configuration . . . 79
Figure 33. GMII TX waveforms . . . 80
Figure 34. Block diagram of GMII TX pins . . . 80
Figure 35. MII TX waveforms . . . 81
Figure 36. Block diagram of MII TX pins . . . 81
Figure 37. GMII-MII RX waveforms . . . 82
Figure 38. Block diagram of GMII-MII RX pins . . . 82
Figure 39. MDC waveforms . . . 83
Figure 40. Paths from MDC/MDIO pads . . . 83
Figure 41. SMI waveforms . . . 84
Figure 42. Block diagram of the SMI pins . . . 84
Figure 43. SSP_CLK timing . . . 86
Figure 44. SPI master mode external timing (CPHA = 0) . . . 88
Figure 45. SPI master mode external timing (CPHA = 1) . . . 89
Figure 46. PBGA420 (23 x 23 x 2.06 mm) package top view . . . 92
Figure 47. PBGA420 (23 x 23 x 2.06 mm) package bottom view . . . 93

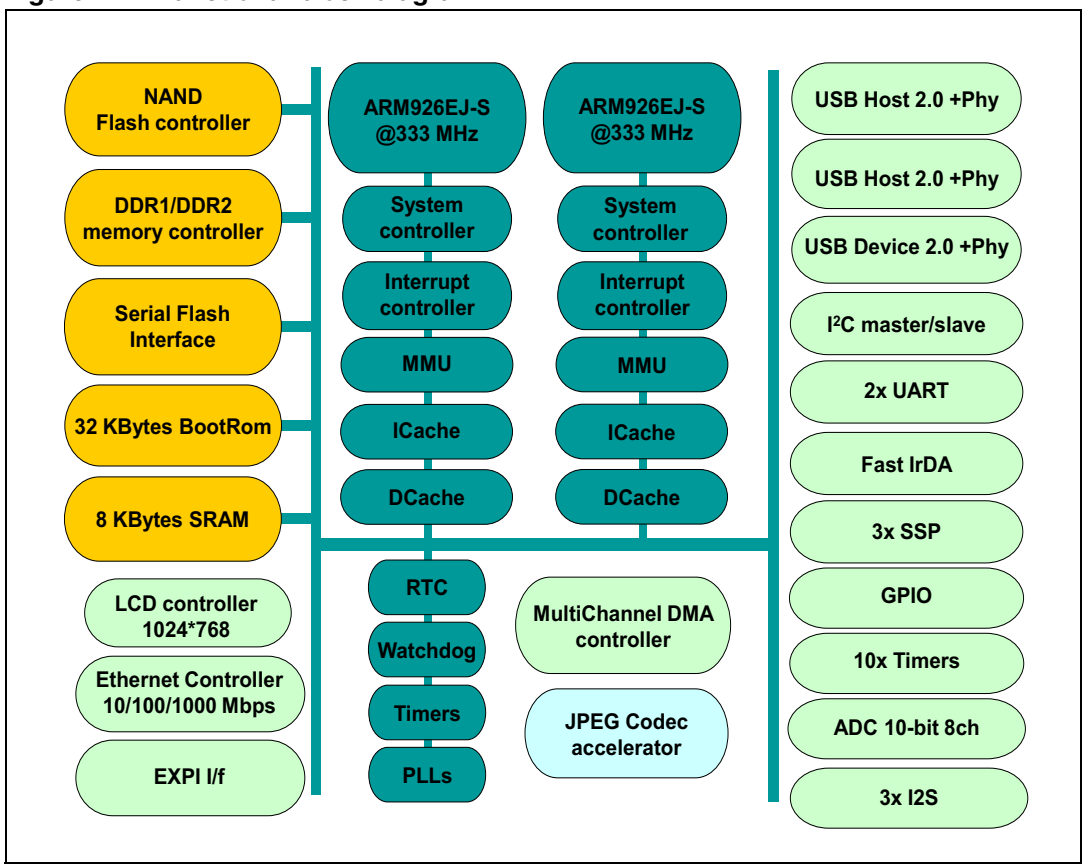
1 Description

The SPEAr600 is a member of the SPEAr family of embedded MPUs for networked devices, it is based on dual ARM926EJ-S processors (up to 333 MHz), widely used in applications where high computation performance is required.

Both processors have an MMU supporting virtual memory management and making the system compliant with the Linux operating system. They also offer 16 KBytes of data cache, 16 KBytes of instruction cache, JTAG and ETM (embedded trace macro-cell) for debug operations.

To expand its range of target applications, SPEAr600 can be extended by adding additional peripherals through the external local bus (EXPI interface).

Figure 1. Functional block diagram



1.1 Main features

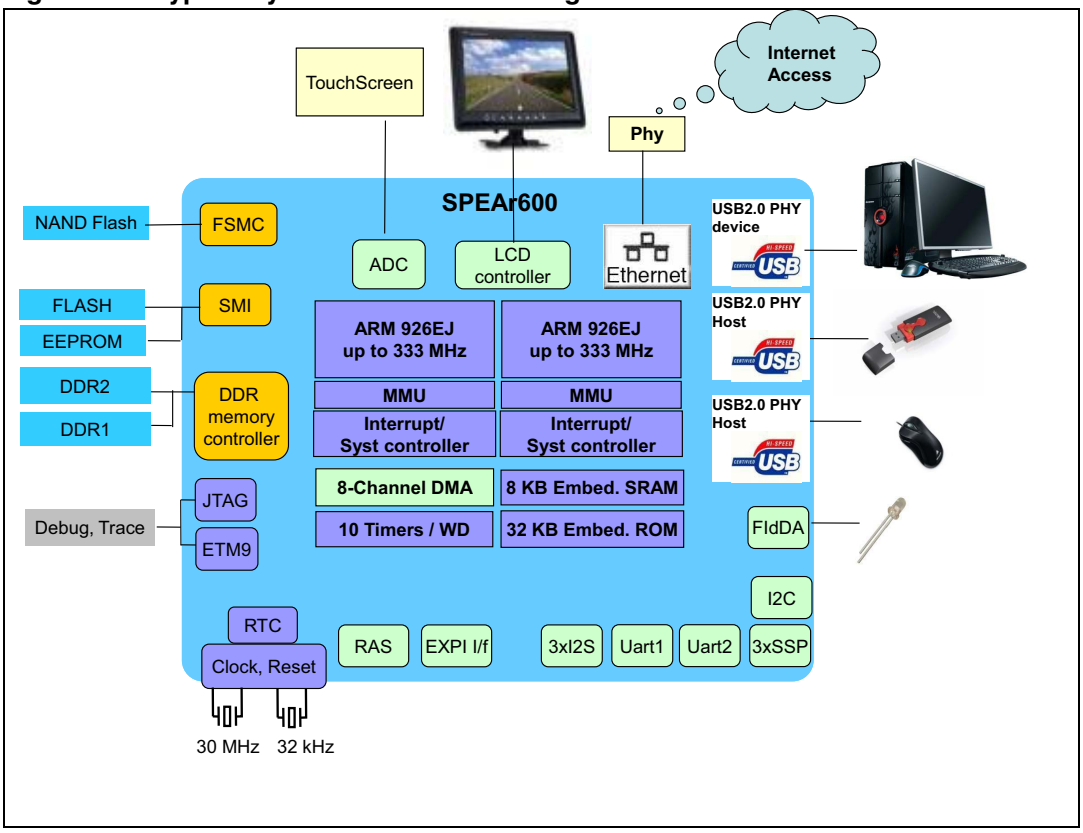
- Dual core ARM926EJ-S 32-bit RISC CPU, up to 333 MHz, each with:
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, byte Java mode (Jazelle™) for direct execution of Java code.
  - Tightly Coupled Memory
  - AMBA bus interface
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- Dynamic memory controller managing external DDR1 memory up to 166 MHz and external DDR2 memory up to 333 MHz
- Serial memory interface
- 8/16-bits NAND Flash controller
- Possible NAND Flash or serial NOR flash booting
- Multichannel DMA controller
- Color LCD Controller for STN/TFT display panels
  - Up to 1024 x 768 resolution
  - 24 bpp true color
- Ethernet GMAC 10/100/1000 Mbps (GMII/MII PHY interface)
- Two USB 2.0 host (high-full-low speed) with integrated PHY transceiver
- One USB 2.0 device (high-full speed) with integrated PHY transceiver
- 10 GPIO bidirectional signals with interrupt capability
- JPEG codec accelerator 1clock/pixel
- ADC 10-bit, 1 Msps 8 inputs/1-bit DAC
- 3 SSP master/slave (supporting Motorola, Texas instruments, National Semiconductor protocols) up to 40 Mbps
- I^2C master/slave interface (slow/ fast/high speed, up to 1.2 Mb/s)
- 10 independent 16-bit timers with programmable prescaler
- I/O peripherals
  - Two UARTs (speed rate up to 460.8 kbps)
  - Fast IrDA (FIR/MIR/SIR) 9.6 Kbps to 4 Mbps speed-rate
- Audio block with 3-I2Ss interfaces to support Audio Play (Up to 3.1) and Audio Record functionality.
- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes, CPU clock with software-programmable frequency
  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller

  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration.
- External local bus (EXPI I/f) that is an AMBA AHB like interface
- Programmable PLLs for CPU and system clocks
- JTAG IEEE 1149.1 boundary scan
- ETM functionality multiplexed on primary pins.
- Supply voltages
  - 1.0 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs 1.8 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- ESD rating: HBM class 2, CDM class II
- PBGA420 (23 x 23 x 2.06 mm, pitch 1 mm)

2 Architecture overview

Figure 2. shows an example of a typical SPEAr600 based system.

Figure 2. Typical system architecture using SPEAr600



The core of the SPEAr600 is the dual ARM926EJ-S reduced instruction set computer (RISC) processor.

It supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

Each ARM CPU:

- Is clocked at a frequency up to 333 MHz
- Embeds 16 Kbytes instruction cache + 16 Kbytes data cache
- Features a memory management unit (MMU) which makes it fully compliant with Linux and VxWorks operating systems.

The SoC includes three major subsystems logic domains which control the following function blocks:

Configurable Cell Array Subsystem

This block contains the Reconfigurable Array Subsystem logic (RAS) made by an array of 600Kgate equivalent standard cells freely customizable by means of a few metal and via mask layer changes during the customization process. The programmable logic allows reducing the SoC NRE cost, the development cycle time improving the devices time to

market. The user custom logic can be configured using the following SoC internal resources:

- 130 Kbyte of static memory arranged in four 32 KB macro group and one 2 KB group.
- Up to 17 selectable source clocks (either internal or external)
- DMA support (up to 16 configurable dma input/output request lines)
- Power management I/F
- Interrupts line (12 outputs - 64 inputs)
- 4 AHB output master ports interconnected with the multi-channel memory controller
- 5 AHB input slave ports
- 1 interconnection port with the Expansion Interface bus (EXPI)
- 9 LVDS (8 outputs - 1 input) signals
- 88/112 PL_GPIOs primary input/output signals

Caution: PL GPIO pins are not configurable by software.

Common Subsystem

This block consists of four different logic subsystems used to control the SoC basic functions:

- I/O connectivity:
  - Low speed: UARTs, SSPs, I2C and IrDA
  - High speed: MII 10/100/1000, USB 2.0 host and devices
- Hardware accelerator: JPEG-codec and DMA
- Video: Color LCD interface
- Common resources: Timers, GPIOs, RTC and Watchdog
- Power management functionality
- SoC configurability: Miscellaneous control logic

CPU Subsystem

The SPEAr600 has a symmetric processor architecture with:

- 2 equivalent subsystems including the ARM926 and its private subsystem logic (GPIOs, Interrupt controller and Timer) providing the essential hardware resources to support a generic Operating System
- The subsystem is replicated twice so both processors have the same memory map. This structure enables a true symmetric multi-processor architecture were both processors can simultaneously execute the same OS (all interrupt sources are handled by both processors)
- All internal peripherals are shared, allowing flexible and efficient software partitions.
- High aggregate throughput can be sustained by splitting critical tasks either onto additional CPUs and optional hardware accelerator engines.
- Both processors are equipped with ICE and ETM configurable debug interfaces. for real-time CPU activity tracing and debugging.
  4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode is supported, with normal or half-rate clock.

The internal architecture is also based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix. The switch matrix structure

allows different subsystem data flows to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

2.1 Embedded memory units

The SPEAr600 has two embedded memory units

- 32 Kbytes of BootROM
- 8 Kbytes of SRAM

2.2 DDR/DDR2 memory controller

SPEAr600 integrates a high performance multi-channel memory controller able to support DDR1 and DDR2 double data rate memory devices. The multi-port architecture ensures that memory is shared efficiently among different high-bandwidth client modules.

Main features:

- Multi channel AHB interfaces:
  - Seven independent AHB ports
  - Separate AHB memory controller programming interface
  - Support all AHB burst types
  - Lock transaction are not supported
- Internal efficient port arbitration scheme to ensure high memory bandwidth utilization
- Programmable register interface to control memory device parameters and protocols
- DRAM controller supports both DDR1 and DDR2 memory devices:
  - DDR1 up to 166 MHz
  - DDR2 up to 333 MHz
- Memory frequency with DLL enable configurable from 100 MHz to 333 MHz
- Wide range of memory devices supported:
  - 128 Mbit, 256 Mbit, 512 Mbit, 1 Gbit, 2 Gbit
  - Two chip selects.
  - 8 or 16-bit data width

2.3 Serial memory interface

SPEAr600 provides a Serial Memory Interface (SMI), acting as an AHB slave interface (32-, 16- or 8-bit) to SPI-compatible off-chip memories.

These serial memories can be used either as data storage or for code execution.

Main features:

- Supports the following SPI-compatible Flash and EEPROM devices:
  - STMicroelectronics M25Pxxx, M45Pxxx
  - STMicroelectronics M95xxx, except M95040, M95020 and M95010
  - ATMEL AT25Fxx
  - YMC Y25Fxx
  - SST SST25LFxx
- Acts always as a SPI master and supports up to 3 SPI slave memory devices (with separate chip select signals), with up to 16 MB address space each
- SMI clock (SMICLK) is generated by SMI (and input to all slaves) using a clock provided by the AHB bus
- SMI_CLK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by 7 programmable bits.

2.4 Flexible static memory controller

Root part number 1 provides Flash Nand Static Memory Controller (FSMC) which is intended to interface an AHB bus to external NAND Flash memories.

Main purpose of FSMC is then:

- Translate AHB protocol into the appropriate external storage device protocol
- Meet the timing of the external devices, slowing down and counting an appropriate number of HCLK (AHB clock) cycles to complete the transaction to the external device

Note: The external storage device cannot be faster than one AHB cycle.

Main features of the FSMC are listed below:

- The FSMC is an AMBA slave module connected to the AHB
- Provides an interface between AHB system bus and Nand Flash memory devices with 8 and 16 bits wide data paths
- FSMC performs only one access at a time and only one external device is accessed
- Support little-endian and big-endian memory architectures
- Handles AHB burst transfers to reduce access time to external devices
- Supplies an independent configuration for each memory bank
- Provides programmable timings to support a wide range of devices:
  - Programmable wait states (up to 31)
  - Programmable bus turn around cycles (up to 15)
  - Programmable output enable and write enable delays (up to 15)
- Provides only one chip select for the first memory bank
- Shares the address bus and the data bus with all the external peripherals, whereas only chips selects are unique for each peripheral
- Offers an external asynchronous wait control
- Offers configurable size at reset for boot memory bank using external control pins.

2.5 Multichannel DMA controller

Within its basic subsystem, SPEAr600 provides a DMA controller (DMAC) able to service up to 8 independent DMA channels for serial data transfers between a single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to-memory, and peripheral-to-peripheral).

Each DMA channel can support unidirectional transfers, with one internal four-word FIFO per channel.

2.6 LCD controller

Main features:

- Resolution programmable up to 1024 x 768
- 16-bpp true-color non-palletized, for color STN and TFT
- 24-bpp true-color non-palletized, for color TFT
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palletized displays for mono STN
- 1, 2, 4 or 8-bpp palletized color displays for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little-endian, big-endian and WinCE data formats

2.7 GPIOs

The General Purpose Input/Outputs (GPIOs) provide programmable inputs or outputs.

Each input/output can be controlled in two distinct modes:

- Software mode, through an APB interface
- Hardware mode, through a hardware control interface.

SPEAr600 provides up to 10 GPIO lines:

- Individually programmable input/output pins (default to input at reset)
- An APB slave acting as control interface in "software mode"
- Programmable interrupt generation capability on any number of pins
- Bit masking in both read and write operations through address lines

2.8 JPEG codec

Main features:

- Compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- Single-clock per pixel encoding/decoding
- Support for up to four channels of component color
- 8-bit/channel pixel depths
- Programmable quantization tables (up to four)
- Programmable Huffman tables (two AC and two DC)
- Programmable minimum coded unit (MCU)
- Configurable JPEG headers processing
- Support for restart marker insertion
- Use of two DMA channels and of two 8 x 32-bits FIFOs (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the codec core.

2.9 8-channel ADC

Main features:

- Successive approximation ADC
- 10-bit resolution @1 Msps
- Hardware over sampling and accumulation up to 128 samples
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- INL ± 1 LSB, DNL ± 1 LSB
- Programmable conversion speed, (min. conversion time is 1 µs)
- Programmable averaging of results from 1 (No averaging) up to 128

2.10 Ethernet controller

Main features:

- Supports the default Gigabit Media Independent Interface (GMII)/Media Independent Interface (MII) defined in the IEEE 802.3 specifications.
- Supports 10/100/1000 Mbps data transfer rates with any one or a combination of the above PHY interfaces
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided for, as well as packet bursting and frame extension at 1000 Mbps
- Programmable frame length to support both Standard and Jumbo Ethernet frames with size up to 16 Kbytes
- 32-bit data transfer interface on system-side
- A variety of flexible address filtering modes are supported
- A set of control and status registers (CSRs) to control GMAC Core operation.
- Complete network statistics with RMON Counters (MMC, MAC Management Counters).

- Native DMA with single-channel Transmit and Receive engines, providing 32/64/128-bit data transfers
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- A set of CSRs to control DMA operation
- An AHB slave acting as programming interface to access all CSRs, for both DMA and GMAC core subsystems
- An AHB master for data transfer to system memory
- 32-bit AHB master bus width, supporting 32-bit wide data transactions
- Supports both big-endian and little-endian byte ordering
- Power Management Module (PMT) with Remote Wake-up and Magic Packet frame processing options

2.11 USB2 host controller

SPEAr600 has two fully independent USB 2.0 hosts. Each consists of 5 major blocks:

- EHCI capable of managing high-speed transfers (HS mode, 480 Mbps)
- OHCI that manages the full and the low speed transfers (12 and 1.5 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

Both hosts can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

Both host controllers can perform high speed transfer simultaneously.

2.12 USB2 device controller

Main features:

- Supports 480 Mbps high-speed mode (HS) for USB 2.0, as well as 12 Mbps full-speed (FS) and the low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, which can be assigned to different interfaces and configurations to implement logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared by all endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug detect (UPD) which detects the connection of a cable.

2.13 Synchronous Serial Peripheral (SSP)

The SPEAR600 has three Synchronous Serial Peripherals (SSPs) (SPI, Microwire or TI protocol).

Main features:

- Maximum speed of 40 Mbps
- Programmable choice of interface protocol:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - TI synchronous serial
- Programmable data frame size from 4 to 16-bit.
- Master and slave mode capability.
- DMA interface

2.14 I2C

Main features:

- Compliance to the I^2C bus specification (Philips)
- I^2C v2.0 compatible.
- Supports three modes:
  - Standard (100 kbps)
  - Fast (400 kbps)
  - High-speed (3.4 Mbps)
- Master and slave mode configuration possible
- Slave Bulk data transfer capability
- DMA interface

2.15 UARTs

The SPEAr600 has two UARTs.

Main features:

- Hardware flow control
- Separate 16x8 (16 locations deep x 8 bits wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps

2.16 Fast IrDA controller

The SPEAr600 has a Fast IrDA controller.

Main features:

- Supports the following standards:
  - IrDA serial infrared physical layer specification (IrPHY), version 1.3
  - IrDA link access protocol (IrLAP), version 1.1
- Supports the following infrared modes and baud rates:
  - Serial infrared (SIR), with rates 9.6 kbps, 19.2 kbps, 38.4 kbps, 57.6 kbps and 115.2 kbps
  - Medium Infrared (MIR), with rates 576 kbps and 1.152 Mbps
  - Fast Infrared (FIR), with rate 4 Mbps
- Transceiver interface compliant to all IrDA transceivers with configurable TX and RX signal polarity
- Half-duplex infrared frame transmission and reception
- 16-bit CRC algorithm for SIR and MIR, and 32-bit CRC algorithm for FIR
- Generates preamble, start and stop flags
- Uses the RZI (Return-to-Zero Inverted) modulation/demodulation scheme for SIR and MIR, and the 4PPM (4 Pulse Position Modulation) modulation/demodulation scheme for FIR
- Provides synchronization by means of a DPLL in FIR mode
- Easily adaptable to different bus systems with 32-bit register interface and FIFO with configurable FIFO size

2.17 I^2S audio block

SPEAr600 contains three I^2S interfaces providing the following features.

Main features:

- Conversion of AHB protocol to I^2S protocol and vice versa
- Supports 2.0, 2.1 and 3.1 audio outputs (I^2S master mode)
- 32 (16L + 16R) and 64 bit (32L + 32R) of raw PCM data length supported
- MIC/Line-In (2.0) recording (I2S master/slave mode)
- Stereo headphone out

2.18 System controller

The System Controller provides an interface for controlling the operation of the overall system.

Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts

- Reset status capture and soft reset generation
- Watchdog module clock enable

2.18.1 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr600 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode**: In this mode the system clocks, HCLK and CLK, are disabled and the System Controller clock SCLK is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.
- **DOZE mode**: In this mode the system clocks, HCLK and CLK, and the System Controller clock SCLK are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

2.19 Clock and reset system

The clock system is a fully programmable block that generates all the clocks for the SPEAr600.

The default operating clock frequencies are:

- Clock @ 333 MHz for the CPUs.
- Clock @ 166 MHz for AHB bus and AHB peripherals. (PLL1 source)
- Clock @ 83 MHz for, APB bus and APB peripherals. (PLL1 source)
- Clock @ 100-333 MHz for DDR memory interface. (PLL1, PLL2 source)
- Clock @ 12 MHz, 30 MHz and 48 MHz for USBs (PLL3 source)

The above frequencies are the maximum allowed values.

All these clocks are generated by three PLLs.

PLL1 and PLL2 sources are fully programmable through dedicated registers.

The clock system consists of 2 main parts: a multi clock generator block and two internal PLLs.

The multi clock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr600 according to dedicated programmable registers.

Each PLL uses an oscillator input of 30 MHz to generate a clock signal at a frequency corresponding to the highest of the group. This is the reference signal used by the multi clock generator block to obtain all the other required clocks for the group. Its main feature is electromagnetic interference reduction capability.

The user can set up the PLL in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

In sleep mode the SPEAr600 runs with the PLL disabled so the available frequency is 30 MHz or a sub-multiple (/2, /4, /16 and /32) or 32 KHz.

PLL3 is used to generate the USB controller clocks and it is not configured through registers.

2.20 Vectored interrupt controller (VIC)

Each ARM Subsystem of SPEAr600 offers Vectored Interrupted Controller (VIC) blocks, providing a software interface to the interrupt system.

Acting as an interrupt controller, the VIC determines the source that is requesting service and where its interrupt service routine (ISR) is loaded, doing that in hardware.

In particular, the VIC supplies the starting address, or vector address, of the ISR corresponding to the highest priority requesting interrupt source.

Main features of the VIC are listed below:

- Support for 32 standard interrupt sources (a total of 64 lines are available for each CPU from its two daisy-chained VICs).
- Generation of both Fast Interrupt request (FIQ) and Interrupt Request (IRQ. IRQ is used for general interrupts, whereas FIQ is intended for fast, low-latency interrupt handling.
- Support for 16 vectored interrupts (IRQ only);
- Hardware interrupt priority
  - FIQ interrupt has the highest priority
  - followed by vectored IRQ interrupts, from vector 0 to vector 15
  - then non-vectored IRQ interrupts with the lowest priority
- Interrupt masking/ interrupts request status
- Software interrupt generation

2.21 General purpose timers

SPEAr600 provides five general purpose timers (GPTs) acting as APB slaves.

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through SPEAr600 configuration registers (frequencies up to 83 MHz can be synthesized).

Two different modes of operation are available:

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

2.22 Watchdog timer

The ARM watchdog module consists of a 32-bit down counter with a programmable time-out interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

2.23 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

Main features:

- Time-of-day clock in 24 hour mode
- Calendar
- Alarm capability
- Isolation mode, allowing RTC to work even if power is not supplied to the rest of the device.

2.24 Reconfigurable array subsystem connectivity (RAS)

The Reconfigurable Logic Array consists of an embedded macro where it is possible to implement a custom project by mapping up to 600k equivalent standard cells. The user can design custom logic and special function using various features offered by the Reconfigurable Logic Array and by the SPEAr600 system listed here below.

- 4 AHB bus master interfaces
- 5 AHB bus slave interfaces
- Dedicated interface with CPU1 to customize the Tightly Couple Memory
- Dedicated interface with CPU1 to customize the Coprocessor
- Dedicated interface with CPU2 to customize the Tightly Coupled Memory
- Interfaces towards a dedicated 130 kB Memory Array Subsystem provided of functional BIST driven by SoC via software and divided in the following ST memory cuts:
  - 3 single port memory cuts (48 words x 128 bits)
  - 4 single port memory cuts (2048 words x 32 bits)
  - 8 single port memory cuts (1024 words x 32 bits)
  - 16 single port memory cuts (512 words x 32 bits)
  - 8 dual port memory cuts (512 words x 32 bits)

  - 4 dual port memory cuts (1024 words x 32 bits)
- Clock system constituted by:
  - 5 clocks coming from the external balls
  - 4 clocks coming from the integrated frequency synthesizers
  - CPU core clock frequency
  - Pll2 frequency
  - 48 MHz clock (USB Pll)
  - 30 MHz clock (Main Oscillator)
  - 32.768 kHz clock (RTC Oscillator)
  - APB clock (programmable)
  - AHB clock (programmable)
  - User Configurable sync/async clock towards Memory Controller port 2 (M2)
- Connection with 84/112 I/Os
- Connection with 9 LVDS lines
- 12 interrupt lines towards CPU1 and CPU2
- 64 interrupt input lines from the various platform IP sources
- 16 peripheral DMA request lines
- 64 user configurable (in the SoC) general purpose input lines
- 64 user configurable (in the RAS) general purpose output lines
- SoC dynamic power management control interface;
- 50 specific ATE Test interface signals dedicated to RAS

2.25 External Port Controller (EXPI I/F)

The port controller is a socket communication interface between the SPEAr600 and an external FPGA device; it implements a simple AHB bidirectional protocol used to compress a couple of std AHB master/slave bus onto 84 PL_GPIOs and 4 PL_CLK primary signals.

Caution: PL_GPIO pins are not configurable by software.

ST provide a symmetric port controller logic solution to be embedded inside the external FPGA with the purpose of interfacing the EXPI bus directly and decompressing the same pair of AHB master/slave ports on the FPGA side in order to interconnect the customer logic as follows (more slave and master agents can be connected to the EXPI):

SPEAr600_AHB-master >> FPGA_AHB-slave

SPEAr600_AHB-slave << FPGA_AHB-master (AHB-full)

The EXPI interface is based on two main groups of signals:

- AHB bidirectional signal bus driven alternatively from the SPEAr600 and FPGA side.
- Unidirectional signals continuously driven from both the SPEAr600 and FPGA sides.

Table 36: EXPI - pad signal assignment lists the EXPI signal names. Further details in these signals are given in the SPEAr600 user manual (UM0510)

3 Pin description

The following tables describe the pinout of the SPEAr600 listed by functional block.

This description refers to the default configuration of SPEAr600 (full features).

More details on the configuration of each pin are given in *Table 16: Multiplexing scheme*.

- *Table 2: System reset, master clock, RTC and configuration pins*
- *Table 3: Power supply pins*
- *Table 4: Debug pins*
- *Table 5: SMI, SSP, UART, FIRDA and I2C pins*
- *Table 6: USB pins*
- *Table 7: Ethernet pins*
- *Table 8: GPIO pins*
- *Table 9: ADC pins*
- *Table 10: NAND Flash I/F pins*
- *Table 11: DDR I/F pins*
- *Table 12: LCD I/F pins*
- *Table 13: LVDS I/F pins*
- *Table 14: EXPI/I2S pins*
- *Table 15: EXPI pins*

List of abbreviations:

PU = Pull Up

PD = Pull Down

3.1 Required external components

1. DDR_COMP_1V8: place an external 121 kΩ resistor between ball V7 and ball V8
2. DDR_COMP_2V5: place an external 121 kΩ resistor between ball V9 and ball V8
3. USB_RREF: connect an external 1.5 kΩ pull-down resistor to ball U4
4. DIGITAL_REXT: place an external 121 kΩ resistor between ball E11 and ball E126.

3.2 Pin descriptions listed by functional block

Table 2. System reset, master clock, RTC and configuration pins

Group	Signal name	Ball	Direction	Function	Pin type
SYSTEM RESET	MRESET	C17	Input	Main reset	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
CONFIG	DIGITAL_REXT	E11	Ref	Configuration	Analog, 3.3 V capable, See *Note 4*

Table 2. System reset, master clock, RTC and configuration pins (continued)

Group	Signal name	Ball	Direction	Function	Pin type
Master clock	MCLK_XI	Y1	Input	30 MHz crystal I	Oscillator, 2.5 V capable
	MCLK_XO	Y2	Output	30 MHz crystal O	
RTC	RTC_XI	A9	Input	32 kHz crystal I	Oscillator, 1.8 V capable
	RTC_XO	B9	Output	32 kHz crystal O	

Table 3. Power supply pins

Group	Signal name	Ball	Value
DIGITAL GROUND	GND	J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, M18, N18, P18, T5, V6	0 V
	RTC_GNDE	A10	
	DITH_VSS	U5	
	DDR_MEM_PLL_VSS_DIG	U17	
	DIGITAL_GNDBGCOMP	E12	
ANALOG GROUND	ADC_AGND	V16	0 V
	DDR_MEM_PLL_VSS_ANA	V17	
	USB_VSSC2V5	T4	
	USB_HOST1_VSSBS	R1	
	USB_HOST2_VSSBS	N2	
	USB_DEV_VSSBS	U2	
	USB_PLL_VSSP	W3	
	USB_PLL_VSSP2V5	W2	
	MCLK_GND	Y3	
	MCLK_GNDSUB	AA3	
	DITH_VSS2V5	V5	
I/O	VDDE3V3	J6, H6, F8, F9, F16, H17, K17, L17, N17, P17, M6, F17	3.3 V
CORE	VDD	G6, L6, G17, M17, R17, F10, F13, F15, J17, T6, U13, U10, U16	1.0 V
HOST1/HOST2 USB PHY	USB_HOST_VDD3V3	R3	3.3V
HOST2 USB PHY	USB_HOST2_VDDBC	N1	2.5 V
	USB_HOST2_VDDBS	N3	1.0 V