Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

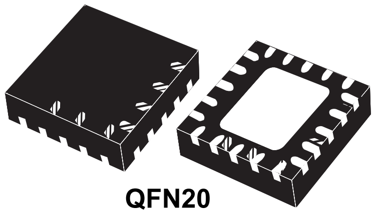
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SPIRIT1

Low data rate, low power sub-1GHz transceiver

Datasheet - production data



QFN20

Features

- Frequency bands: 150-174 MHz, 300-348 MHz, 387-470 MHz, 779-956 MHz
- Modulation schemes: 2-FSK, GFSK, MSK, GMSK, OOK, and ASK
- Air data rate from 1 to 500 kbps
- Very low power consumption (9 mA RX and 21 mA TX at +11 dBm)
- Programmable RX digital filter from 1 kHz to 800 kHz
- Programmable channel spacing (12.5 kHz min.)
- Excellent performance of receiver sensitivity (-118 dBm), selectivity, and blocking
- Programmable output power up to +16 dBm
- Fast startup and frequency synthesizer settling time (6 µs)
- Frequency offset compensation
- Integrated temperature sensor
- Battery indicator and low battery detector
- RX and TX FIFO buffer (96 bytes each)
- Configurability via SPI interface
- Automatic acknowledgment, retransmission, and timeout protocol engine
- AES 128-bit encryption co-processor
- Antenna diversity algorithm
- Fully integrated ultra low power RC oscillator
- Wake-up on internal timer and wake-up on external event
- Flexible packet length with dynamic payload length
- Sync word detection
- Address check
- Automatic CRC handling
- FEC with interleaving
- Digital RSSI output
- Programmable carrier sense (CS) indicator
- Automatic clear channel assessment (CCA) before transmitting (for listen-before-talk systems). Embedded CSMA/CA protocol
- Programmable preamble quality indicator (PQI)
- Whitening and de-whitening of data
- Wireless M-BUS, EN 300 220, FCC CFR47 15 (15.205, 15.209, 15.231, 15.247, 15.249), and ARIB STD T-67, T93, T-108 compliant
- QFN20 4x4 mm RoHS package
- Operating temperature range from -40 °C to 105 °C

Applications

- AMR (automatic meter reading)
- Home and building automation
- WSN (wireless sensors network)
- Industrial monitoring and control
- Wireless fire and security alarm systems
- Point-to-point wireless link

Table 1. Device summary

Order code	Package	Packing
SPIRIT1QTR	QFN20	Tape and reel

Contents

1 Description . . . 8

2 Introduction . . . 9

3 Typical application diagram and pin description . . . 11

3.1 Typical application diagram . . . 11

4 Pinout . . . 15

5 Absolute maximum ratings and thermal data . . . 16

6 Characteristics . . . 17

6.1 General characteristics . . . 17

6.2 Electrical specifications . . . 17

6.2.1 Electrical characteristics . . . 17

6.2.2 Digital SPI . . . 18

6.2.3 RF receiver . . . 19

6.2.4 RF transmitter . . . 24

6.2.5 Crystal oscillator . . . 29

6.2.6 Sensors . . . 30

7 Operating modes . . . 32

7.1 Reset sequence . . . 35

7.2 Timer usage . . . 36

7.3 Low duty cycle reload mode . . . 36

7.3.1 LDC mode with automatically acknowledgement. . . . 38

7.4 CSMA/CA engine . . . 38

8 Block description . . . 42

8.1 Power management . . . 42

8.1.1 Switching frequency . . . 42

8.2 Power-on-reset (POR) . . . 42

8.3 Low battery indicator . . . 42

8.4 Voltage reference . . . 43

8.5 Oscillator and RF synthesizer 43
8.6 RCO: features and calibration 47
8.6.1 RC oscillator calibration 47
8.7 AGC 47
8.8 AFC 48
8.9 Symbol timing recovery 49
8.9.1 DLL mode 49
8.9.2 PLL mode 49
8.10 Receiver 49
8.11 Transmitter 49
8.12 Temperature sensors (TS) 50
8.13 AES encryption co-processor 51

9 Transmission and reception 51
9.1 PA configuration 51
9.2 RF channel frequency settings 54
9.3 RX timeout management 55
9.4 Intermediate frequency setting 56
9.5 Modulation scheme 57
9.5.1 Data rate 59
9.5.2 RX channel bandwidth 60
9.6 Data coding and integrity check process 61
9.6.1 FEC 61
9.6.2 CRC 61
9.6.3 Data whitening 62
9.6.4 Data padding 62
9.7 Packet handler engine 62
9.7.1 STack packet 63
9.7.2 Wireless M-Bus packet (W M-BUS, EN13757-4) 64
9.7.3 Basic packet 65
9.7.4 Automatic packet filtering 66
9.7.5 Link layer protocol 67
9.8 Data modes 68
9.9 Data FIFO 69
9.10 Receiver quality indicators 71

9.10.1 RSSI 71
9.10.2 Carrier sense 72
9.10.3 PQI 72
9.10.4 SQI 73
9.11 Antenna diversity 73
9.12 Frequency hopping 74

10 MCU interface 75

10.1 Serial peripheral interface 75
10.2 Interrupts 77
10.3 GPIOs 78
10.4 MCU clock 80

11 Register table 82

12 Package mechanical data 101

13 Revision history 103

List of tables

Table 1. Device summary . . . 1
Table 2. Description of the external components of the typical application diagram . . . 13
Table 3. BOM for different bands . . . 14
Table 4. Pinout description . . . 15
Table 5. Absolute maximum ratings . . . 16
Table 6. Thermal data . . . 16
Table 7. Recommended operating conditions . . . 16
Table 8. General characteristics . . . 17
Table 9. Power consumption static modes . . . 17
Table 10. Power consumption . . . 18
Table 11. Digital SPI input and output (SDO, SDI, SCLK, CSn, and SDN) and GPIO specification (GPIO_1-4) . . . 18
Table 12. RF receiver characteristics . . . 19
Table 13. RF receiver characteristics - sensitivity . . . 22
Table 14. RF transmitter characteristics . . . 24
Table 15. Crystal oscillator characteristics . . . 29
Table 16. Ultra low power RC oscillator . . . 29
Table 17. N-Fractional ΣΔ frequency synthesizer characteristics . . . 30
Table 18. Analog temperature sensor characteristics . . . 30
Table 19. Battery indicator and low battery detector . . . 30
Table 20. States . . . 33
Table 21. Commands list . . . 34
Table 22. POR parameters . . . 36
Table 23. SPIRIT1 timers description and duration . . . 36
Table 24. SMPS configuration settings . . . 42
Table 25. Programmability of trans-conductance at startup . . . 43
Table 26. CP word look-up . . . 44
Table 27. RC calibrated speed . . . 47
Table 28. PA_level . . . 52
Table 29. Frequency threshold . . . 55
Table 30. RX timeout stop condition configuration . . . 56
Table 31. IF_OFFSET settings . . . 57
Table 32. CHFLT_M and CHFLT_E value for channel filter bandwidth (in kHz, for fclk = 24 MHz) . . 60
Table 33. CHFLT_M and CHFLT_E value for channel filter bandwidth (in kHz, for fclk = 26 MHz) . . 60
Table 34. Packet configuration . . . 67
Table 35. SPI interface timing requirements . . . 77
Table 36. Interrupts . . . 77
Table 37. Digital outputs . . . 78
Table 38. Digital inputs . . . 80
Table 39. MCU_CK_CONF configuration register . . . 80
Table 40. MCU clock vs. state . . . 81
Table 41. General configuration registers . . . 82
Table 42. Radio configuration registers (analog blocks) . . . 85
Table 43. Radio configuration registers (digital blocks) . . . 87
Table 44. Packet/protocol configuration registers . . . 89
Table 45. Frequently used registers . . . 97
Table 46. General information . . . 100
Table 47. QFN20 (4 x 4 mm.) mechanical data . . . 101

Table 48. Document revision history 103

List of figures

Figure 1. SPIRIT1 block diagram 9
Figure 2. Suggested application diagram 11
Figure 3. Application diagram for Tx boost mode 12
Figure 4. Application diagram for SMPS OFF mode 13
Figure 5. Diagram and transition 32
Figure 6. Power-on reset timing and limits 35
Figure 7. LDCR for Tx 37
Figure 8. LDCR for Rx 37
Figure 9. CSMA flowchart 40
Figure 10. Shaping of ASK signal 50
Figure 11. Output power ramping configuration 53
Figure 12. LFSR block diagram 62
Figure 13. Threshold of the linear FIFO 70
Figure 14. SPI “write” operation 76
Figure 15. SPI “read” operation 76
Figure 16. SPI “command” operation 76
Figure 17. QFN20 (4 x 4 mm.) drawing dimension 102

1 Description

The SPIRIT1 is a very low-power RF transceiver, intended for RF wireless applications in the sub-1 GHz band. It is designed to operate both in the license-free ISM and SRD frequency bands at 169, 315, 433, 868, and 915 MHz, but can also be programmed to operate at other additional frequencies in the 300-348 MHz, 387-470 MHz, and 779-956 MHz bands. The air data rate is programmable from 1 to 500 kbps, and the SPIRIT1 can be used in systems with channel spacing of 12.5/25 kHz, complying with the EN 300 220 standard. It uses a very small number of discrete external components and integrates a configurable baseband modem, which supports data management, modulation, and demodulation. The data management handles the data in the proprietary fully programmable packet format also allows the M-Bus standard compliance format (all performance classes).

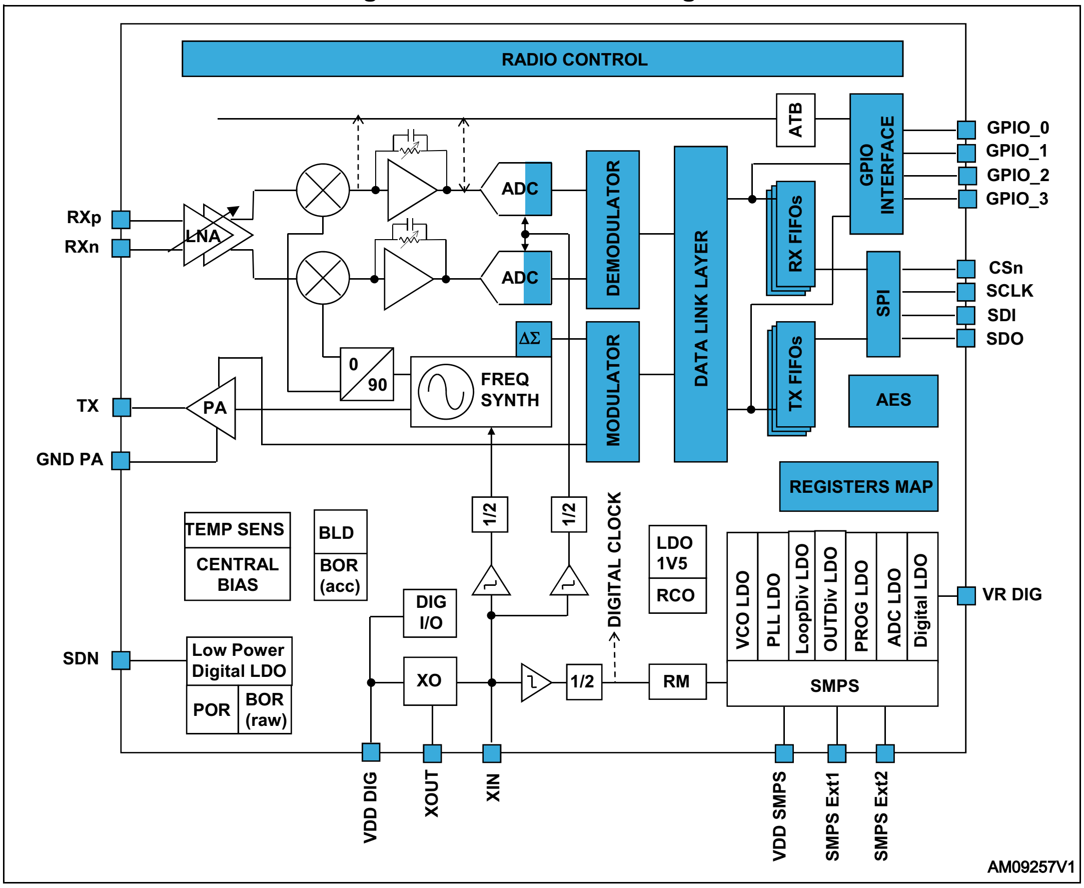
However, the SPIRIT1 can perform cyclic redundancy checks on the data as well as FEC encoding/decoding on the packets. The SPIRIT1 provides an optional automatic acknowledgement, retransmission, and timeout protocol engine in order to reduce overall system costs by handling all the high-speed link layer operations.

Moreover, the SPIRIT1 supports an embedded CSMA/CA engine. An AES 128-bit encryption co-processor is available for secure data transfer. The SPIRIT1 fully supports antenna diversity with an integrated antenna switching control algorithm. The SPIRIT1 supports different modulation schemes: 2-FSK, GFSK, OOK, ASK, and MSK. Transmitted/received data bytes are buffered in two different three-level FIFOs (TX FIFO and RX FIFO), accessible via the SPI interface for host processing.

2 Introduction

A simplified block diagram of the SPIRIT1 is shown in *Figure 1*.

Figure 1. SPIRIT1 block diagram



The receiver architecture is low-IF conversion. The received RF signal is amplified by a two-stage low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). LNA and IF amplifiers make up the RX front-end (RXFE) and have programmable gain. At IF, I/Q signals are digitized by ADCs. The demodulated data is then provided to an external MCU either through the 96-byte RX FIFO, readable via SPI, or directly using a programmable GPIO pin. A 128-bit AES co-processor is available to perform (offline) data encryption/decryption to secure data transfer.

The transmitter part of the SPIRIT1 is based on direct synthesis of the RF frequency. The power amplifier (PA) input is the LO generated by the RF synthesizer, while the output level can be configured between -30 dBm and +11 dBm in 0.5 dB steps. The data to be transmitted can be provided by an external MCU either through the 96-byte TX FIFO writable via SPI, or directly using a programmable GPIO pin. The SPIRIT1 supports frequency hopping, TX/RX and antenna diversity switch control, extending the link range and improving performance.

The SPIRIT1 has a very efficient power management (PM) system.

An integrated switched mode power supply (SMPS) regulator allows operation from a battery voltage ranging from +1.8 V to +3.6 V, and with power conversion efficiency of at least 80%.

A crystal must be connected between XIN and XOUT. It is digitally configurable to operate with different crystals. As an alternative, an external clock signal can be used to feed XIN for proper operation. The SPIRIT1 also has an integrated low-power RC oscillator, generating the 34.7 kHz signal used as a clock for the slowest timeouts (i.e. sleeping and backoff).

A standard 4-pin SPI bus is used to communicate with the external MCU. Four configurable general purpose I/Os are available.

3 Typical application diagram and pin description

3.1 Typical application diagram

This section describes different application diagram of SPIRIT1 that can be used according to customer needs. In particular *Figure 2* shows the default configuration, *Figure 3* shows the TX boost mode configuration and *Figure 4* shows the SMPS off configuration. The default configuration is giving the best power consumption figures. The TX boost mode configuration is used to increase TX output power and the SMPS off configuration is used to enhance sensitivity at the expense of power consumption. When using SMPS off configuration, SMPS should disabled by setting to1 bit DISABLE_SMPS in PM_CONFIG register. It is important the SDN pin to be driven by an external microcontroller. It should be set low when the supply voltage of the device is steady to VDD. A short circuit connection of the SDN pin to ground should be avoided.

Figure 2. Suggested application diagram

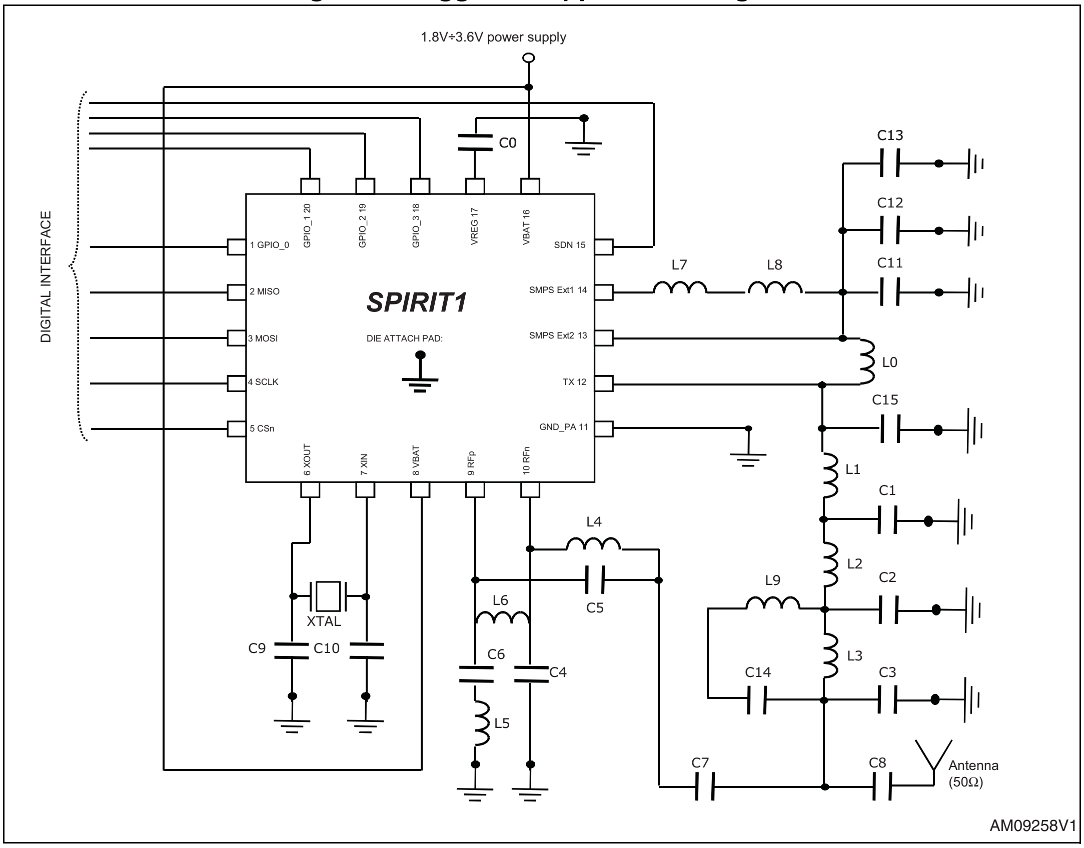


Figure 3. Application diagram for Tx boost mode

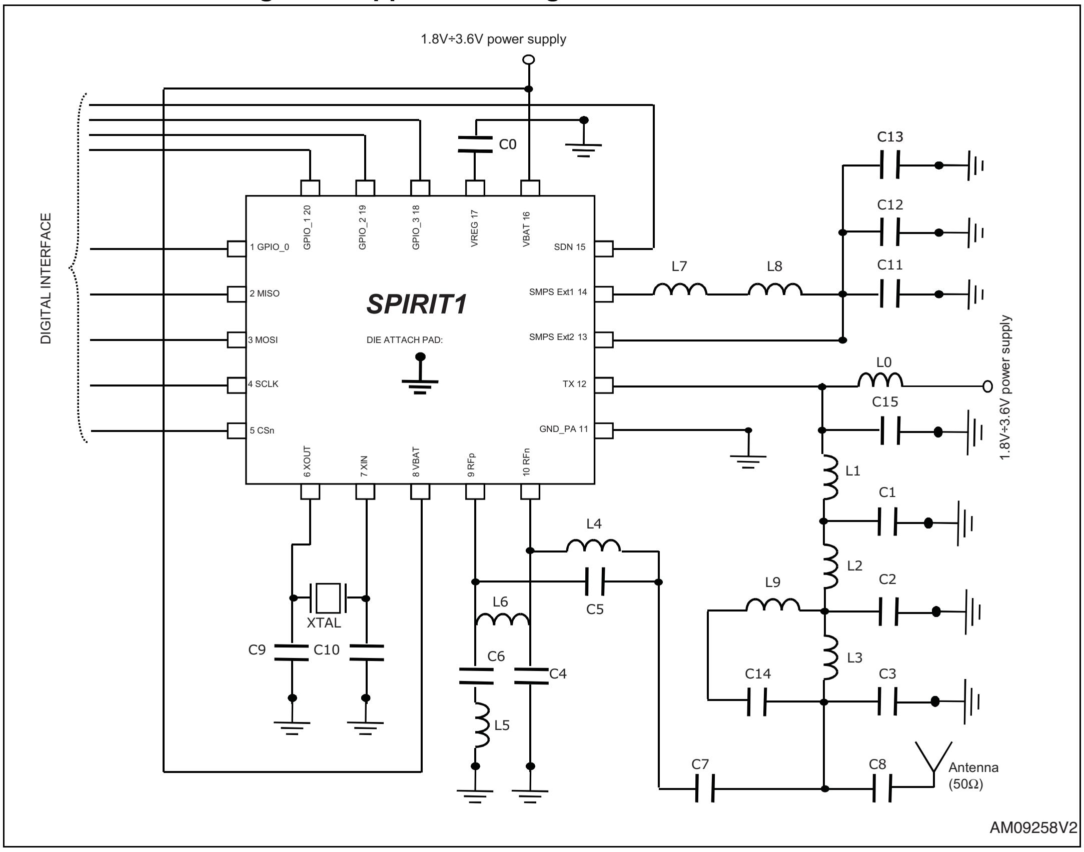


Figure 4. Application diagram for SMPS OFF mode

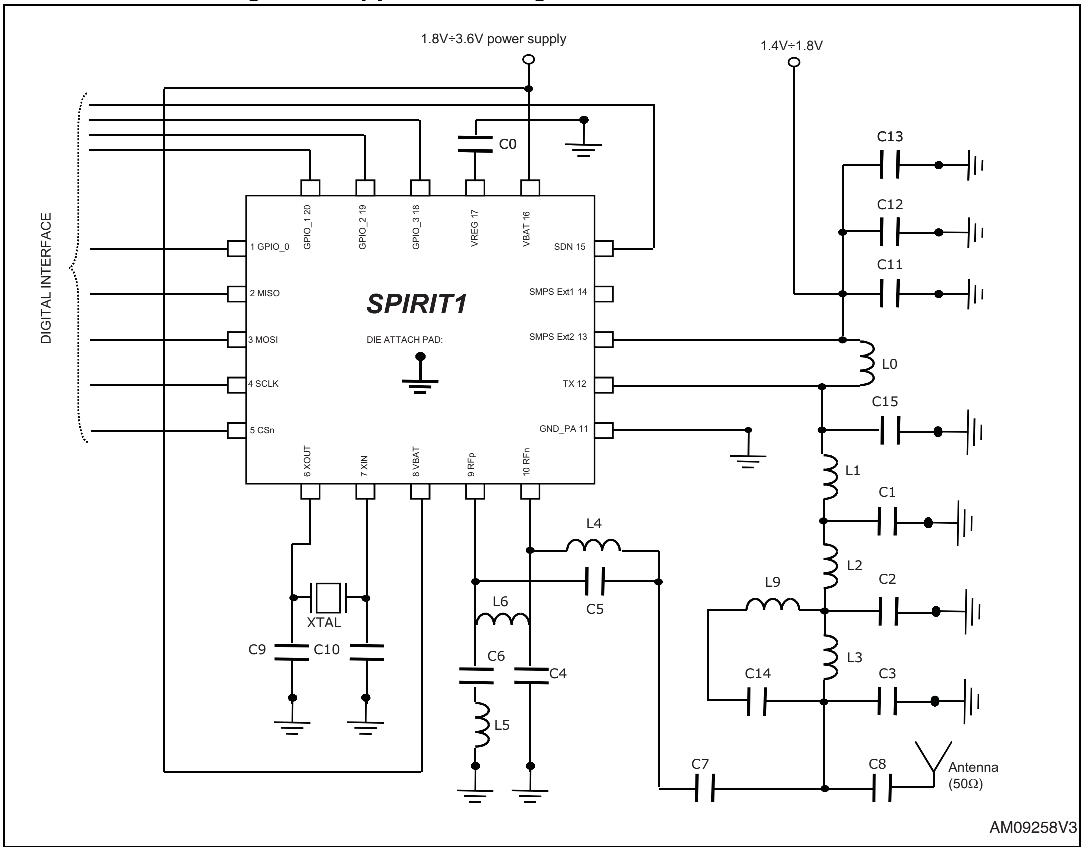


Table 2. Description of the external components of the typical application diagram

Components	Description
C0	Decoupling capacitor for on-chip voltage regulator to digital part
C1, C2, C3, C14, C15	RF LC filter/matching capacitors
C4, C5	RF balun/matching capacitors
C6, C7, C8	RF balun/matching DC blocking capacitors
C9, C10	Crystal loading capacitors
C11, C12, C13	SMPS LC filter capacitor
L0	RF choke inductor
L1, L2, L3, L9	RF LC filter/matching inductors
L4, L5, L6	RF balun/matching inductors
L7, L8	SMPS LC filter inductor
XTAL	24, 26, 48, 52 MHz

Table 2 assumes to cover all the frequency bands using a set of different as shown in *Table 3: BOM for different bands*.

Table 3. BOM for different bands

Ref design (1)	170 MHz band		315 MHz band		433 MHz band		868 MHz band		915/922 MHz band	
	STEVAL-IKRV001V1		STEVAL-IKRV001V2		STEVAL-IKRV001V3		STEVAL-IKRV001V4		STEVAL-IKRV001V5	
Comp.	Supplier	Value	Supplier	Value	Supplier	Value	Supplier	Value	Supplier	Value
C0	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF
C1	Murata	18pF	Murata	12pF	Murata	8.2pF		NE	Murata	7pF
C2	Murata	27pF	Murata	27pF	Murata	18pF	Murata	8.2pF	Murata	2.4pF
C3	Murata	4.3pF	Murata	15pF	Murata	10pF	Murata	5.6pF	Murata	3.6pF
C4		NE	Murata	3.9pF	Murata	2.2pF	Murata	2.2pF	Murata	2pF
C5	Murata	8pF	Murata	4.7pF	Murata	3.3pF	Murata	1.8pF	Murata	1.5pF
C6	Murata	220pF	Murata	220pF	Murata	220pF	Murata	220pF	Murata	330pF
C7	Murata	68nH (inductor)	Murata	220pF	Murata	220pF	Murata	220pF	Murata	220pF
C8	Murata	390pF	Murata	220pF	Murata	220pF	Murata	220pF	Murata	220pF
C9	Murata	12pF	Murata	12pF	Murata	12pF	Murata	12pF	Murata	12pF
C10	Murata	10pF	Murata	10pF	Murata	10pF	Murata	10pF	Murata	10pF
C11	Murata	1µF	Murata	1µF	Murata	1µF	Murata	470nF	Murata	1µF
C12	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF
C13	Murata	560pF	Murata	330pF	Murata	330pF	Murata	330pF	Murata	330pF
C14	Murata	220pF	Murata	1.8pF	Murata	1.8pF	Murata	1.2pF		NE
C15	Murata	6.2pF	Murata	1.2pF		NE		NE		NE
L0	Murata	200nH	Murata	220nH	Murata	150nH	Murata	100nH	Murata	100nH
L1	Coilcraft	39nH	Murata	12nH	Murata	8.2nH	Murata	3nH	Murata	3.6nH
L2	Coilcraft	56nH	Murata	12nH	Murata	10nH		0R0 (resistor)	Murata	5.1nH
L3	Murata	3.6pF (cap.)	Murata	15nH	Murata	10nH	Murata	4.3nH	Tyco Electronics	0R0
L4	Murata	100nH	Murata	47nH	Murata	39nH	Murata	18nH	Murata	15nH
L5	Murata	47nH	Murata	39nH	Murata	27nH	Murata	18nH	Murata	18nH
L6		NE		NE		NE	Murata	22nH	Murata	15nH
L7	Murata	10µH	Murata	10µH	Murata	10µH	Murata	10µH	Murata	10µH
L8		0R0 (resistor)	Murata	270nH	Murata	100nH	Coilcraft	27nH	Coilcraft	27nH
L9	Coilcraft	51nH	Murata	15nH	Murata	6.2nH	Murata	2.7nH		NE
XTAL	NDK	25 MHz	NDK	50 MHz	NDK	50 or 52 MHz	NDK	50 or 52 MHz	NDK	50 or 52 MHz

1. For complete BOM including part numbers, please check the corresponding reference design.

4 Pinout

Table 4. Pinout description

Pin	Name	I/O	Description
1	GPIO_0	I/O	See description of GPIOs below
2	MISO	O	SPI data output pin
3	MOSI	I	SPI data input pin
4	SCLK	I	SPI clock input pin
5	CSn	I	SPI chip select
6	XOUT	O	Crystal oscillator output. Connect to an external 26 MHz crystal or leave floating if driving the XIN pin with an external signal source
7	XIN	I	Crystal oscillator input. Connect to an external 26 MHz crystal or to an external source. If using an external clock source with no crystal, DC coupling with a nominal 0.2 VDC level is recommended with minimum AC amplitude of 400 mVpp. The instantaneous level at input cannot exceed the 0 - 1.4 V range.
8	VBAT	VDD	+1.8 V to +3.6 V input supply voltage
9	RXp	I	Differential RF input signal for the LNA. See application diagram for a typical matching network
10	RXn	I	
11	GND_PA	GND	Ground for PA. To be carefully decoupled from other grounds.
12	TX	O	RF output signal
13	SMPS Ext2	I	Regulated DC-DC voltage input
14	SMPS Ext1	O	DC-DC output pin
15	SDN	I	Shutdown input pin. 0-VDD V digital input. SDN should be = ‘0’ in all modes except shutdown mode. When SDN =’1’ the SPIRIT1 is completely shut down and the contents of the registers are lost. The GPIO and SPI ports during SHUTDOWN are in HiZ.
16	VBAT	VDD	+1.8 V to +3.6 V input supply voltage
17	VREG[1]	VDD	Regulated output voltage. A 100 nF decoupling capacitor is required
18	GPIO3	I/O	General purpose I/O that may be configured through the SPI registers to perform various functions, including: – MCU clock output – FIFO status flags – Wake-up input – Battery level detector – TX-RX external switch control – Antenna diversity control – Temperature sensor output
19	GPIO2	I/O	
20	GPIO1	I/O	
21	GND	GND	Exposed pad ground pin

1. This pin is intended for use with the SPIRIT1 only. It cannot be used to provide supply voltage to other devices.

5 Absolute maximum ratings and thermal data

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.

Table 5. Absolute maximum ratings

Pin	Parameter	Value	Unit
8,14,16	Supply voltage and SMPS output	-0.3 to +3.9	V
17	DC voltage on VREG	-0.3 to +1.4	V
1,3,4,5,15,18,19,20	DC voltage on digital input pins	-0.3 to +3.9	V
2	DC voltage on digital output pins	-0.3 to +3.9	V
11	DC voltage on analog pins	-0.3 to +3.9	V
6,7,9,10	DC voltage on RX/XTAL pins	-0.3 to +1.4	V
13	DC voltage on SMPS Ext2 pin	-0.3 to +1.8	V
12	DC voltage on TX pin	-0.3 to +3.9	V
T_{STG}	Storage temperature range	-40 to +125	°C
$V_{ESD\text{-}HBM}$	Electrostatic discharge voltage	±1.0	KV

Table 6. Thermal data

Symbol	Parameter	QFN20	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	45	°C/W

Table 7. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BAT}	Operating battery supply voltage	1.8	3	3.6	V
T_A	Operating ambient temperature range	-40		105	°C

6 Characteristics

6.1 General characteristics

Table 8. General characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
FREQ	Frequency range	150	-	174	MHz
		300		348	MHz
		387		470	MHz
		779		956	MHz
DR	Air data rate for each modulation scheme. Note that if "Manchester", "3-out-of-6" and/or FEC encoding/decoding options are selected, the effective bit rate will be lower.				
	2-FSK	1	-	500	kBaud
	GMSK (BT=1, BT=0.5)	1		500	kBaud
	GFSK (BT=1, BT=0.5)	1		500	kBaud
	MSK	1		500	kBaud
	OOK/ASK	1		250	kBaud

6.2 Electrical specifications

6.2.1 Electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance is referred to a 50 Ohm antenna connector, via the reference design using application diagram as in *Figure 2*, except otherwise noted.

Table 9. Power consumption static modes

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IBAT	Supply current	Shutdown (1)	-	2.5	-	nA
		Standby (1)		600		nA
		Sleep (1)		850		nA
		Ready (default mode)(1)		400		µA
		Lock(1)		4.4		mA

1. See *Table 20*.

Table 10. Power consumption

Symbol	Parameter	Test conditions	SMPS ON	SMPS OFF	Unit
IBAT	Supply current	RX (1) 169 MHz	9.2	16.9	mA
		RX (1)315 MHz	9.2	16.9	
		RX (1) 433 MHz	9.2	16.9	
		RX (1) 868 MHz	9.7	17.6	
		RX (1) 915 MHz	9.8	17.6	
		RX (1) 922 MHz	9.8	17.9	
		TX (1)(2) +16 dBm 169 MHz	54		
		TX (1)(2) +16 dBm 315 MHz	52		
		TX (1)(2) +16 dBm 433 MHz	49.3		
		TX (1)(2) +15.5 dBm 868 MHz	44		
		TX (1)(2) +16 dBm 920 MHz	45.2		
		TX (1) +11 dBm 169 MHz	18	33	
		TX (1) +11 dBm 315 MHz	22	37	
		TX (1) +11 dBm 433 MHz	19.5	33	
		TX (1) +11 dBm 868 MHz	21	41	
		TX (1) +11 dBm 920 MHz	20	39	
		TX (1) -8 dBm 169 MHz	6		
		TX (1) -8 dBm 315 MHz	6.5		
		TX (1) -7 dBm 433 MHz	7		
		TX (1) -7 dBm 868 MHz	7		

1. See table *Table 20*.
2. TX boost mode configuration V_{BAT} = 3.6 V.

6.2.2 Digital SPI

Table 11. Digital SPI input and output (SDO, SDI, SCLK, CSn, and SDN) and GPIO specification (GPIO_1-4)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency				10	MHz
C_{IN}	Port I/O capacitance			1.4		pF
T_{RISE}	Rise time	0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		6.0		ns
		0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		

Table 11. Digital SPI input and output (SDO, SDI, SCLK, CSn, and SDN) and GPIO specification (GPIO_1-4) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{FALL}	Fall time	0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		7.0		ns
		0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
V_{IH}	Logic high level input voltage		VDD/2 +0.3			V
V_{IL}	Logic low level input voltage				VDD/8 +0.3	V
V_{OH}	High level output voltage	IOH = -2.4 mA (-4.2 mA if high output current capability is programmed).	(5/8)* VDD+ 0.1			V
V_{OL}	Low level output voltage	IOL = +2.4 mA (+4 mA if high output current capability is programmed).			0.5	V

6.2.3 RF receiver

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V, no frequency offset in the RX signal. All performance is referred to a 50 Ohm antenna connector, via the reference design.

Table 12. RF receiver characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RL	Return loss	169.4-169.475 MHz, 433-435 MHz, 868-868.6 MHz, 310-320 MHz, 902-928 MHz(1)			-10	dB
CH_{BW}	Receiver channel bandwidth		1		800	kHz
P_{SAT}	Saturation 1% PER (packet length = 20 bytes) FEC DISABLED	868 MHz 2-GFSK (BT=1) 38.4 kbps (20 kHz dev. CH Filter=100 kHz)		10		dBm
IIP_3	Input third order intercept	Input power -50 dBm 915 MHz	-37	-31	-26	dBm

Table 12. RF receiver characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$C/I_{1\text{-}CH}$ (2) (3)	Adjacent channel rejection, 1% PER (packet length = 20 bytes) FEC DISABLED 868 MHz	Desired channel 3 dB above sensitivity level. 12.5 kHz Δf, 2-FSK 1.2 kbps, (1 kHz dev. CH Filter=6 kHz)		49		dB
		Desired channel 3 dB above sensitivity level. 100 kHz Δf, 2-FSK 1.2 kbps, (4.8 kHz dev. CH Filter=58 kHz)		40		dB
		Desired channel 3 dB above sensitivity level. 200 kHz Δf, 2-GFSK (BT=1) 38.4 kbps, (20 kHz dev. CH Filter=100 kHz)		40		dB
		Desired channel 3 dB above sensitivity level. 750 kHz Δf, 2-GFSK (BT=1) 250 kbps, (127 kHz dev. CH Filter=540 kHz)		38		dB
$C/I_{2\text{-}CH}$ (4)	Alternate channel rejection, 1% PER (packet length = 20 bytes) FEC DISABLED 868 MHz	Desired channel 3 dB above sensitivity level. 25 kHz Δf, 2-FSK 1.2 kbps, (1 kHz dev. CH Filter=6 kHz)		52		dB
		Desired channel 3 dB above sensitivity level. 200 kHz Δf, 2-FSK 1.2 kbps, (4.8 kHz dev. CH Filter=58 kHz)		43		dB
		Desired channel 3 dB above sensitivity level. 400 kHz Δf, 2-GFSK (BT=1) 38.4 kbps, (20 kHz dev. CH Filter=100 kHz)		44		dB
		Desired channel 3 dB above sensitivity level. 1.5 MHz Δf, 2-GFSK (BT=1) 250 kbps, (127 kHz dev. CH Filter=540 kHz)		46		dB
IM_{REJ} (4)	Image rejection, 1% PER (packet length = 20 bytes) 1% PER (packet length = 20 bytes) FEC DISABLED	868 MHz 2-GFSK (BT=1) 38.4 kbps (20kHz dev. CH Filter=100 kHz), desired channel 3 dB above the sensitivity limit, with IQC correction.		47		dB
RX_{BLK} (4)	Blocking at offset above the upper band edge and below the lower band edge 1% BER	@ 2 MHz offset, 868 MHz 2-GFSK (BT=1) 38.4kbps, desired channel 3 dB above the sensitivity limit		-42		dBm
		@ 10 MHz offset, 868 MHz 2-GFSK (BT=1) 38.4kbps, desired channel 3 dB above the sensitivity limit		-40		dBm

Table 12. RF receiver characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RX_{SPUR}	Spurious emissions (maximum values according to ETSI EN 300 220-1)	RF = 170 MHz, f< 1 GHz		-65		dBm
		RF = 170 MHz, 1 GHz < f < 4 GHz		-69		
		RF = 433 MHz - 435 MHz, f< 1 GHz		-63		
		RF = 433 MHz - 435 MHz, 1 GHz < f < 4 GHz		-83		
		RF = 868 MHz, f< 1 GHz		-70		
		RF = 868 MHz, 1 GHz < f < 6 GHz		-60		
	Spurious emissions (maximum values according to ARIB STD-T93)	RF = 312 MHz - 315 MHz, f< 1 GHz		-69		
		RF = 312 MHz - 315 MHz, f> 1 GHz		-59		
	Spurious emissions (maximum values according to ARIB STD-T67)	RF = 426 MHz - 470 MHz		-61		
	Spurious emissions (maximum values according to ARIB STD-T108)	RF = 920 MHz - 924 MHz, f< 710 MHz		<-70		
		RF = 920 MHz - 924 MHz, 710 MHz < f < 915 MHz				
		RF = 920 MHz - 924 MHz, 915 MHz < f < 930 MHz				
		RF = 920 MHz - 924 MHz, 930 MHz < f < 1 GHz				
		RF = 920 MHz - 924 MHz, f> 1 GHz		-75		
ZIN, RX	Differential Input Impedance (simulated values)	Max RX gain RF = 170 MHz RF = 315 MHz RF = 433 MHz RF = 868 MHz RF = 915 MHz RF = 922 MHz		 200 - j36 180 - j57 170 - j70 118 - j87 113 - j87 113 - j87		Ω

1. Guaranteed in an entire single sub band. Reference design can be different for different application bands.
2. Interferer is CW signal (as specified by ETSI EN 300 220 v1).
3. Selectivity performance is guaranteed if no SPI accesses are performed during reception or SPI clock is below 1 MHz.
4. Blocker is CW signal (as specified by ETSI EN 300 220 v1).

Table 13. RF receiver characteristics - sensitivity

Symbol	Parameter	Test condition	SMPS ON	SMPS OFF	Unit
RX_{SENS}	Sensitivity, 1% BER (according to W-MBUS N mode specification)	169 MHz 2-FSK 1.2kbps (4 kHz dev. CH Filter=10 kHz)	-117	-123	dBm
		169 MHz 2-GFSK (BT=0.5) 2.4kbps (2.4 kHz dev. CH Filter=7 kHz)	-114	-121	dBm
		169 MHz 2-FSK 38.4kbps (20 kHz dev. CH Filter=100 kHz)	-104	-109	dBm
		169 MHz 2-GFSK (BT=0.5) 50 kbps (25 kHz dev. CH Filter=100 kHz)	-104	-108	dBm
	Sensitivity, 1% PER (packet length = 20 bytes) FEC DISABLED	315 MHz 2-FSK 1.2 kbps (4.8 kHz dev. CH Filter=58 kHz)	-109	-110	dBm
		315 MHz MSK 500 kbps (CH Filter=800 kHz)	-88	-88	dBm

Table 13. RF receiver characteristics - sensitivity (continued)

Symbol	Parameter	Test condition	SMPS ON	SMPS OFF	Unit
RX_{SENS}	Sensitivity, 1% PER (packet length = 20 bytes) FEC DISABLED	433 MHz 2-FSK 1.2 kbps (1 kHz dev. CH Filter=6 kHz)	-116	-120	dBm
		433 MHz 2-GFSK (BT=1) 1.2 kbps (4.8 kHz dev. CH Filter=58 kHz)	-106	-110	dBm
		433 MHz 2-GFSK (BT=1) 38.4 kbps (20 kHz dev. CH Filter=100 kHz)	-103	-107	dBm
		433 MHz 2-GFSK (BT=1) 250 kbps (127 kHz dev. CH Filter=540 kHz)	-96	-100	dBm
	Sensitivity, 1% PER (packet length = 20 bytes) FEC DISABLED	868 MHz 2-FSK 1.2 kbps (1 kHz dev. CH Filter=6 kHz)	-118	-118	dBm
		868 MHz 2-GFSK (BT=1) 1.2 kbps (4.8 kHz dev. CH Filter=58 kHz)	-108	-109	dBm
		868 MHz 2-GFSK (BT=1) 38.4 kbps (20 kHz dev. CH Filter=100 kHz)	-105	-106	dBm
		868 MHz GFSK (BT=1) 250 kbps (127 kHz dev. CH Filter=540 kHz)	-98	-99	dBm
		868 MHz MSK 250 kbps (CH Filter=540 kHz)	-93	-94	dBm
	Sensitivity, 1% PER (packet length = 20 bytes) FEC DISABLED	915 MHz 2-FSK 1.2 kbps (4.8 kHz dev. CH Filter=58 kHz)	-108	-109	dBm
		915 MHz 2-FSK 38.4 kbps (20 kHz dev. CH Filter =100 kHz)	-106	-106	dBm
		915 MHz 2-FSK 250 kbps (127 kHz dev. CH Filter=540 kHz)	-98	-99	dBm
		915 MHz MSK 500 kbps (CH Filter=800 kHz)	-94	-95	dBm
	Sensitivity, 1% PER (packet length = 20 bytes) FEC DISABLED	922 MHz 2-FSK 1.2 kbps (4.8 kHz dev. CH Filter=58 kHz)	-108	-109	dBm
		922 MHz 2-FSK 38.4 kbps (20 kHz dev. CH Filter =100 kHz)	-106	-106	dBm
		922 MHz 2-FSK 250 kbps (127 kHz dev. CH Filter=540 kHz)	-98	-99	dBm
		922 MHz MSK 500 kbps (CH Filter=800 kHz)	-94	-95	dBm

Table 13. RF receiver characteristics - sensitivity (continued)

Symbol	Parameter	Test condition	SMPS ON	SMPS OFF	Unit
RX_{SENS}	Sensitivity, 1% PER (packet length = 20 bytes) FEC DISABLED(1)	433 MHz OOK 1.2 kbps (CH Filter=6 kHz)	-116	-117	dBm
		433 MHz OOK 2.4 kbps (CH Filter=12 kHz)	-113	-116	dBm
		433 MHz OOK 38.4 kbps (CH Filter=100 kHz)	-99	-100	dBm
		433 MHz OOK 250 kbps (CH Filter=540 kHz)	-87	-87	dBm
	Sensitivity, 1% PER (packet length = 20 bytes) FEC DISABLED (2)	868 MHz OOK 1.2 kbps (CH Filter=6 kHz)	-116	-116	dBm
		868 MHz OOK 2.4 kbps (CH Filter=12 kHz)	-113	-114	dBm
		868 MHz OOK 38.4 kbps (CH Filter=100 kHz)	-100	-100	dBm
		868 MHz OOK 250 kbps (CH Filter=540 kHz)	-90	-90	dBm

1. In OOK modulation, indicated value represents mean power.

6.2.4 RF transmitter

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance is referred to a 50 Ohm antenna connector, via the reference design.

Table 14. RF transmitter characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{MAX\_TX\_BOOST}$	Maximum output power(1)(2)	Delivered to a 50 Ohm single-ended load via reference design using TX boost mode configuration	-	16		dBm
P_{MAX}	Maximum output power(2)	Delivered to a 50 Ohm single-ended load via reference design	-	11		dBm
P_{MIN}	Minimum output power	Delivered to a 50 Ohm single-ended load via reference design	-	-30		dBm
P_{STEP}	Output power step		-	0.5		dB

Table 14. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{SPUR,ETSI}$	Unwanted emissions according to ETSI EN300 220-1 (harmonic included, using reference design)	RF = 170 MHz, frequencies below 1 GHz	-		-36	dBm
		RF = 170 MHz, Frequencies above 1 GHz	-		< -60	dBm
		RF = 170 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-55	dBm
		RF = 434 MHz, frequencies below 1 GHz	-		-42	dBm
		RF = 434 MHz, Frequencies above 1 GHz	-		-46	dBm
		RF = 434 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-61	dBm
		RF = 868 MHz, frequencies below 1 GHz	-		-51	dBm
		RF = 868 MHz, Frequencies above 1 GHz	-		-40	dBm
		RF = 868 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-54	dBm