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SPNZ801113

Integrated 4-Port 10/100 Managed Switch with Two MACs MII or RMII Interfaces

Rev 1.0

General Description

The SPNZ801113 is a highly-integrated, Layer 2 managed 4-port switch with optimized design, plentiful features and smallest package size. It is designed for cost-sensitive 10/100Mbps 4-port switch systems with on-chip termination, lowest-power consumption, and small package to save system cost. It has 1.4Gbps high-performance memory bandwidth, shared memory-based switch fabric with full non-blocking configuration. It also provides an extensive feature set such as the power management, programmable rate limiting and priority ratio, tag/port-based VLAN, packet filtering, quality of service (QoS), four queue prioritization, management interface, MIB counters. Port 3 and Port 4 support either MII or RMII interfaces with SW3-MII/RMII and SW4-MII/RMII (see Functional Diagram) for SPNZ801113 uplink data interface. An industrial temperature-grade version of the SPNY80111 is also available (see "Ordering Information" section).The SPNZ801113 provides multiple CPU control/data interfaces to effectively address both current and emerging fast Ethernet applications.

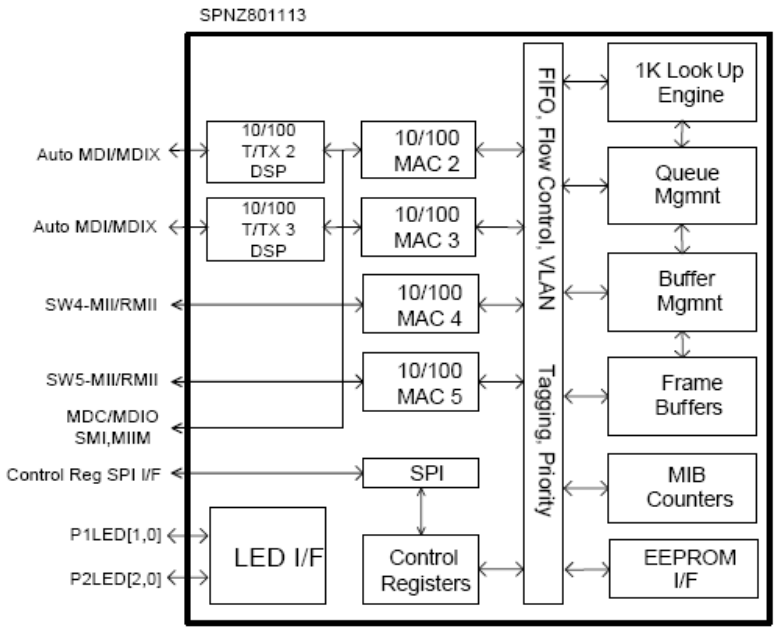
The SPNZ801113 consists of 10/100 fast Ethernet PHYs with patented and enhanced mixed-signal technology, media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

The SPNZ801113 contains four MACs and two PHYs. The two PHYs support the 10/100Base-T/TX.

All registers of MACs and PHYs units can be managed by the control interface of SPI or the SMI. MIIM registers of the PHYs can be accessed through the MDC/MDIO interface. EEPROM can set all control registers by I^2C controller interface for the unmanaged mode.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram



Features

Advanced Switch Features

- IEEE 802.1q VLAN support for up to 128 VLAN groups (full-range 4096 of VLAN IDs).
- Static MAC table supports up to 32 entries.
- VLAN ID tag/untag options, per port basis.
- IEEE 802.1p/q tag insertion or removal on a per port basis based on ingress port (egress).
- Programmable rate limiting at the ingress and egress on a per port basis.
- Jitter-free per packet based rate limiting support.
- Broadcast storm protection with percentage control (global and per port basis).
- IEEE 802.1d rapid spanning tree protocol RSTP support.
- Tail tag mode (1 byte added before FCS) support at Port 4 to inform the processor which ingress port receives the packet.
- 1.4Gbps high-performance memory bandwidth and shared memory based switch fabric with fully non-blocking configuration.
- Dual MII/RMII with MAC 3 SW3-MII/RMII and MAC 4 SW4-MII/RMII interfaces.
- Enable/Disable option for huge frame size up to 2000 Bytes per frame.
- IGMP v1/v2 snooping (Ipv4) support for multicast packet filtering.
- IPv4/IPv6 QoS support.
- Support unknown unicast/multicast address and unknown VID packet filtering.
- Self-address filtering.

Comprehensive Configuration Register Access

- Serial management interface (MDC/MDIO) to all PHYs registers and SMI interface (MDC/MDIO) to all registers.
- High-speed SPI (up to 25MHz) and I^2C master Interface to all internal registers.
- I/0 pins strapping and EEPROM to program selective registers in unmanaged switch mode.
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…).

QoS/CoS Packet Prioritization Support

- Per port, 802.1p and DiffServ-based.
- 1/2/4-queue QoS prioritization selection.
- Programmable weighted fair queuing for ratio control.
- Re-mapping of 802.1p priority field per port basis.

Integrated 4-Port 10/100 Ethernet Switch

- New generation switch with five MACs and five PHYs that are fully compliant with the IEEE 802.3u standard.
- Non-blocking switch fabric assures fast packet delivery by utilizing an 1K MAC address lookup table and a store-and-forward architecture.
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table).
- Full-duplex IEEE 802.3x flow control (PAUSE) with force mode option.
- Half-duplex back pressure flow control.
- HP Auto MDI/MDI-X and IEEE Auto crossover support.
- MII interface of MAC supports both MAC mode and PHY mode.
- Per port LED Indicators for link, activity, and 10/100 speed.
- Register port status support for link, activity, full/half duplex and 10/100 speed.
- On-chip terminations and internal biasing technology for cost down and lowest power consumption.

Switch Monitoring Features

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII/RMII.
- MIB counters for fully-compliant statistics gathering 34 MIB counters per port.
- Loop-back support for MAC, PHY and remote diagnostic of failure.
- Interrupt for the link change on any ports.

Low-Power Dissipation:

- Full-chip hardware power-down.
- Full-chip software power-down and per port software power down.
- Energy-detect mode support <0.1W full-chip power consumption when all ports have no activity.
- Very-low full-chip power consumption (<0.3W), without extra power consumption on transformers.
- Dynamic clock tree shutdown feature.
- Voltages:
  - Analog VDDAT 3.3V only.
  - VDDIO support 3.3V, 2.5V and 1.8V.
  - Low 1.2V core power.
  - 0.13um CMOS technology.
- Commercial temperature range: 0°C to +70°C.
- Industrial Temperature Range: –40°C to +85°C.
- Available in 64-pin QFN, lead-free small package

Applications

- VoIP Phone
- Set-top/Game Box
- Automotive Ethernet
- Industrial Control
- IPTV POF
- SOHO Residential Gateway
- Broadband Gateway / Firewall / VPN
- Integrated DSL/Cable Modem
- Wireless LAN access point + gateway
- Standalone 10/100 switch
- Embedded System

Ordering Information

Part Number	Temperature Range	Package	Lead Finish/Grade
SPNZ801113	0°C to 70°C	64-Pin QFN	Pb-Free/Commercial
SPNY801113	–40°C to +85°C	64-Pin QFN	Pb-Free/Industrial

Revision History

Revision	Date	Description
1.0	06/18/12	Initial document created.

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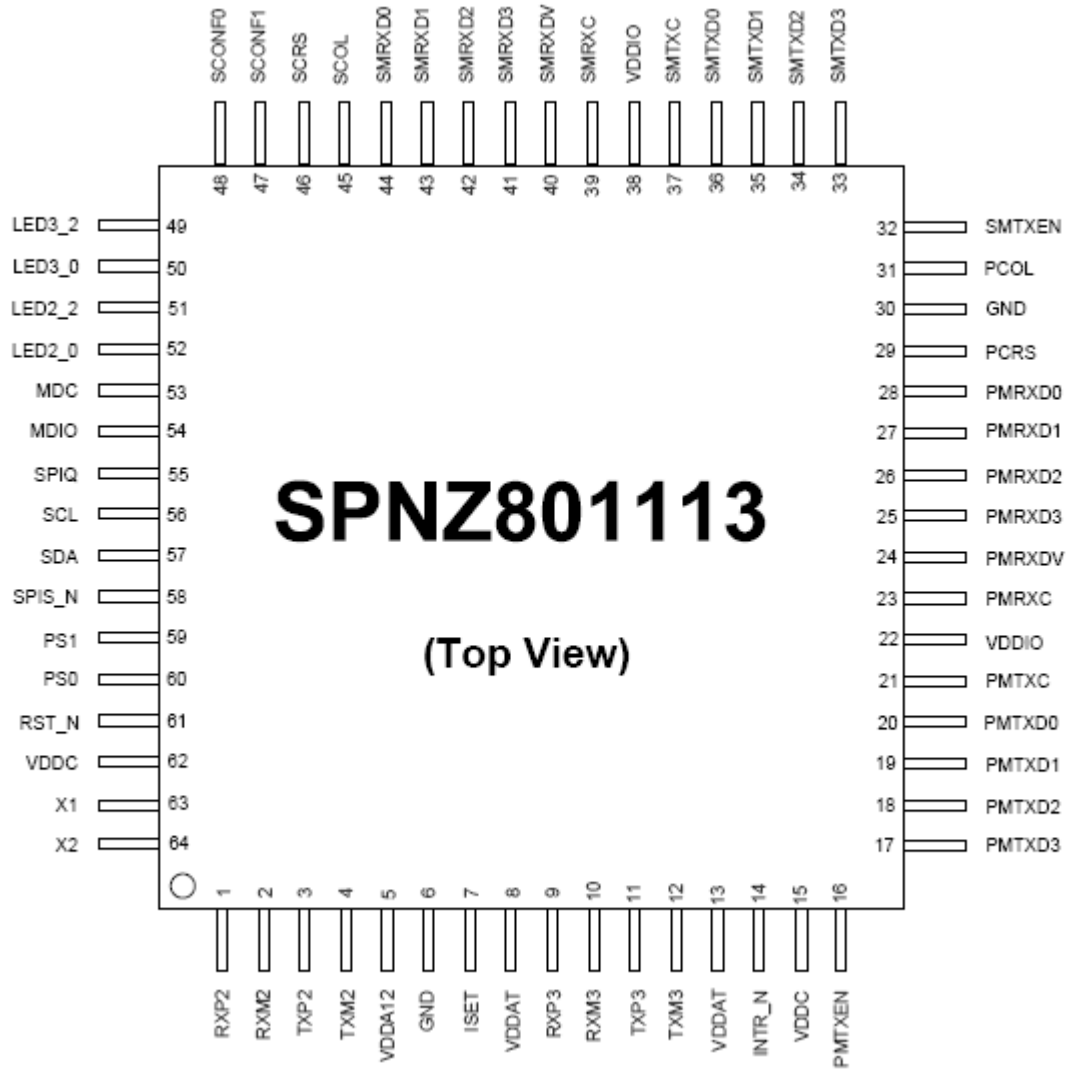
Pin Configuration



64-Pin QFN

Pin Description

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
1	RXP1	I	1	Physical receive signal + (differential).
2	RXM1	I	1	Physical receive signal – (differential).
3	TXP1	O	1	Physical transmit signal + (differential).
4	TXM1	O	1	Physical transmit signal – (differential).
5	VDDA12	P		1.2V analog power.
6	GND	GND		Ground with all grounding of die bottom.
7	ISET			Set physical transmit output current. Pull-down with a 12.4kΩ1% resistor.
8	VDDAT	P		3.3V analog V_{DD}.
9	RXP2	I	2	Physical receive signal + (differential).
10	RXM2	I	2	Physical receive signal - (differential).
11	TXP2	O	2	Physical transmit signal + (differential).
12	TXM2	O	2	Physical transmit signal – (differential).
13	VDDAT	P		3.3V analog V_{DD}.
14	INTR_N	OPU		Interrupt. This pin is Open-Drain output pin.
15	VDDC	P		1.2V digital core V_{DD}.
16	SM3TXEN	IPD	3	MAC3 Switch MII/RMII transmit enable.
17	SM3TXD3	IPD	3	MAC3 Switch MII transmit bit 3.
18	SM3TXD2	IPD	3	MAC3 Switch MII transmit bit 2.
19	SM3TXD1	IPD	3	MAC3 Switch MII/RMII transmit bit 1.
20	SM3TXD0	IPD	3	MAC3 Switch MII/RMII transmit bit 0.
21	SM3TXC/SM3REFCLK	I/O	3	MAC3 Switch MII transmit clock: Input: SW3-MII MAC mode. Output: SW3-MII PHY mode. Input: SW3-RMII reference clock.
22	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.
23	SM3RXC	I/O	3	MAC3 Switch MII Receive clock: Input: SW3-MII MAC mode. Output: SW3-MII PHY mode. Output: SW3-RMII reference clock. Unused RMII clock can be pull-down or disable by register 87.
24	SM3RXDV/SM3CRSDV	IPD/O	3	SM3RXDV: MAC3 Switch SW3-MII receive data valid. SM3CRSDV: MAC3 Switch SW3-RMII Carrier Sense/Receive Data Valid.
25	SM3RXD3	IPD/O	3	MAC3 Switch MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
26	SM3RXD2	IPD/O	3	MAC3 Switch MII receive bit 2 and Strap option: PD (default) = disable back pressure; PU = enable back pressure.
27	SM3RXD1	IPD/O	3	MAC3 Switch MII/RMII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
28	SM3RXD0	IPD/O	3	MAC3 Switch MII/RMII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
29	SM3CRS	IPD/O	3	MAC3 Switch MII carrier sense.
30	GND	GND		Ground with all grounding of die bottom.
31	SM3COL	IPD/O	3	MAC3 Switch MII collision detect.
32	SM4TXEN	IPD	4	MAC4 Switch MII/RMII transmit enable.
33	SM4TXD3	IPD	4	MAC4 Switch MII transmit bit 3.
34	SM4TXD2	IPD	4	MAC4 Switch MII transmit bit 2.
35	SM4TXD1	IPD	4	MAC4 Switch MII/RMII transmit bit 1.
36	SM4TXD0	IPD	4	MAC4 Switch MII/RMII transmit bit 0.
37	SM4TXC/SM4REFCLK	I/O	4	MAC4 Switch MII transmit clock: Input: SW4-MII MAC mode clock. Input: SW4-RMII reference clock, please also see the strap-in pin P1LED1 for the clock mode and normal mode. Output: SW4-MII PHY modes.
38	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.
39	SM4RXC	I/O	4	MAC4 Switch MII Receive clock: Input: SW4-MII MAC mode. Output: SW4-MII PHY mode. Output: SW4-RMII 50MHz reference clock (the device is default clock mode, the clock source comes from X1/X2 pins 25MHz crystal). When set the device as normal mode (the chip's clock source comes from SM4TXC), the SM4RXC reference clock output should be disabled by the register 87. Please also see the strap-in pin P1LED1 for the selection of the clock mode and normal mode.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
40	SM4RXDV/SM4CRSDV	IPD/O	4	SM4RXDV: MAC4 Switch SW4-MII receive data valid. SM4CRSDV: MAC4 Switch SW4-RMII Carrier Sense/Receive Data Valid
41	SM4RXD3	IPD/O	4	MAC4 Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII/RMII full-duplex flow control; PU = Enable Switch MII/RMII full-duplex flow control.
42	SM4RXD2	IPD/O	4	MAC4 Switch MII receive bit 2. Strap option: PD (default) = Switch MII/RMII in full-duplex mode; PU = Switch MII/RMII in half-duplex mode.
43	SM4RXD1	IPD/O	4	MAC4 Switch MII/RMII receive bit 1. Strap option: PD (default) =MAC4 Switch SW4-MII/RMII in 100Mbps mode; PU = MAC4 Switch SW-5MII/RMII in 10Mbps mode.
44	SM4RXD0	IPD/O	4	MAC4 Switch MII/RMII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = Mode 1. See “Register 11.”

	Mode 0	Mode 1
PxLED1	Lnk/Act	100Lnk/Act
PxLED0	Speed	Full duplex

45	SM4COL	IPD/O	4	MAC4 Switch MII collision detect: Input: SW4-MII MAC modes. Output: SW4-MII PHY modes.
46	SM4CRS	IPD/O	4	MAC4 Switch MII modes carrier sense: Input: SW4-MII MAC modes. Output: SW4-MII PHY modes.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]	
47	SCONF1	IPD		MAC4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF1 Pin 47 with SCONF0 Pin 48 together. See pins configuration table below:	
				Pin# (47,48)	Port 4 Switch MAC4 SW4- MII
				00 (Default)	SW4-MII PHY mode
				01	Disabled
				10	Disabled
				11	SW4-MII MAC mode
48	SCONF0	IPD		Port 4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF0 pin 48 with SCONF1 Pin 47 together. See Pin 47 description.	
49	P2LED1	IPU/O	2	LED indicator for Port 2. This pin has to be pulled down by 1K resistor in the design for SPNZ801113.	
50	P2LED0	IPU/O	2	LED indicator for Port 2. Strap option: Switch MAC3 used only. PU (default) = Select MII interface for the Switch MAC3 SW3-MII. PD = Select RMII interface for the Switch MAC3 SW3-RMII.	
51	P1LED1	IPU/O	1	LED indicator for Port 1. Strap option: Switch RMII used only. PU (default) = Select the device as clock mode, when use RMII interface, all clock source come from pin x1/x2 crystal 25MHz. PD = Select the device as normal mode when use RMII interface. All clock source comes from SW4-RMII SM4TXC pin with an external input 50MHz clock. In the normal mode, the 25MHz crystal clock from pin X1/X2 doesn't take affect and should disable SW4-RMII SW4RXC 50MHz clock output by the register 87. The normal mode is used when SW4-RMII receive an external 50MHz RMII reference clock from pin SM4TXC.	

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
52	P1LED0	IPU/O	1	LED indicator for Port 1. Strap option: for Switch MAC4 only. PU (default) = Select MII interface for the Switch MAC4 SW4-MII. PD = Select RMII interface for the Switch MAC4 SW4-RMII.
53	MDC	IPU	All	MII management interface clock. Or SMI interface clock
54	MDIO	IPU/O	All	MII management data I/O. Or SMI interface data I/O Features internal pull down to define pin state when not driven. Note: Need an external pull-up when driven.
55	SPIQ	IPU/O	All	SPI serial data output in SPI slave mode. Note: Need an external pull-up when driven.
56	SPIC/SCL	IPU/O	All	(1) Input clock up to 25MHz in SPI slave mode, (2) output clock at 61KHz in I^2C master mode. Note: Need an external pull-up when driven.
57	SPID/SDA	IPU/O	All	(1) Serial data input in SPI slave mode; (2) serial data input/output in I^2C master mode. Note: Need an external pull-up when driven.
58	SPIS_N	IPU	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the device is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer. (2) Not used in I^2C master mode.
59	PS1	IPD		Serial bus configuration pin. For this case, if the EEPROM is not present, the Switch will start itself with the PS[1.0] = 00 default register values.
				Pin Configuration: Serial Bus Configuration
				PS[1.0]=00: I^2C Master Mode for EEPROM
				PS[1.0]=01: SMI Interface Mode
				PS[1.0]=10: SPI Slave Mode for CPU Interface
				PS[1.0]=11: Factory Test Mode (BIST)
60	PS0	IPD		Serial bus configuration pin.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
61	RST_N	IPU		Reset the device. Active low.
62	VDDC	P		1.2V digital core V_{DD}.
63	X1	I		25MHz crystal clock connection/or 3.3V Oscillator input. Crystal/Oscillator should be <= ±50ppm tolerance.
64	X2	O		25MHz crystal clock connection.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   IPU = Input w/internal pull-up.
   IPD = Input w/internal pull-down.
   IPD/O = Input w/internal pull-down during reset, output pin otherwise.
   IPU/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   OTRI = Output tristated.

Pin for Strap-In Options

The SPNZ801113 can function as a managed switch or unmanaged switch. If no EEPROM or micro-controller exists, the SPNZ801113 will operate from its default setting. The strap-in option pins can be configures by external pull-up/down resistors and take the effect after power up reset or warm reset, the functions are described in the following table:

Pin Number	Pin Name	Type(1)	Port	Pin Function(2)
25	SM3RXD3	IPD/O		MAC3 Switch MII receive bit 3 Strap option: PD (default) = enable flow control; PU = disable flow control.
26	SM3RXD2	IPD/O		MAC3 Switch MII receive bit 2 and Strap option: PD (default) = disable back pressure; PU = enable back pressure.
27	SM3RXD1	IPD/O		MAC3 Switch MII/RMII receive bit 1 Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
28	SM3RXD0	IPD/O		MAC3 Switch MII/RMII receive bit 0 Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
41	SM4RXD3	IPD/O		MAC4 Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII/RMII full-duplex flow control; PU = Enable Switch MII/RMII full-duplex flow control.
42	SM4RXD2	IPD/O		*MAC4 Switch MII receive bit 2.* *Strap option:* *PD (default) = Switch MII/RMII in full-duplex mode;* *PU = Switch MII/RMII in half-duplex mode.*
43	SM4RXD1	IPD/O		MAC4 Switch MII/RMII receive bit 1. Strap option: PD (default) =MAC4 Switch SW4-MII/RMII in 100Mbps mode; PU = MAC4 Switch SW-5MII/RMII in 10Mbps mode.
44	SM4RXD0	IPD/O		MAC4 Switch MII/RMII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.”

	Mode 0	Mode 1
PxLED1	Lnk/Act	100Lnk/Act
PxLED0	Speed	Full duplex

Pin for Strap-In Options (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]	
47	SCONF1	IPD		MAC4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF1 Pin 47 with SCONF0 Pin 48 together. See pins configuration table below:	
				Pin# (47,48)	Switch MAC4 SW4- MII/RMII
				00 (Default)	SW4-MII PHY mode
				01	Disabled
				10	Disabled
				11	SW4-MII MAC mode
48	SCONF0	IPD		Port 4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF0 Pin 48 with SCONF1 Pin 47 together. See pin 47 description.	
49	P2LED1	IPU/O	2	LED indicator for Port 2. This pin has to be pulled down by 1K resistor in the design for SPNZ801113.	
50	P2LED0	IPU/O	2	LED indicator for Port 2. Strap option: Switch MAC3 used only. PU (default) = Select MII interface for the Switch MAC3 SW3-MII. PD = Select RMII interface for the Switch MAC3 SW3-RMII.	
51	P1LED1	IPU/O	1	LED indicator for Port 1. Strap option: Switch RMII used only. PU (default) = Select the device as clock mode. When use RMII interface, all clock source come from Pin x1/x2 crystal 25MHz. PD = Select the device as normal mode when use RMII interface. All clock sources come from SW4-RMII SM4TXC pin with an external input 50MHz clock. In the normal mode, the 25MHz crystal clock from pin X1/X2 doesn't take affect and should disable SW4-RMII SW4RXC 50MHz clock output by the register 87. The normal mode is used when SW4-RMII receive an external 50MHz RMII reference clock from pin SM4TXC.	
52	P1LED0	IPU/O	1	LED indicator for Port 1. Strap option: for Switch MAC4 only. PU (default) = Select MII interface for the Switch MAC4 SW4-MII. PD = Select RMII interface for the Switch MAC4 SW4-RMII.	

Pin for Strap-In Options (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]	
59	PS1	IPD		Serial bus configuration pin. For this case, if the EEPROM is not present, the Switch will start itself with the PS[1.0] = 00 default register values.	
				Pin Configuration	Serial Bus Configuration
				PS[1.0]=00	I^2C Master Mode for EEPROM
				PS[1.0]=01	SMI Interface Mode
				PS[1.0]=10	SPI Slave Mode for CPU Interface
				PS[1.0]=11	Factory Test Mode (BIST)

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   IPU = Input w/internal pull-up.
   IPD = Input w/internal pull-down.
   IPD/O = Input w/internal pull-down during reset, output pin otherwise.
   IPU/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   OTRI = Output tristated.

Introduction

The SPNZ801113 contains two 10/100 physical layer transceivers and four media access control (MAC) units with an integrated Layer 2 managed switch. The device runs in multiple modes. They are two copper + two MAC MII, two copper + two MAC RMII, two copper + 1 MAC MII+ 1 MAC RMII and two copper + 1 MAC MII or 1 MAC RMII. Those are useful for implementing multiple products in many applications.

The SPNZ801113 has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the SPNZ801113 via the SPI bus, or partial control via the MDC/MDIO interface. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the SPNZ801113 supports IEEE 802.3 10BASE-T, 100BASE-TX on all ports with Auto MDI/MDIX. The SPNZ801113 can be used as fully managed 4-port switch through two microprocessors by its two MII interface or RMII interface for an advance management application.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry with enhanced mix signal technology that makes the design more efficient and allows for lower power consumption and smaller chip die size.

The major enhancement of the SPNZ801113 is a small package with two configurable MII and RMII modes for two MAC interfaces. The SPNZ801113 supports more new features for host processor management, multiple kind of packets filtering, tag as well as port based VLAN, rapid spanning tree support, IGMP snooping support, port mirroring support and more flexible rate limiting and more functionality.

Functional Overview: Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The SPNZ801113 generates 125MHz, 83MHz, 41MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator.

Scrambler/De-Scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

10BASE-T Transmit

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the SPNZ801113 decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the SPNZ801113 supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8898MQ/TMQ device. This feature is extremely useful when end users are unaware of cable types, and also, saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers, or MIIM PHY registers. The IEEE 802.3u standard MDI and MDI-X definitions are:

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 1. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 1 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

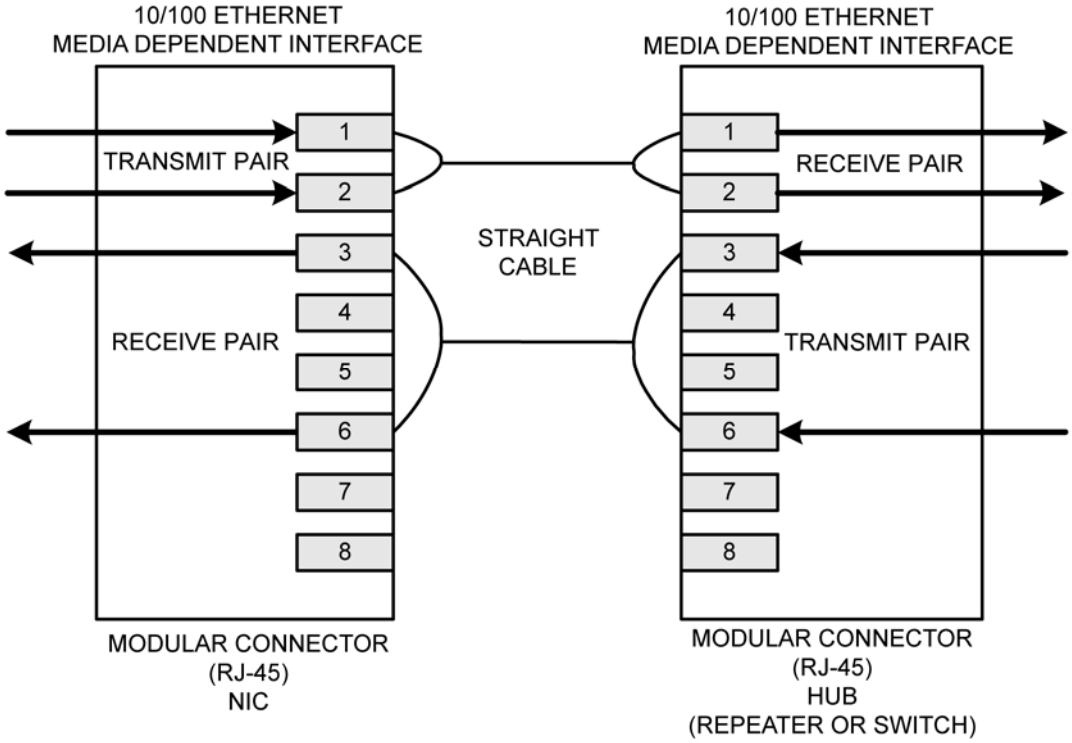


Figure 1. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

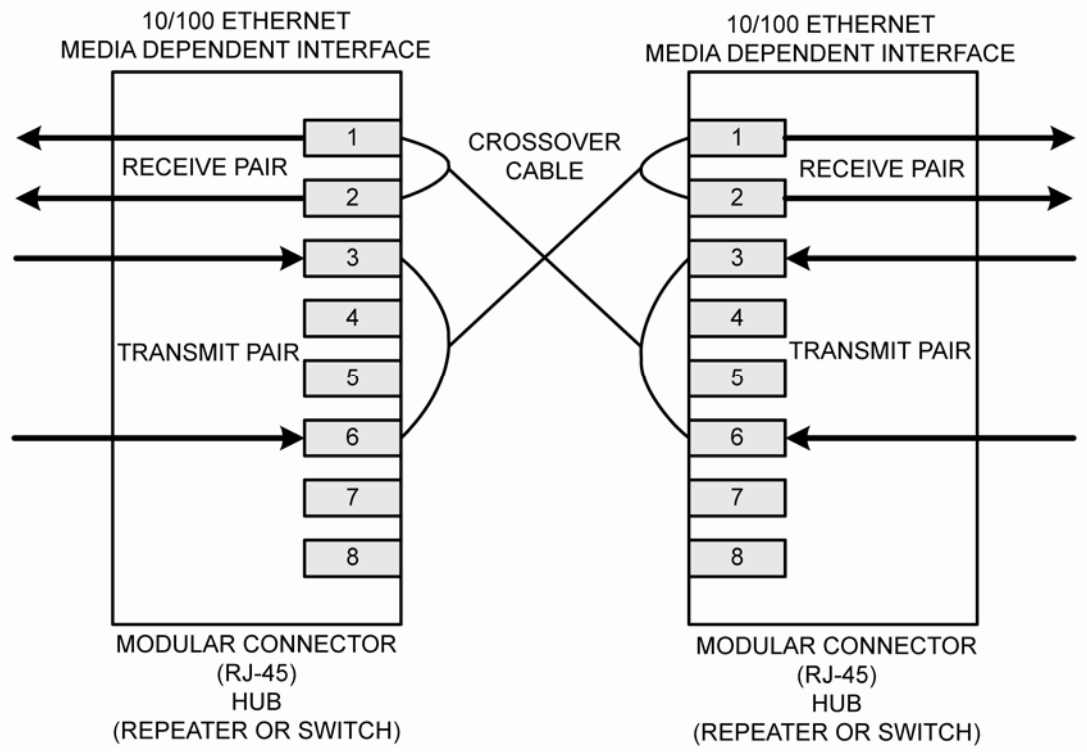


Figure 2. Typical Crossover Cable Connection

Auto-Negotiation

The SPNZ801113 conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Highest: 100Base-TX, full-duplex
- High: 100Base-TX, half-duplex
- Low: 10Base-T, full-duplex
- Lowest: 10Base-T, half-duplex

If auto-negotiation is not supported or the SPNZ801113 link partner is forced to bypass auto-negotiation, then the SPNZ801113 sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the SPNZ801113 to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. The auto-negotiation link up process is shown in Figure 3:

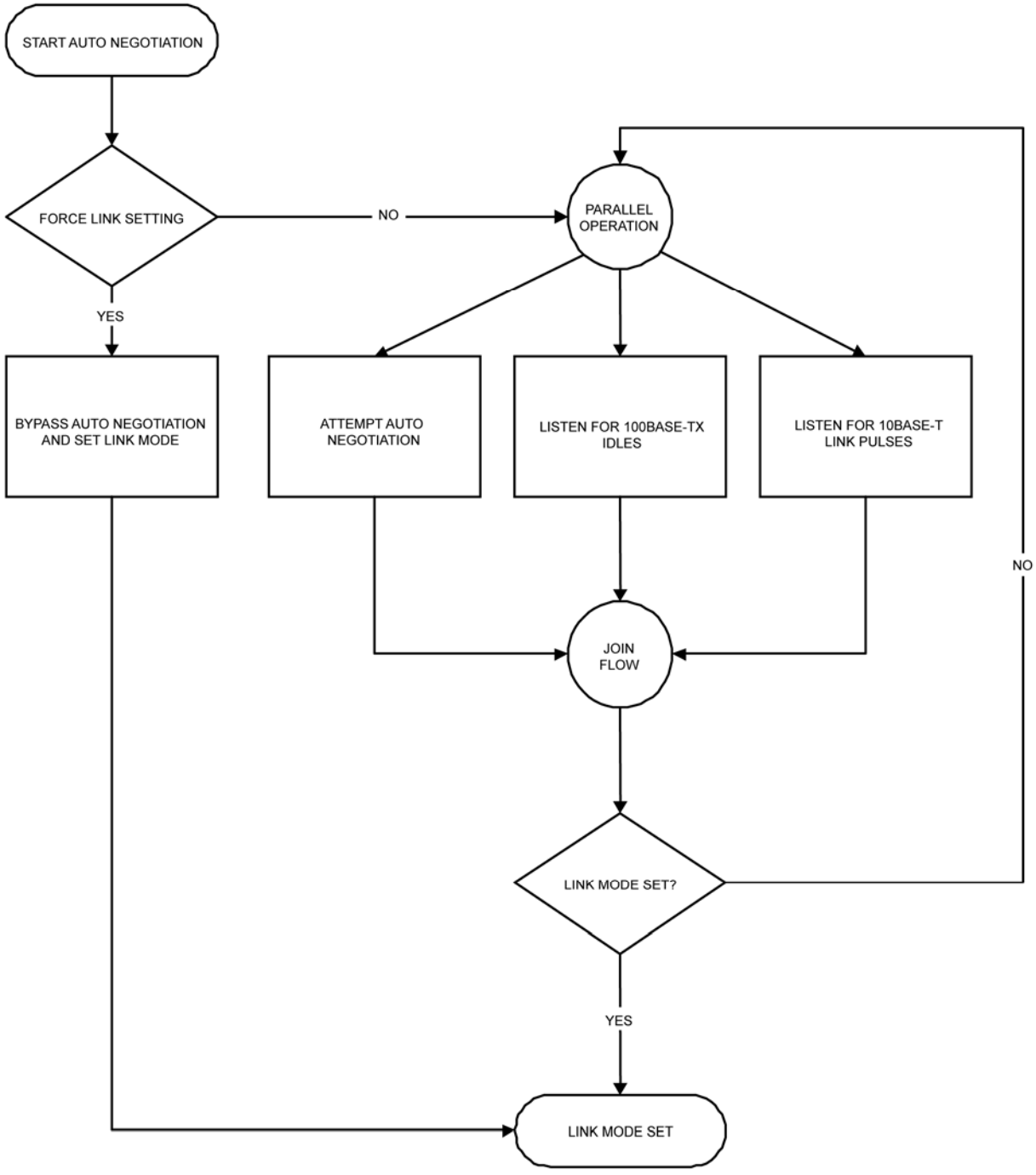


Figure 3. Auto-Negotiation

On-Chip Termination Resistors

The SPNZ801113 reduces board cost and simplifies board layout by using on-chip termination resistors for RX/TX differential pairs without the external termination resistors. The solution of the on chip termination and internal biasing will enhance much power consumption compare with using external biasing and termination resistors, and the transformer will not consume power any longer. The center tap doesn't need to be tied to analog power, just leave them floating or connect the capacitors to ground separately.

Functional Overview: Power Management

The SPNZ801113 can also use multiple power level of 3.3V, 2.5V or 1.8V for VDDIO to support different I/O voltage.

The SPNZ801113 supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are five operation modes under the power management function which is controlled by the Register 14 bit [4:3] and the Port Register Control 13 bit3 as shown below:

Register 14 bit [4:3] = 00 Normal Operation Mode

Register 14 bit [4:3] = 01 Energy Detect Mode

Register 14 bit [4:3] = 10 Soft Power Down Mode

Register 14 bit [4:3] = 11 Power Saving Mode

The Port Register Control 13 bit 3 =1 is for the Port Based Power-Down Mode

Table 2 indicates all internal function blocks status under four different power management operation modes.

SPNZ801113 Function Blocks	Power Management Operation Modes			
	Normal Mode	Power Saving Mode	Energy Detect Mode	Soft Power Down Mode
Internal PLL Clock	Enabled	Enabled	Disabled	Disabled
Tx/Rx PHY	Enabled	*Rx unused block disabled*	Energy detect at Rx	Disabled
MAC	Enabled	Enabled	Disabled	Disabled
Host Interface	Enabled	Enabled	Disabled	Disabled

Table 2. Internal Function Block Status

Normal Operation Mode

This is the default setting bit [4:3] =00 in register 14 after the chip power-up or hardware reset. When SPNZ801113 is in this normal operation mode, all PLL clocks are running, PHY and MAC are on and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit [4:3] in register 14 to transit the current normal operation mode to any one of the other three power management operation modes.

Energy Detect Mode

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the SPNZ801113 is not connected to an active link partner. In this mode, if the cable is not plugged, then the SPNZ801113 can automatically enter to a low power state, i.e., the energy detect mode. In this mode, SPNZ801113 will keep transmitting 120ns width pulses at 1 pulse/s rate. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the SPNZ801113 can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the SPNZ801113 reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit [4:3] = 01 in register 14. When the SPNZ801113 is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit [7:0] Go-Sleep time in register 15, then the SPNZ801113 will go into a low power state. When SPNZ801113 is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable, SPNZ801113 will enter normal power state. When SPNZ801113 is at normal power state, it is able to transmit or receive packet from the cable.

Soft Power-Down Mode

The soft power-down mode is entered by setting bit [4:3] =10 in register 14. When SPNZ801113 is in this mode, all PLL clocks are disabled, also all of PHYs and the MACs are off. Any dummy host access will wake-up this device from current soft power down mode to normal operation mode and internal reset will be issued to make all internal registers go to the default values.

Power Saving Mode

The power saving mode is entered when auto-negotiation mode is enabled, cable is disconnected, and by setting bit [4:3] =11 in register 14. When SPNZ801113 is in this mode, all PLL clocks are enabled, MAC is on, all internal registers value will not change, and host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the SPNZ801113 can automatically enabled the PHY power up to normal power state from power saving mode.

During this power saving mode, the host CPU can set bit [4:3] in register 14 to transit the current power saving mode to any one of the other three power management operation modes.

Port-Based Power-Down Mode

In addition, the SPNZ801113 features a per-port power down mode. To save power, a PHY port that is not in use can be powered down by the port registers control 13 bit3, or MIIM PHY registers 0 bit11.

Functional Overview: Switch Core

Address Look-Up

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The SPNZ801113 is guaranteed to learn 1K addresses and distinguishes itself from a hash-based look-up table which, depending upon the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal look-up engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted first to make room for the new entry.

Migration

The internal look-up engine also monitors whether a station is moved. If this occurs, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

Aging

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 +/- 75 seconds. This feature can be enabled or disabled through Register 3. See "Register 3" section.