# imall

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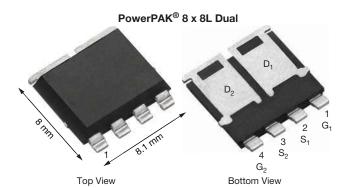
## SQJQ906E

www.vishay.com

ISHA

**Vishay Siliconix** 

## Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET



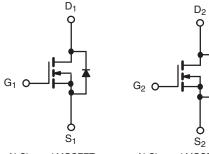
**PRODUCT SUMMARY** V<sub>DS</sub> (V) 40  $R_{DS(on)}(\Omega)$  at  $V_{GS}$  = 10 V 0.0033 I<sub>D</sub> (A) per leg 95 Configuration Dual PowerPAK 8 x 8L Package

#### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>q</sub> and UIS tested
- Fully lead (Pb)-free device
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS COMPLIANT HALOGEN FREE



N-Channel MOSFET



ABSOLUTE MAXIMUM RATINGS	<b>S</b> (T <sub>C</sub> = 25 °C, unless	otherwise noted	i)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	40	v	
Gate-source voltage		V <sub>GS</sub>	± 20	v	
Continuous drain current	$T_{C} = 25 \ ^{\circ}C \ ^{a}$	1	95		
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	55		
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	45	А	
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	300		
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	36		
Single pulse avalanche energy		E <sub>AS</sub>	64	mJ	
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	50	W	
	T <sub>C</sub> = 125 °C		17	vv	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>d, e</sup>			260		

THERMAL RESISTANCE RATINGS								
PARAMETER		SYMBOL	LIMIT	UNIT				
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	100	°C/W				
Junction-to-case (drain)		R <sub>thJC</sub>	3	0/10				

#### Notes

- a. Package limited
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static		-		•	•			
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0, I_D = 250 \ \mu A$		40	-	-	v	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		2.5	3	3.5		
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA	
Zero gate voltage drain current		$V_{GS} = 0 V$	V <sub>DS</sub> = 20 V	-	-	1		
	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	$V_{DS} = 40 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	150		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	40	-	-	А	
Drain-source on-state resistance <sup>a</sup>		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5 A	-	0.0027	0.0033	Ω	
	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}$	I <sub>D</sub> = 5 A, T <sub>J</sub> = 125 °C	-	-	0.0048		
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5 A, T <sub>J</sub> = 175 °C	-	-	0.0056		
Forward Transconductance b	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		-	75	-	S	
Dynamic <sup>b</sup>		·						
Input capacitance	C <sub>iss</sub>			-	2880	3600		
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 20 V, f = 1 MHz		-	1635	2045	pF	
Reverse transfer capacitance	C <sub>rss</sub>	1		-	85	105		
Total gate charge <sup>c</sup>	Qg		V <sub>DS</sub> = 20 V, I <sub>D</sub> = 10 A	-	34	42	nC	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	11	-		
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>	1		-	4	-		
Gate resistance	Rg	f = 1 MHz		0.7	1.1	1.9	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	14	19		
Rise time <sup>c</sup>	tr	$V_{DD} = 20 \text{ V}, \text{ R}_{L} = 2 \Omega$ $\text{I}_{D} \cong 10 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	4	6	- ns	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	26	35		
Fall time <sup>c</sup>	t <sub>f</sub>			-	4	6		
Source-Drain Diode Ratings and Cha	racteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	600	А	
	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0		-	1	1.2	V	

Notes

a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing

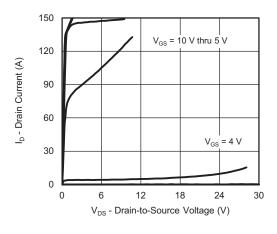
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

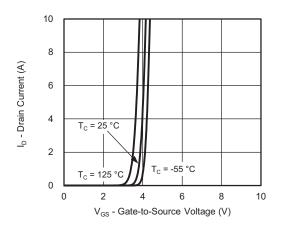
2



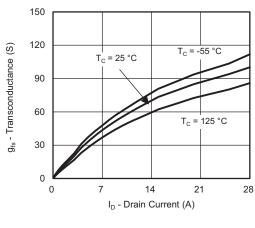
#### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



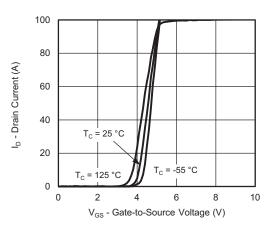
**Output Characteristics** 



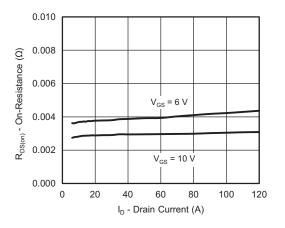
**Transfer Characteristics** 



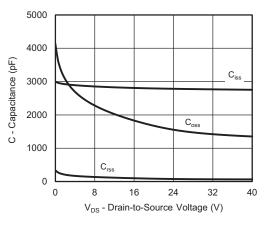
Transconductance



**Transfer Characteristics** 



**On-Resistance vs. Drain Current** 



#### Capacitance

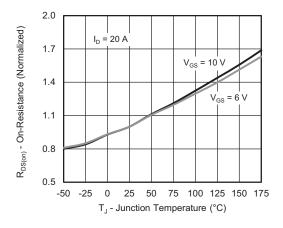
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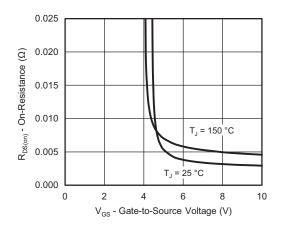
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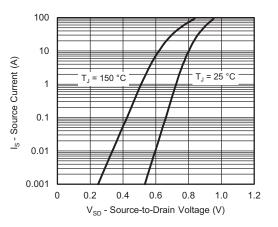
#### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



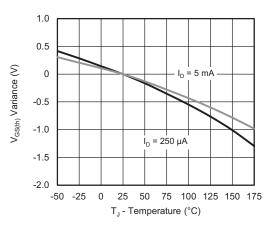
**On-Resistance vs. Junction Temperature** 



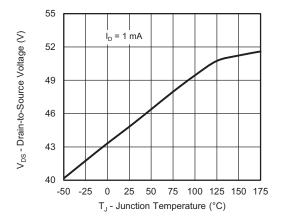
On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage



**Threshold Voltage** 



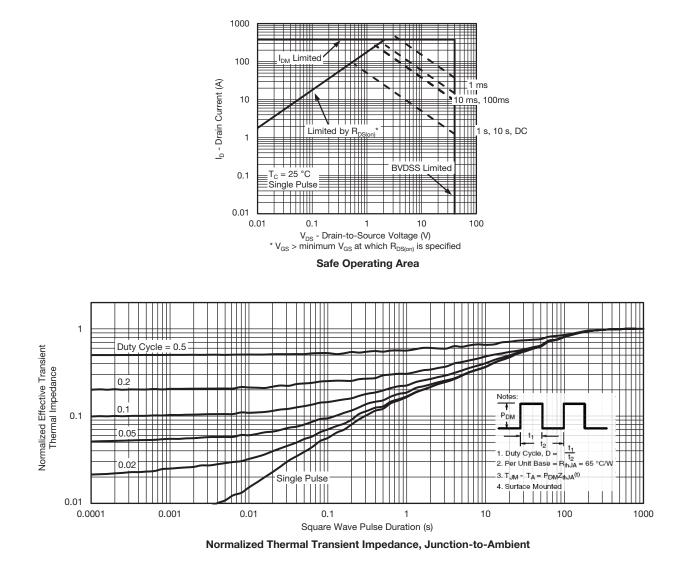
Drain Source Breakdown vs. Junction Temperature

4

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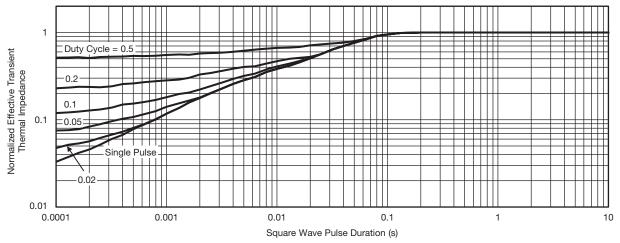
#### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)





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**THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

• The characteristics shown in the two graphs

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- Normalized Transient Thermal Impedance Junction to Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction to Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg?76462</u>.

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