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Adjustable Off-Line Inductorless Switching Regulator

Features

- ▶ Efficient operation without magnetics
- ▶ No high voltage capacitors
- ▶ Adjustable main output voltage (9.0 to 50V)
- ▶ Additional 5.0V internal regulator
- ▶ Up to 100mA combined output current
- ▶ Single BOM for 120VAC/230VAC
- ▶ Built-in soft start
- ▶ Less than 200mW standby power

Applications

- ▶ White goods
- ▶ Household appliances
- ▶ Lighting controls
- ▶ Circuit breakers
- ▶ Keep-alive supplies

General Description

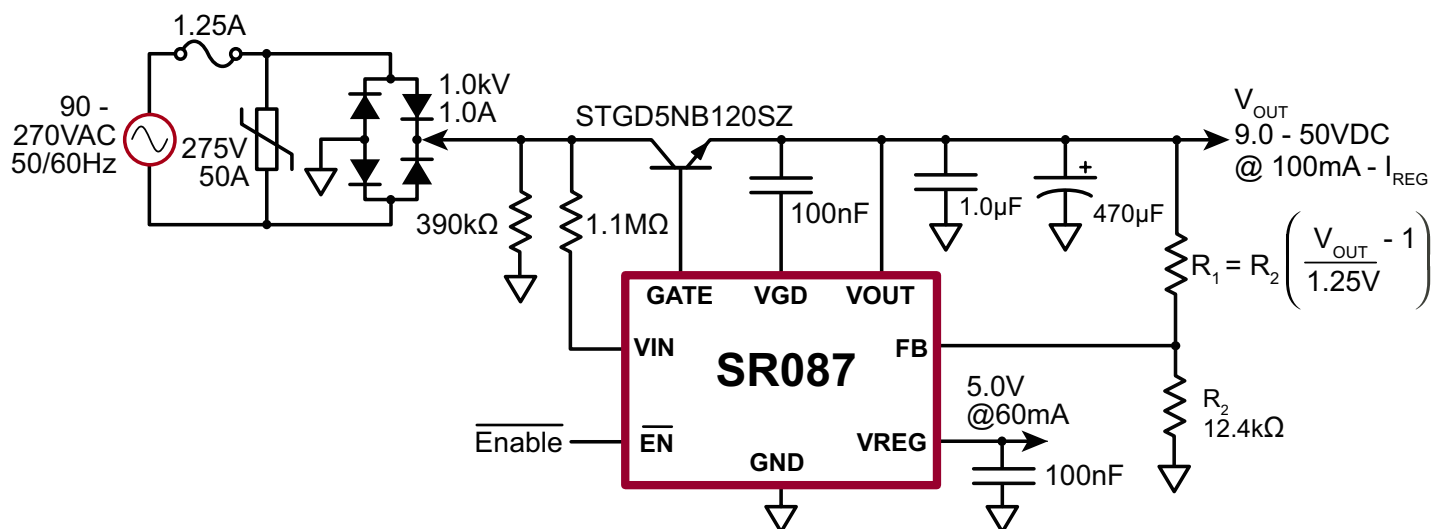
The Supertex SR087 is an inductorless switching regulator designed to operate directly from a rectified AC line. The operating principle is to turn on a pass transistor when the rectified AC is below the output voltage, and to turn it off when the output voltage reaches a specific level. A linear regulator supplied by V_{OUT} provides an additional fixed 5.0V output. Efficiencies of around 55% may be realized for loads up to 1.0W in 120VAC applications, with around 50% efficiencies for loads up to 800mW in 230VAC applications.

A logic-level enable input allows the SR087 to be disabled – useful when it is employed as a keep-alive power supply.

WARNING! Galvanic isolation is not provided. Dangerous voltages are present when connected to the AC line. It is the responsibility of the designer employing the SR087 to ensure adequate safeguards are in place to protect the end user from electrical shock.

The circuits shown in this datasheet are not guaranteed to meet surge and conducted EMI requirements. The effectiveness of these circuits may vary with a particular application. The designer should conduct tests to ascertain compliance with applicable standards and regulations.

Typical Application Circuit



Ordering Information

Part Number	Package Option	Packing
SR087SG-G	8-Lead SOIC Narrow Body w/ Heat Slug	2500/Reel

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
Output voltage (V_{OUT})	-0.3V to 56V
Feedback voltage (V_{FB})	-0.3V to 6.5V
Enable voltage (V_{EN})	-0.3V to 6.5V
Operating junction temperature	-40°C to +125°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
8-Lead SOIC	84°C/W*

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{OUT}	Output voltage	9.0	-	50	V	---
I_{OUT}	Load on V_{OUT} , including feedback divider and load on V_{REG}	100	-	-	μ A	---
V_{HR}	Headroom for internal linear regulator ($V_{OUT} - V_{REG}$)	4.0	-	-	V	---

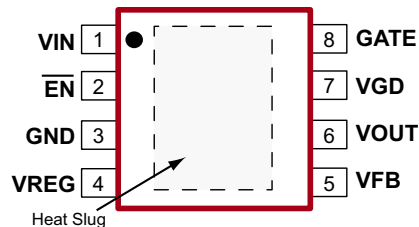
Specifications (Unless otherwise noted, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, Voltages referenced to GND pin)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{GD}	Current consumption at V_{GD}	-	-	60	μ A	---
$I_{OUT(int)}$	Current consumption of the lower circuitry	-	-	400	μ A	$V_{OUT} = 9.0 - 50\text{V}$
V_{GD}	Gate drive supply voltage ¹	11	13	15	V	---
$V_{Gate(hi)}$	Gate output high voltage ¹	11	-	15	V	---
$V_{Gate(lo)}$	Gate output low voltage ¹	-	-	0.5	V	---
$V_{FB(off)}$	Feedback voltage (gate off)	1.18	1.25	1.31	V	---
$V_{FB(hys)}$	Feedback voltage hysteresis	-	50	-	mV	---
I_{FB}	FB input current	-	-	500	nA	---
$V_{TRIP(on)}$	V_{IN} trip voltage (gate on) ¹	0	-	3.0	V	---

Note:

- Referenced to V_{OUT} .

Pin Configuration



8-Lead SOIC

(top view)

Backside on the SOIC package is at ground potential and may be connected to ground or left unconnected.

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
— = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC

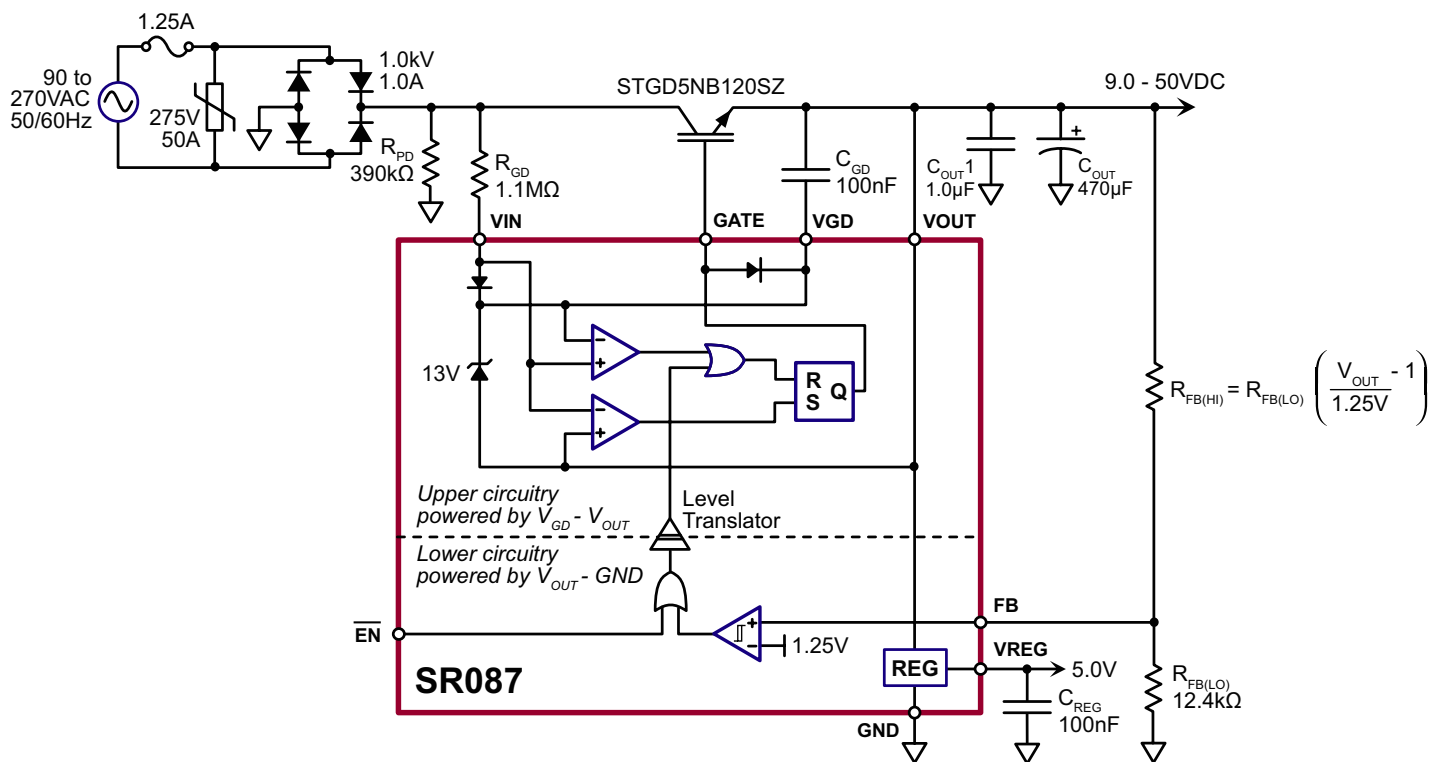
Specifications (cont.)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{TRIP(off)}$	V_{IN} trip voltage, Gate off ¹	9.0	-	15	V	---
$V_{EN(on)}$	Enable voltage, on	0.2	-	-	V	---
$V_{EN(off)}$	Enable voltage, off	-	-	0.75	V_{REG}	---
$t_{DIG(on)}$	V_{IN} – Gate turn-on delay	0	-	1.0	μs	$C_{Gate} = 1.0nF$
$t_{DIG(off)}$	V_{IN} – Gate turn-off delay	-	-	600	ns	$C_{Gate} = 1.0nF$
$t_{DFG(off)}$	FB – Gate turn-off delay	-	-	450	ns	$C_{Gate} = 1.0nF$ $V_{FB} = 1.5V$
V_{REG}	Regulated output voltage	4.750	5.000	5.250	V	$I_{LOAD} = 1.0mA$, $V_{OUT} = 9.0V$
ΔV_{REG}	V_{REG} load regulation	-50	-	+50	mV	$0mA < I_{LOAD} < 60mA$, $V_{OUT} = 9.0V$, $T_{Amb} = 25^{\circ}C$
V_D	Gate – V_{GD} diode drop	-	-	1.0	V	$I = 20mA$

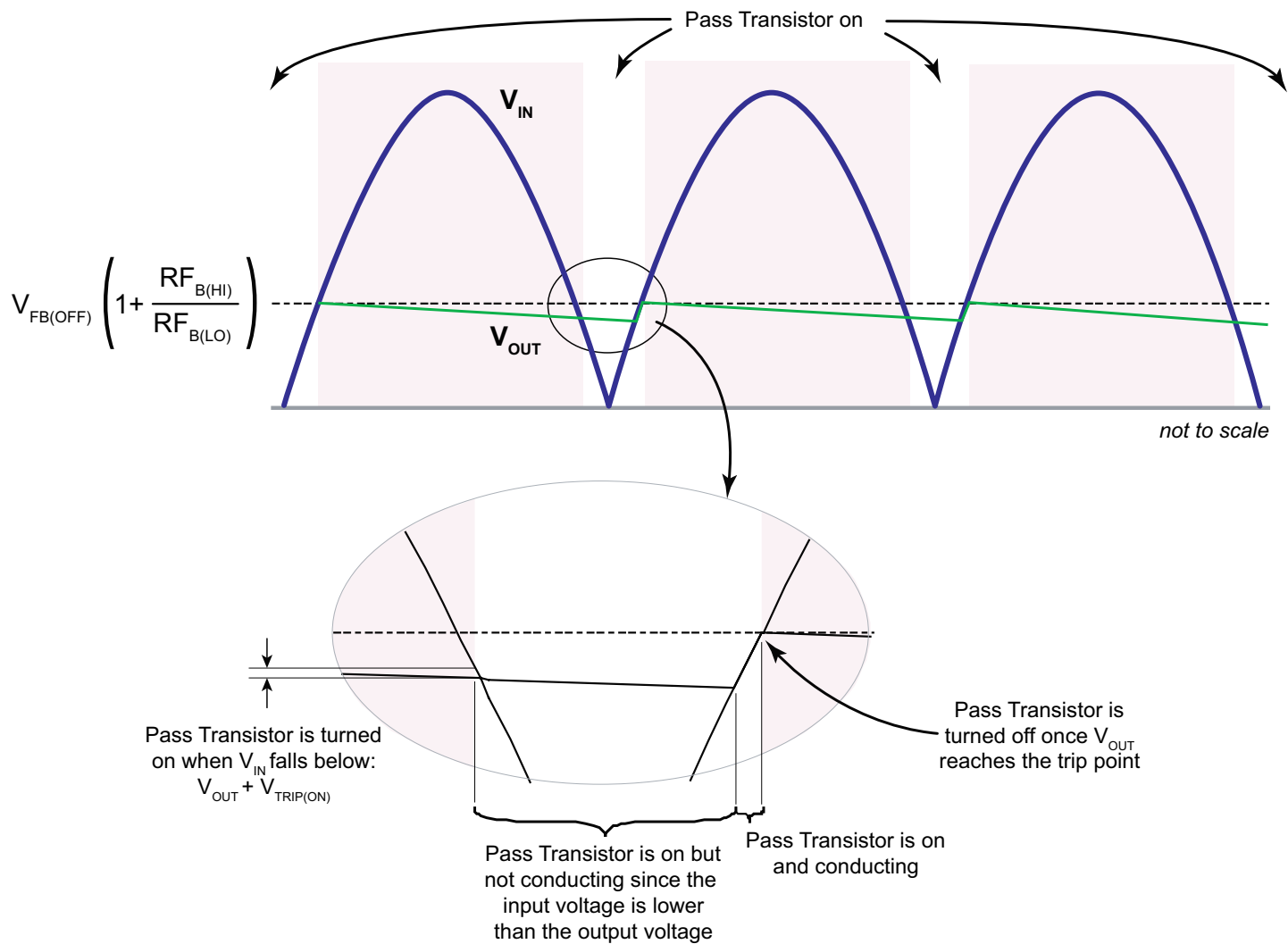
Note:

1. Referenced to V_{OUT} .

Block Diagram

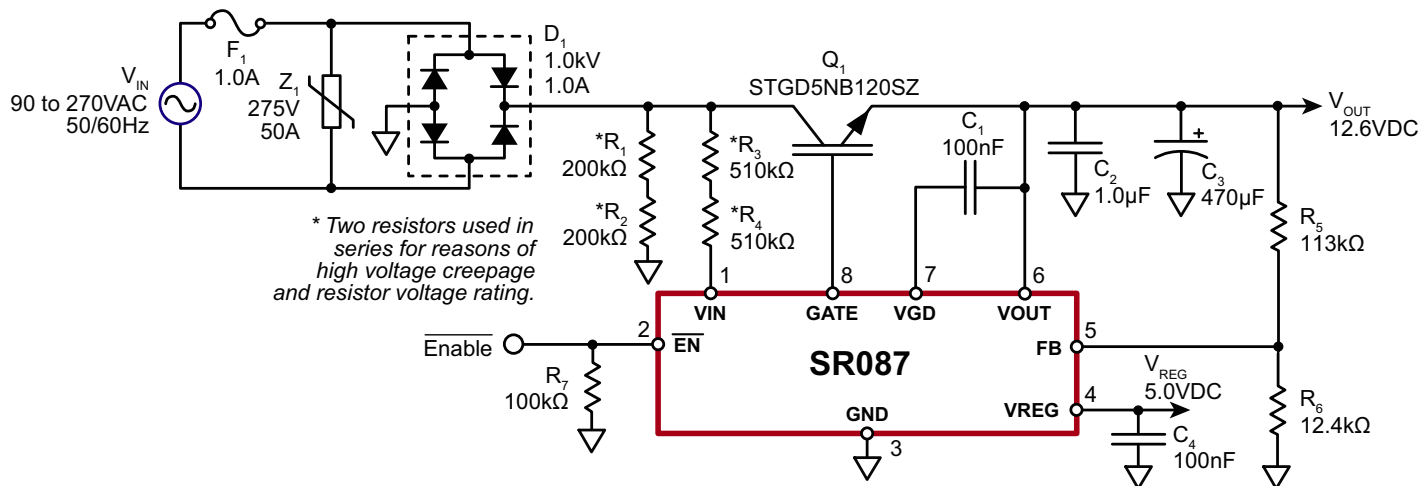


SR087 Timing



Data Sheet Application Section:

Typical Application Circuit



Output Voltage*

V_{OUT} may be adjusted in the range of 9V to 50V*, by changing feedback resistor R_5 according to the following equation.

$$R_5 = R_6 [(V_{OUT} / 1.25V) - 1]$$

Leave R_6 at 12.4k Ω or less - it assures a minimum 100 μ A load required for the proper operation of the SR087. Change R_3 and R_4 according to the R_3+R_4 equation below. Select C_2 and C_3 with appropriate voltage ratings. For C_3 , use a low ESR capacitor with an adequate ripple current rating (800mA_{RMS}). Use ceramic for C_2 .

Since V_{REG} is a linear regulator supplied from V_{OUT} , the maximum current available from V_{REG} is reduced as V_{OUT} is increased due to power considerations.

$$I_{REG(max)} = 1.5W / (V_{OUT} - 5.0V), \text{ or } 60mA, \text{ whichever is less.}$$

Input Voltage

To reduce standby power for 230VAC-only applications, or for supply voltages less than 90Vrms, R_3 and R_4 should be changed according to the R_3+R_4 equation below. R_1+R_2 should remain at 400k Ω or less. Two resistors in series are employed to ensure adequate creepage distances for 230VAC operation. For 120VAC-only applications, single resistors may be employed.

Output Ripple*

Storage capacitor C_3 was sized to provide about 2V_{P-P} ripple at 100mA load ($I_{OUT} + I_{REG}$). For lighter loads, C_3 may be reduced. Conversely, C_3 may be increased for lower ripple. Use a low ESR capacitor with an adequate ripple current rating (800mA_{RMS} for 100mA loads). Efficiency and output current capability may drop with increased capacitance because of a smaller conduction angle associated with lower ripple. Due to feedback hysteresis, ripple cannot be reduced below 4%.

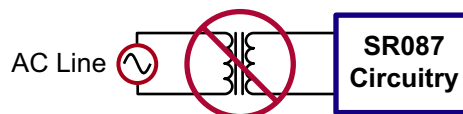
$$V_{RIPPLE(P-P)} \approx (I_{OUT} + I_{REG}) / 2f_{IN} C_3$$

* V_{REG} requires at least 4.0V of headroom. Therefore, V_{OUT} including ripple, must not fall below 9.0V.

Line Transformer

During initial testing it is tempting to use an isolation transformer or a variable transformer on the AC line. However, the high inductance of the transformer (frequently in the

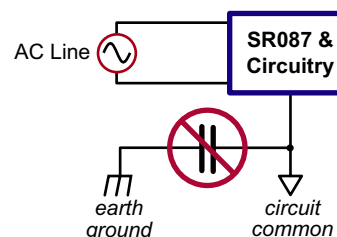
mH's) interferes with the normal operation of the SR087 and should not be used. This is not a concern with the normal inductance of the AC line or for AC line filters.



The SR087 draws current from the AC line in short, high current pulses. The transformer's high inductance tends to limit the current pulse. Furthermore, inductive kickback on the falling edge of the current pulse can create high voltage spikes which must be absorbed by the transient protector.

EMI Capacitor

The use of a small-value capacitor from circuit common to earth ground prevents the SR087 from operating and should not be employed.



EMI

The SR087 circuit as depicted on Page 1, (Typical Application Circuit), meets FCC Class B and CISPR 14-1 (household appliances) requirements for conducted emissions, for combined loads of less than 20mA ($I_{OUT} + I_{REG}$).

Fuse

Although the average current drawn from the AC line is low, the RMS current is fairly high due to the current being drawn in short, high-current pulses. Since a fuse is basically a resistor with a power dissipation given by $I_{RMS}^2 R$, the fuse must be sized for the RMS current, not the average current. For a 1.0W load and 120VAC the RMS current is 700mA_{RMS}, and for a 0.5W load at 230VAC it is 360mA_{RMS}.

Load

Total load on the SR087 is the total load current drawn from V_{OUT} (I_{OUT}) and, since the linear regulator is supplied from V_{OUT} , it also includes the current drawn from V_{REG} (I_{REG}). Total

$R_3 + R_4$ Equation:

$$(R_3 + R_4) < \frac{\sqrt{2V_{IN}^2 - V_X^2} - V_X \cos^{-1} \left(\frac{V_X}{\sqrt{2} \cdot V_{IN}} \right)}{\pi \cdot 25\mu} \quad \text{where } V_X = V_{OUT} + 15V$$

Use the minimum anticipated RMS value for V_{IN} . Take resistor tolerance into account, selecting the next lower standard value. Choosing a lower value has no effect other than higher standby power.

load is calculated as follows:

$$I_{LOAD} = I_{OUT} + I_{REG}$$

$$P_{LOAD} = V_{OUT} (I_{OUT} + I_{REG})$$

UPS

The SR087 will not operate from uninterruptable power supplies having a square wave output. This type of output is usually referred to as 'modified sine wave'.

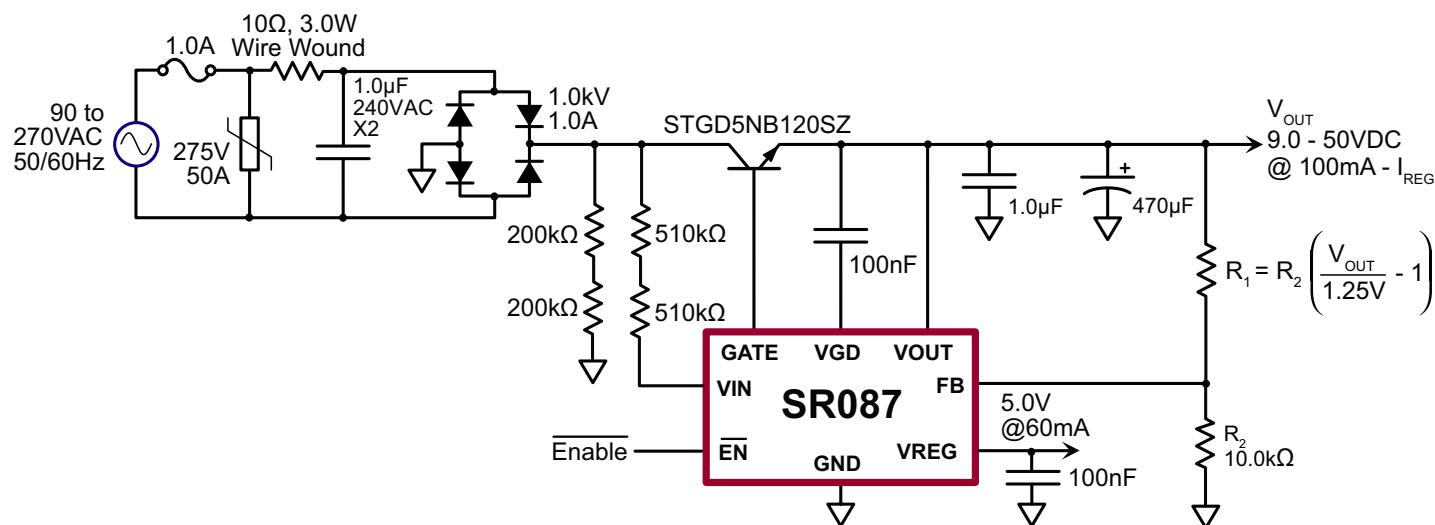
Transient Protection

The transient protector must be located before the bridge rectifier. The reason for this is to minimize capacitance to allow the rectified AC to fall below V_{OUT} .

Since there is no capacitor to absorb AC line transients, complete transient protection must be provided by the TVS or MOV device. Since the recommended IGBT is rated at 1.2kV and the SR087 never sees the full input voltage, the bridge rectifier becomes the limiting element when selecting an MOV. If using a 1.0kV bridge, an MOV having a clamping voltage of < 1.0kV is recommended.

An RC network on the AC line, as shown in the circuit below, affords additional protection from line transients, as well as reducing conducted EMI. It does, however, reduce power supply efficiency.

Additional Transient Protection

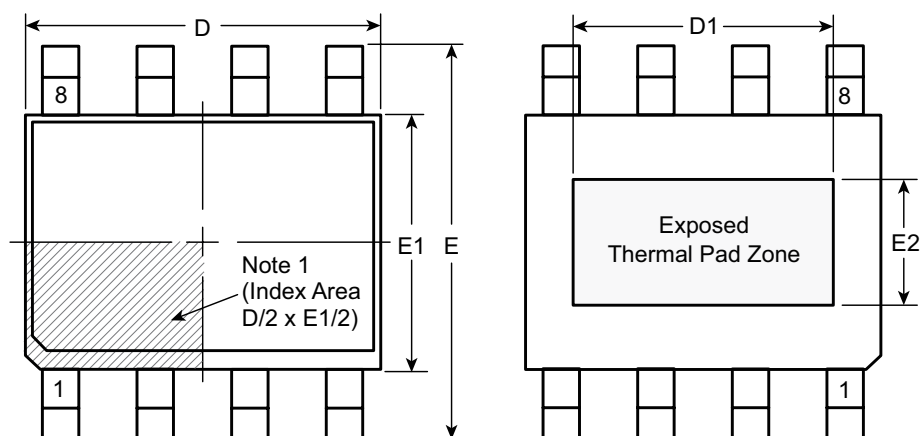


Pin Description

Name	Pin	Description
VIN	1	Rectified AC input voltage
\overline{EN}	2	Active low enable input
GND	3	Circuit ground <i>Note: circuit ground will be at the AC line potential</i>
VREG	4	Regulated output voltage, fixed 5.0V
FB	5	Feedback input
VOUT	6	Output voltage (9.0 - 50V adj.)
VGD	7	Gate drive supply (referenced to V_{OUT})
GATE	8	Drives external IGBT pass transistor

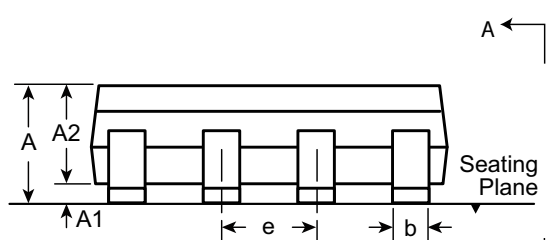
8-Lead SOIC (Narrow Body w/Heat Slug) Package Outline (SG)

4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch

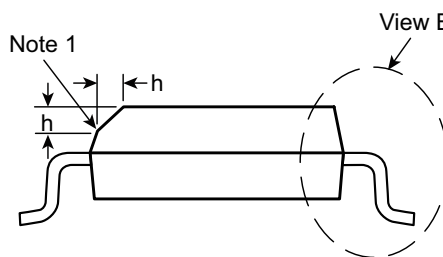


Top View

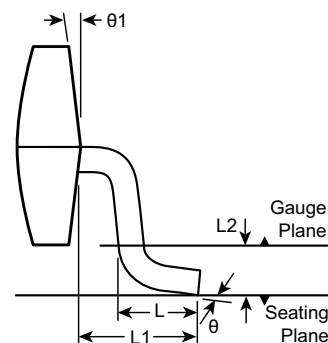
Bottom View



Side View



View A-A



View B

Notes:

- If optional chamfer feature is not present, a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	E2	e	h	L	L1	L2	θ	$\theta 1$		
Dimension (mm)	MIN	1.25*	0.00	1.25	0.31	4.80*	3.30 [†]	5.80*	3.80*	2.29 [†]	1.27 BSC	0.25	0.40	1.04 REF	0.25	5°		
	NOM	-	-	-	-	4.90	-	6.00	3.90	-		-	-		-	-	-	-
	MAX	1.70	0.15	1.55*	0.51	5.00*	3.81 [†]	6.20*	4.00*	2.79 [†]		0.50	1.27		0.25	8°	15°	

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-8SOSG, Version D041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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