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SSL4120T

Resonant power supply control IC with PFC

Rev. 1 — 21 June 2012 Objective data sheet

1. General description

The SSL4120T integrates a Power Factor Corrector (PFC) controller and a controller for a Half-Bridge resonant Converter (HBC) in a multi-chip IC. It provides the drive function for the discrete MOSFET in an up-converter and for the two discrete power MOSFETs in a resonant half-bridge configuration.

The efficient operation of the PFC is achieved by implementing functions such as quasi-resonant operation at high power levels and quasi-resonant operation with valley skipping at lower power levels. OverCurrent Protection (OCP), OverVoltage Protection (OVP), and demagnetization sensing ensure safe operation under all conditions.

The HBC module is a is a high-voltage controller for a zero-voltage switching LLC resonant converter. It contains a high-voltage level shift circuit and several protection circuits including OCP, open-loop protection, capacitive mode protection and a general purpose latched protection input.

The high-voltage chip is fabricated using a proprietary high-voltage Bipolar-CMOS-DMOS power logic process that enables efficient direct start-up from the rectified universal mains voltage. The low-voltage Silicon On Insulator (SOI) chip is used for accurate, high-speed protection functions and control.

The topology of a PFC circuit and a resonant converter controlled by the SSL4120T is very flexible, enabling it to be used in a broad range of applications with a wide mains voltage range. Combining PFC and HBC controllers in a single IC makes the SSL4120T ideal for controlling power supplies in LCD and plasma televisions.

Highly efficient and reliable power supplies providing over 100 W can be designed easily using the SSL4120T, with a minimum of external components.

2. Features and benefits

2.1 General features

- Integrated PFC and HBC controllers
- Universal mains supply operation (70 V to 276 V (AC))
- High level of integration resulting in a low external component count and a cost effective design
- Enable input (enable only PFC or both PFC and HBC controllers)
- On-chip high-voltage start-up source
- Stand-alone operation or IC supplied from external DC source

2.2 PFC controller features

- Boundary mode operation with on-time control
- Valley/zero voltage switching for minimum switching losses
- Frequency limiting to reduce switching losses
- Accurate boost voltage regulation
- Burst mode switching with soft-start and soft-stop

2.3 HBC controller features

- Integrated high-voltage level shifter
- Adjustable minimum and maximum frequency
- Maximum 500 kHz half-bridge switching frequency
- Adaptive non-overlap time
- Burst mode switching

2.4 Protection features

- Safe restart mode for system fault conditions
- General latched protection input for output overvoltage protection or external temperature protection
- Protection timer for time-out and restart
- Overtemperature protection
- Soft (re)start for both controllers
- Undervoltage protection for mains (brownout), boost, IC supply and output voltage
- Overcurrent regulation and protection for both controllers
- Accurate overvoltage protection for boost voltage
- Capacitive mode protection for HBC controller

3. Applications

The device can be used in all LED lighting applications that require very efficient, low Total Harmonic Distortion (THD), high power-factor, true universal input voltage and cost-effective power supply solution between 10 W and 300 W."

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SSL4120T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

5. Block diagram

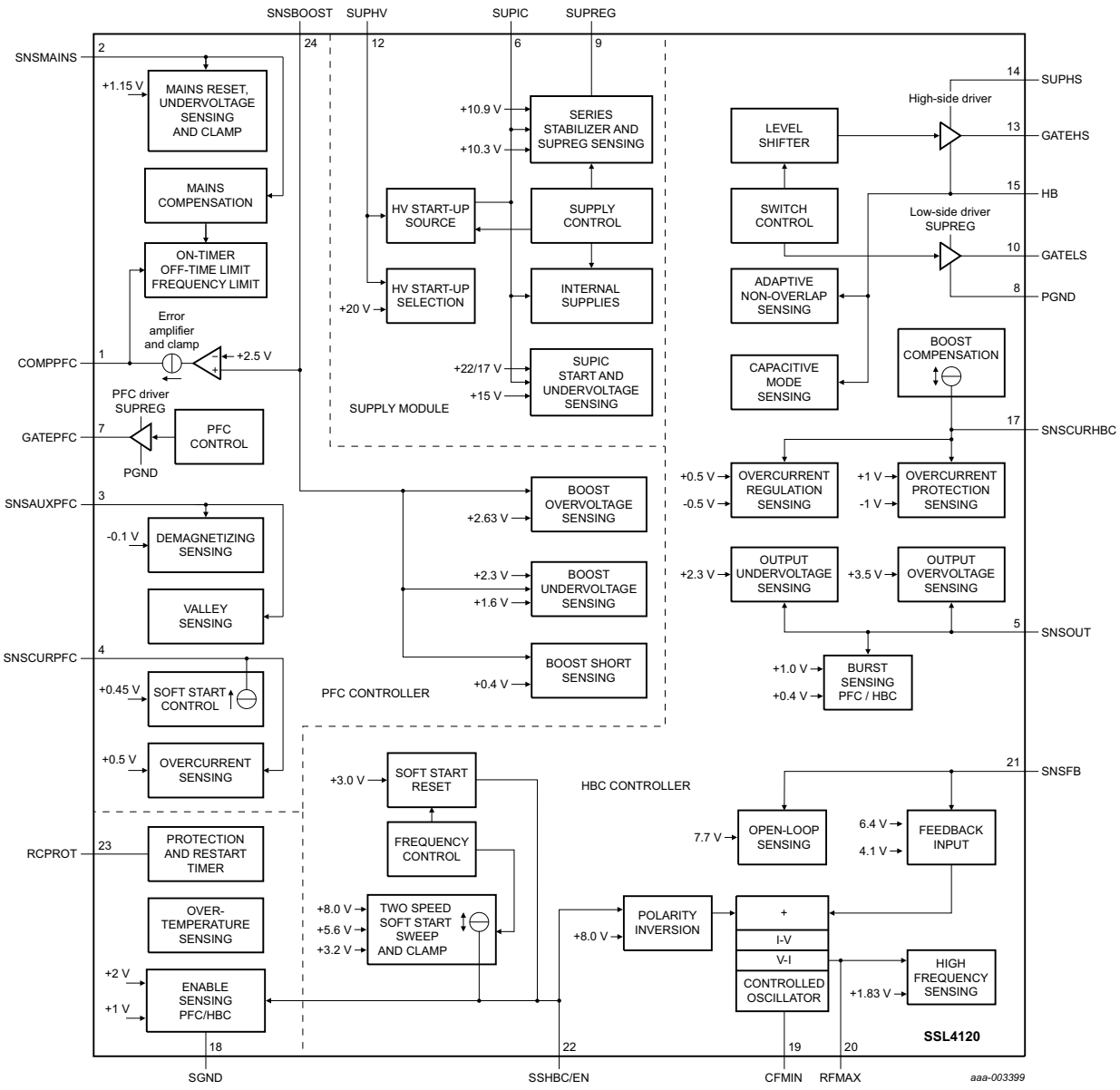


Fig 1. Block diagram of SSL4120T

6. Pinning information

6.1 Pinning

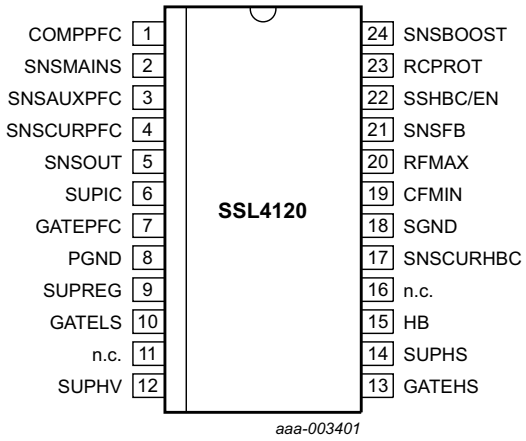


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
COMPPFC	1	frequency compensation for PFC controller; externally connected to filter
SNSMAINS	2	sense input for mains voltage; externally connected to resistive divided mains voltage
SNSAUXPFC	3	sense input for PFC demagnetization timing; externally connected to auxiliary winding of PFC
SNSCURPFC	4	sense input for momentary current and soft start of the PFC controller; externally connected to current sense resistor and soft start filter
SNSOUT	5	sense input for monitoring the output voltage of the HBC; externally connected to the auxiliary winding; sense input for burst mode of HBC controller or PFC and HBC controllers
SUPIC	6	low-voltage supply for SUPIC input; output of internal HV start-up source; externally connected to auxiliary winding of HBC or to external DC supply
GATEPFC	7	gate driver output for PFC MOSFET
PGND	8	power ground; reference (ground) for HBC low-side and PFC driver
SUPREG	9	regulated SUPREG IC supply; output from internal regulator; input for drivers; externally connected to SUPREG buffer capacitor
GATELS	10	gate driver output for low-side MOSFET of HBC
n.c.	11	not connected; high-voltage spacer.
SUPHV	12	high-voltage supply input for internal HV start-up source; externally connected to boost voltage
GATEHS	13	gate driver output for high-side MOSFET of HBC
SUPHS	14	high-side driver supply input; externally connected to bootstrap capacitor (C_{SUPHS})

Table 2. Pin description *...continued*

Symbol	Pin	Description
HB	15	reference for high-side driver; input for half-bridge slope detection; externally connected to half-bridge node HB between HBC MOSFETs (see Figure 19)
n.c.	16	not connected; high-voltage spacer
SNSCURHBC	17	sense input for momentary HBC current; externally connected to resonant current sense resistor
SGND	18	signal ground; reference (ground) for IC.
CFMIN	19	minimum frequency setting for HBC; externally connected to capacitor
RFMAX	20	maximum frequency setting for HBC; externally connected to resistor
SNSFB	21	sense input for output voltage regulation feedback; externally connected to opto-coupler
SSHBC/EN	22	combined soft start timing of HBC and IC enable input; enabling of PFC or PFC and HBC controllers; externally connected to soft start capacitor and enable pull-down signal
RCPROT	23	protection timer setting for time-out and restart; externally connected to resistor and capacitor
SNSBOOST	24	sense input for boost voltage; externally connected to resistive divided boost voltage

7. Functional description

7.1 Overview of IC modules

The functionality of the SSL4120T can be grouped as follows:

- Supply module:

  Supply management for the IC; includes the restart and (latched) shut-down states
- Protection and restart timer:

  Externally adjustable timer used for delayed protection and restart timing
- Enable input:

  Control input for enabling and disabling the controllers; very low current consumption when disabled
- PFC controller:

  Controls and protects the power factor converter; generates a 400 V (DC) boost voltage from the rectified AC mains input with a high power factor
- HBC controller:

  Controls and protects the resonant converter; generates a regulated (mains isolated) output voltage from the 400 V (DC) boost voltage

Figure 1 shows the block diagram of the SSL4120T. A typical application is illustrated in Figure 19.

7.2 Power supply

The SSL4120T contains several supply related pins.

7.2.1 Low-voltage supply input (pin SUPIC)

The SUPIC pin is the main low-voltage supply input to the IC. All internal circuits (other than the high voltage circuit) are directly or indirectly (via SUPREG) supplied from this pin. SUPIC is connected externally to a buffer capacitor C_{SUPIC}. This buffer capacitor can be charged in several ways:

- from the internal high voltage start-up source
- from the auxiliary winding of the HBC transformer
- from the capacitive supply of the switching half-bridge node
- from an external DC supply, e.g. a standby supply

The IC starts operating when voltage on SUPIC reaches the start level, provided that the voltage on SUPREG has also reached the start level. The start level depends on the condition of the SUPHV pin:

- High voltage present on SUPHV, $V_{SUPHV} > V_{det(SUPHV)}$.

  This is the case with a stand-alone application where C_{SUPIC} is initially charged from the HV start-up source. The start level is $V_{start(hvd)(SUPIC)}$ (typ. 22 V). The wide difference between the start and stop ($V_{uvp(SUPIC)}$) levels allows energy to be stored in the SUPIC buffer capacitor which is used to supply the IC until the output voltage has stabilized.
- Not connected or no voltage present at SUPHV, $V_{SUPHV} < V_{det(SUPHV)}$.

  This is the case when the SSL4120T is supplied from an external DC source. The start level is $V_{start(nohvd)(SUPIC)}$ (typ. 17 V). The IC is supplied from the DC supply during start-up. To minimize power dissipation, the DC supply to pin SUPIC should be above, but close to, $V_{uvp(SUPIC)}$ (typ. 15 V).

The IC will stop operating when V_{SUPIC} drops below $V_{uvp(SUPIC)}$. This is the SUPIC UnderVoltage Protection (UVP) voltage (UVP-SUPIC; see Section 7.9). The PFC controller will stop switching immediately, but the HBC controller will continue operating until the low-side MOSFET becomes active.

The current consumption depends on the state of the IC. The SSL4120T operating states are described in Section 7.3.

- Disabled IC state

  When the IC is disabled via the SSHBC/EN pin, the current consumption is very low ($I_{dism(SUPIC)}$).
- SUPIC charge, SUPREG charge, Thermal hold, Restart and Protection shut-down states

  Only a small section of the IC is active while C_{SUPIC} and C_{SUPREG} are charging during a restart sequence prior to start-up or during shut-down after a protection function has been activated. The PFC and HBC controllers are disabled. Current consumption is limited to $I_{protm(SUPIC)}$.

- Boost charge state

  The PFC controller is switching; the HBC controller is off. The current from the high voltage start-up source is large enough to supply SUPIC (current consumption < $I_{ch(nom)(SUPIC)}$).
- Operational supply state

  Both the PFC and HBC controllers are switching. Current consumption is $I_{oper(SUPIC)}$. When the HBC controller is enabled, the switching frequency will be high initially and the current consumption of the HBC MOSFET drivers will be dominant. The stored energy in C_{SUPIC} will supply the initial SUPIC current before the SUPIC supply source takes over.

Pin SUPIC has a low short-circuit detection voltage ($V_{scp(SUPIC)}$; typ. 0.65 V). The current dissipated in the HV start-up source is limited while $V_{SUPIC} < V_{scp(SUPIC)}$ (see Section 7.2.4).

7.2.2 Regulated supply (pin SUPREG)

The voltage range on pin SUPIC exceeds that of the gate voltages of the external MOSFETs. For this reason, the SSL4120T contains an integrated series stabilizer. The series stabilizer creates an accurate regulated voltage ($V_{reg(SUPREG)}$; typ. 10.9 V) at the buffer capacitor C_{SUPREG}. This stabilized voltage is used to:

- supply the internal PFC driver
- supply the internal low-side HBC driver
- supply the internal high-side driver via external components
- as a reference voltage for optional external circuits

The SUPREG series stabilizer is enabled after C_{SUPIC} has been fully charged. This ensures that any optional external circuitry connected to SUPREG will not dissipate any of the start-up current.

To ensure that the external MOSFETs receive sufficient gate drive current, the voltage on SUPREG must reach $V_{start(SUPREG)}$ (and the voltage on SUPIC must reach the start level) before the IC starts operating.

SUPREG is provided with undervoltage protection (UVP-SUPREG; see Section 7.9). When V_{SUPREG} falls below $V_{uvp(SUPREG)}$ (typ. 10.3 V), two events will be triggered:

- The IC will stop operating to prevent unreliable switching because the gate driver voltage is too low. The PFC controller will stop switching immediately, but the HBC controller will continue until the low-side stroke is active.
- The maximum current from the internal SUPREG series stabilizer is reduced to $I_{ch(red)(SUPREG)}$ (typ. 5.4 mA). This will reduce the dissipation in the series stabilizer in the event of an overload at SUPREG while SUPIC is supplied from an external DC source.

7.2.3 High-side driver floating supply (pin SUPHS)

The high-side driver is supplied by an external bootstrap buffer capacitor, C_{SUPHS}. The bootstrap capacitor is connected between the high-side reference pin HB and the high-side driver supply input pin SUPHS. C_{SUPHS} is charged from pin SUPREG via an

external diode D_{SUPHS}. The voltage drop between SUPREG and SUPHS can be minimized by carefully selecting the appropriate diode, especially when using large MOSFETs and high switching frequencies.

7.2.4 High voltage supply input (pin SUPHV)

In a stand-alone power supply application, this pin is connected to the boost voltage. C_{SUPIC} and C_{SUPREG} will be charged by the HV start-up source (which delivers a constant current from SUPHV to SUPIC) via this pin.

Short-circuit protection on pin SUPIC (SCP-SUPIC; see Section 7.9) limits the dissipation in the HV start-up source when SUPIC is shorted to ground and limits the current on SUPHV (to $I_{red(SUPHV)}$) as long as the voltage on SUPIC is below $V_{scp(SUPIC)}$.

Under normal operating conditions, the voltage on pin SUPIC will exceed $V_{scp(SUPIC)}$ very quickly after start-up and the HV start-up source will switch to the nominal current $I_{nom(SUPHV)}$.

During start-up and restart, the HV start-up source will charge C_{SUPIC} and regulate the voltage on SUPIC by hysteretic control. So the start level has a small degree of hysteresis $V_{start(hys)(SUPIC)}$. The HV start-up source switches-off when V_{SUPIC} exceeds the start level $V_{start(hvd)(SUPIC)}$. Current consumption through pin SUPHV will be low ($I_{tko(SUPHV)}$).

Once start-up is complete and the HBC controller is operating, SUPIC can be supplied from the auxiliary winding of the HBC transformer. In this operational state, the HV start-up source is disabled.

7.3 Flow diagram

The operation of the SSL4120T can be divided into a number of states - see Figure 3. The abbreviations used in Figure 3 are explained In Table 8.

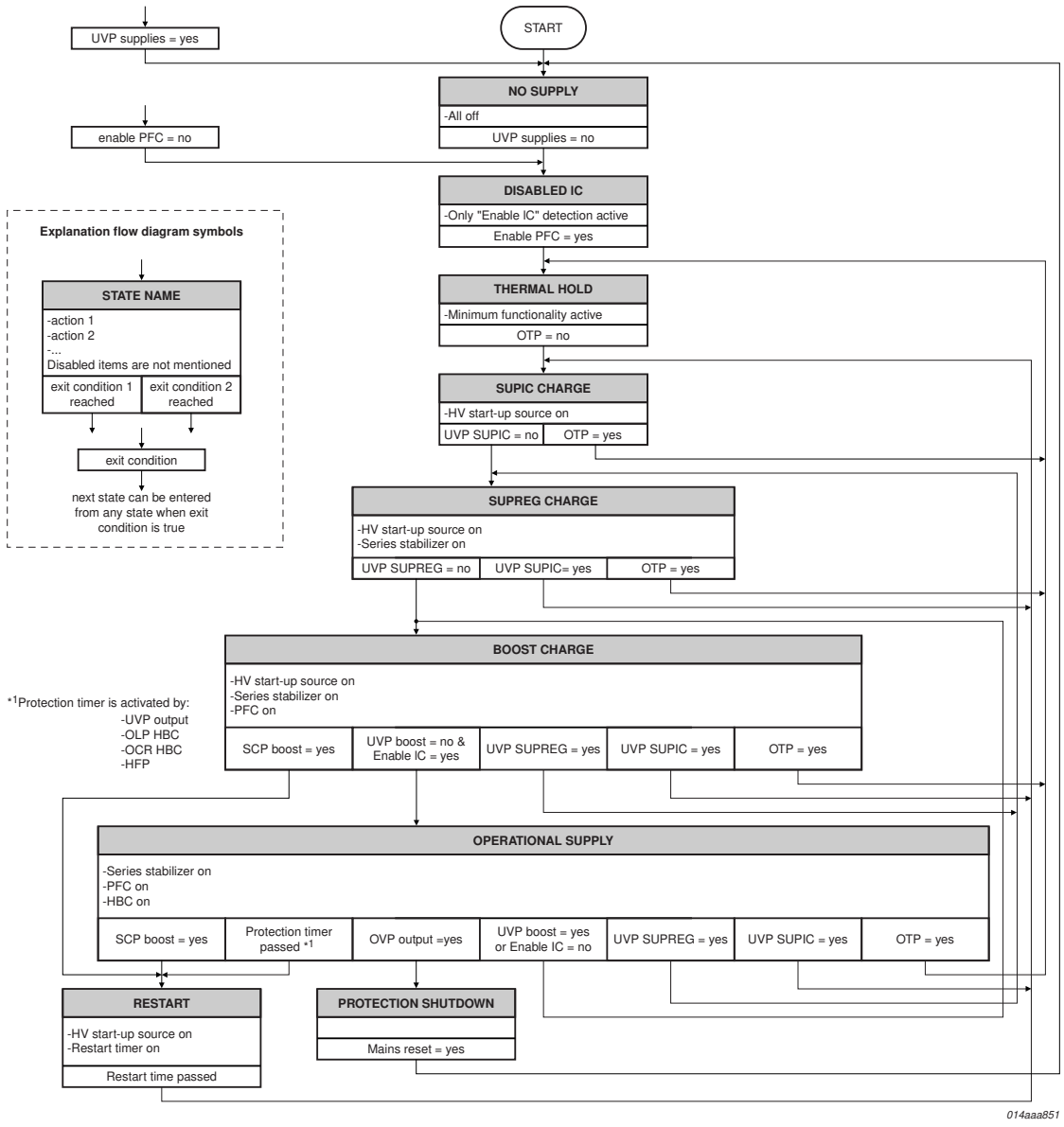


Fig 3. Flow diagram of the SSL4120T

Table 3. Operating states

State	Description
No supply	Supply voltages on SUPIC and SUPHV are too low to provide any functionality. Undervoltage protection (UVP-supplies; see Section 7.9) is active when $V_{SUPHV} < V_{rst(SUPHV)}$ and $V_{SUPIC} < V_{rst(SUPIC)}$. The IC is reset.
Disabled IC	IC is completely disabled because pin SSHBC/EN is LOW.
Thermal hold	Activated as long as OTP is active. IC is not operating. PFC and HBC controllers are disabled and C_{SUPIC} and C_{SUPREG} are not charged.
SUPIC charge	IC supply capacitor (C_{SUPIC}) is charged by HV start-up source. C_{SUPREG} is not charged.
SUPREG charge	Stabilized supply capacitor (C_{SUPREG}) is charged by series regulator.

Table 3. Operating states *...continued*

State	Description
Boost charge	Boost voltage is built up by operational PFC.
Operational supply	Output voltage is generated. Both PFC and HBC controllers are fully operational.
Restart	Activated when a protection function is triggered. Restart timer is activated. During this time, PFC and HBC controllers are disabled and C_{SUPREG} is not charged. C_{SUPIC} is charged.
Protection shut-down	Activated when a protection function is triggered. IC is not operational. PFC and HBC controllers are disabled and C_{SUPIC} and C_{SUPREG} are not charged.

7.4 Enable input (pin SSHBC/EN)

The power supply application can be completely disabled by pulling pin SSHBC/EN LOW.

Figure 4 illustrates the internal functionality. When a voltage is present on pin SUPHV or on pin SUPIC, a current $I_{pu(EN)}$ (typ. 42 µA) flows out of SSHBC/EN. If the pin is not pulled-down, this current will lift the voltage up to $V_{pu(EN)}$ (typ. 3 V). Since this voltage is above both $V_{en(PFC)(EN)}$ (typ. 1.2 V) and $V_{en(IC)(EN)}$ (typ. 2.2 V), the IC will be completely enabled.

The IC can be completely disabled by pulling the voltage on SSHBC/EN down below both $V_{en(PFC)(EN)}$ and $V_{en(IC)(EN)}$ via an opto-coupler driven from the secondary side of the HBC transformer (see Figure 4). The PFC controller will stop switching immediately, but the HBC controller will continue switching until the low-side stroke is active. It is also possible to control the voltage on SSHBC/EN from another circuit on the secondary side via a diode. The external pull-down current must be larger than the internal soft start charge current $I_{ss(hf)(SSHBC)}$.

If the voltage on SSHBC/EN is pulled down below $V_{en(IC)(EN)}$, but not below $V_{en(PFC)(EN)}$, only the HBC will be disabled. This feature can be useful when another power converter is connected to the boost voltage of the PFC.

The low-side power switch of the HBC will be on when the HBC is disabled via the SSHBC/EN pin.

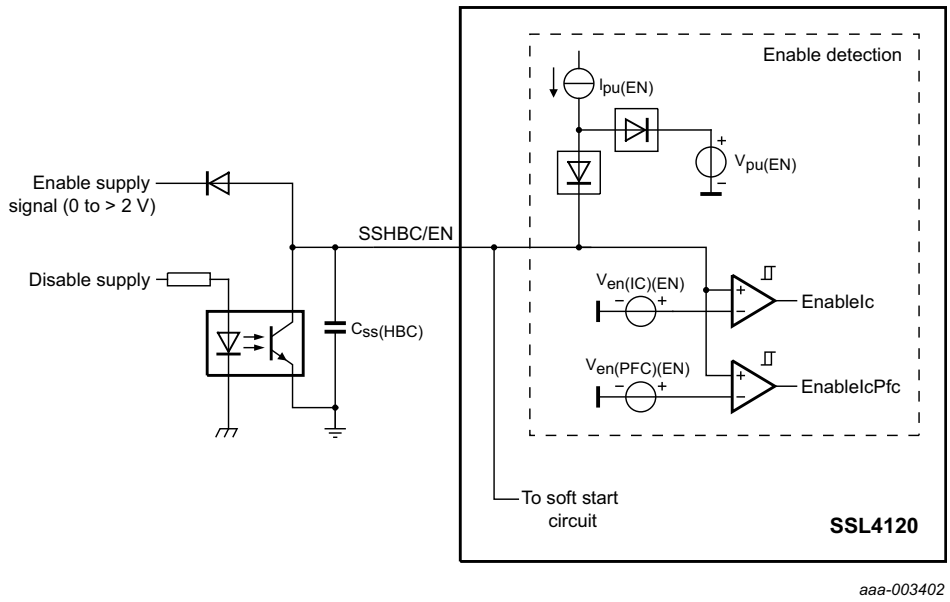


Fig 4. Circuit configuration around pin SSHBC/EN

7.5 IC protection

7.5.1 IC restart and shut-down

In addition to the protection functions that influence the operation of the PFC and HBC controllers, a number of protection functions are provided that disable both controllers. See the protection overview in Section 7.9 for details on which protections trigger a restart or a protection shut-down.

- Restart

  When the SSL4120T enters the Restart state, the PFC and HBC controllers are switched off. After a period defined by the Restart timer, the IC automatically restarts following the normal start-up cycle.

- Protection shut-down

  When the SSL4120T enters the Protection shut-down state, the PFC and HBC controllers are switched off. The Protection shut-down state is latched, so the IC will not start up again automatically. It can be restarted by resetting the Protection shut-down state in one of the following ways:

  – by lowering V_{SUPIC} and V_{SUPHV} below their respective reset levels, $V_{rst(SUPIC)}$ and $V_{rst(SUPHV)}$
  – via a fast shut-down reset (see Section 7.5.3).
  – via the enable pin (see Section 7.4)

- Thermal hold

  In the Thermal hold state, the PFC and HBC controllers are switched off. The Thermal hold state remains active until the IC junction temperature drops to about 10 °C below T_{otp} (see Section 7.5.6).

7.5.2 Protection and restart timer

The SSL4120T contains a programmable timer which can be used for timing several protection functions. The timer can be used in two ways - as a protection timer and as a restart timer. The timing of the timers can be set independently via an external resistor R_{prot} and capacitor C_{prot} connected to pin RCPROT.

7.5.2.1 Protection timer

Certain error conditions can be allowed to persist for a period of time before protective action needs to be taken. The protection timer defines the protection period - how long the error is allowed to persist before the protection function is triggered. The protection functions that use the protection timer can be found in the protection overview in Section 7.9.

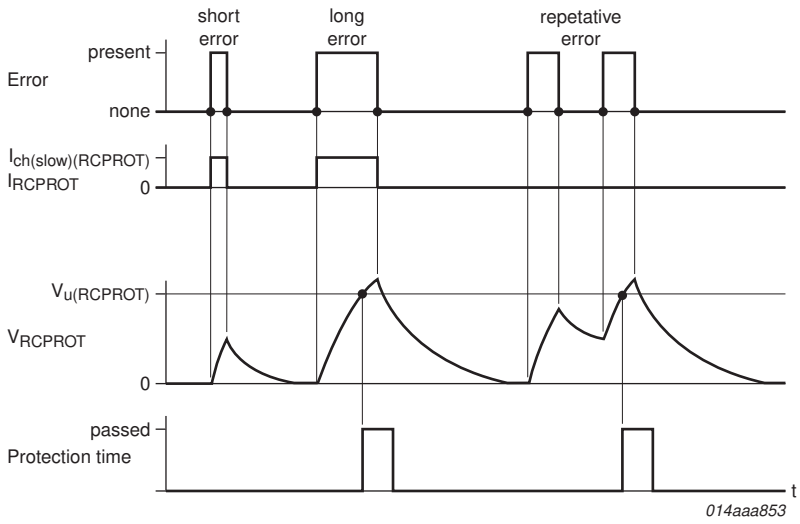


Fig 5. Operation of the protection timer

Figure 5 shows the operation of the protection timer. When an error condition occurs, a fixed current $I_{ch(slow)(RCPROT)}$ (typ. 100 µA) flows out of the RCPROT pin and charges C_{prot}. R_{prot} will cause the voltage to rise exponentially. The protection time has elapsed when the voltage on RCPROT reaches the upper switching level $V_{u(RCPROT)}$ (typ. 4 V). At this instant, the appropriate protective action is taken and C_{prot} is discharged.

If the error condition is removed before the voltage on RCPROT reaches $V_{u(RCPROT)}$, C_{prot} is discharged via R_{prot} and no action is taken.

The voltage on RCPROT may be raised above $V_{u(RCPROT)}$ by an external circuit to force a restart.

7.5.2.2 Restart timer

Certain error conditions require the IC to be disabled for a period of time, particularly when the error condition can cause components to overheat. In such cases, the IC should be disabled to allow the power supply to cool down, before restarting automatically. The restart time is determined by the restart timer. The restart timer is active in the Restart state. The protection functions that trigger a restart can be found in the protection overview in Section 7.9.

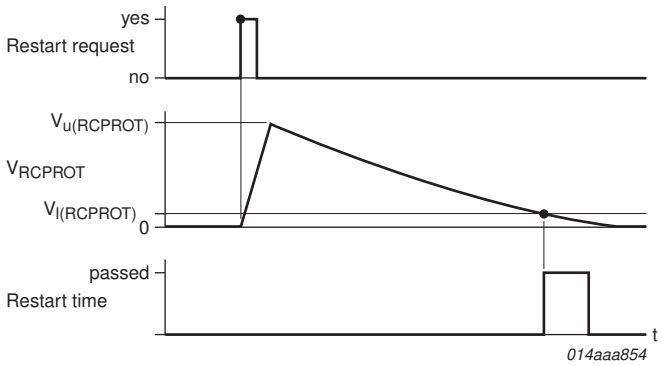


Fig 6. Operation of the restart timer

Figure 6 shows the operation of the restart timer. Normally C_{prot} is discharged to 0 V. When a restart is requested, C_{prot} is quickly charged to the upper switching level $V_{u(RCPROT)}$. Then the RCPROT pin becomes high ohmic and C_{prot} discharges through R_{prot}. The restart time has elapsed when V_{RCPROT} reaches the lower switching level $V_{l(RCPROT)}$ (typ. 0.5 V). The IC then restarts and C_{prot} is discharged.

7.5.3 Fast shut-down reset (pin SNSMAINS)

The latched Protection shut-down state will be reset when V_{SUPIC} and V_{SUPHV} drop below their respective reset levels, $V_{rst(SUPIC)}$ and $V_{rst(SUPHV)}$. Typically, the PFC boost capacitor, C_{boost}, will need to discharge before V_{SUPIC} and V_{SUPHV} drop below their reset levels, which can take a long time.

Fast shut-down reset facilitates a faster reset. When the mains supply is interrupted, the voltage on pin SNSMAINS will fall. As soon as $V_{SNSMAINS}$ falls below $V_{rst(SNSMAINS)}$ and subsequently rises again by a hysteresis value, the IC will leave the Protection shut-down state. The boost capacitor C_{boost} does not need to be discharged to initiate a new start-up.

The Protection shut-down state can also be ended by pulling down the enable input (pin SSHBC/EN).

7.5.4 Output overvoltage protection (pin SNSOUT)

The SSL4120T outputs are provided with overvoltage protection (OVP-output; see Section 7.9). The output voltage can be measured via the auxiliary winding of the resonant transformer. This voltage can be sensed at the SNSOUT pin via an external rectifier and resistive divider. An overvoltage is detected when the SNSOUT voltage exceeds $V_{ovp(SNSOUT)}$ (typ. 3.5 V). Once an overvoltage has been detected, the SSL4120T will go to the Protection shut-down state.

Additional external protection circuits, such as an external overtemperature protection circuit, can be connected to this pin. They should be connected to pin SNSOUT via a diode so that the error condition will trigger an OVP event.

7.5.5 Output undervoltage protection (pin SNSOUT)

In applications where the SSL4120T is supplied from the auxiliary winding of the HBC transformer, a SUPIC undervoltage protection event (UVP-SUPIC) will be triggered automatically when an error condition results in a drop in the output voltage.

In applications where the SSL4120T is supplied from a separate DC source (e.g. a standby supply), the SSL4120T will not automatically stop switching if an error condition causes the output voltage to fall. For this reason, the SSL4120T outputs are provided with undervoltage protection (UVP output; see Section 7.9). A UVP output event will restart the IC if V_{SNSOUT} drops below $V_{uvp(SNSOUT)}$ (typ. 2.3 V).

During start-up, the output voltage will be below $V_{uvp(SNSOUT)}$ for a time. This should not be considered an error condition provided it doesn't last longer than expected. For this reason, the protection timer is started as soon as V_{SNSOUT} drops below $V_{uvp(SNSOUT)}$. The Restart state is activated if the UVP output event is still active once the protection time has expired.

7.5.6 OverTemperature Protection (OTP)

Accurate internal overtemperature protection is provided in the SSL4120T. When the junction temperature exceeds the overtemperature protection activation temperature, T_{otp} (typ. 150 °C), the IC will go to the Thermal hold state. The SSL4120T will exit the Thermal hold state when the temperature falls again, to around 10 °C below T_{otp}.

7.6 Burst mode operation (pin SNSOUT)

The HBC and PFC controllers can be operated in Burst mode. In Burst mode the controllers will be on for a period, then off for a period. Burst mode operation increases efficiency under low-load conditions.

A low-load condition can be detected using a simple external circuit that makes use of the information from the feedback loop or from the average primary current. The detection circuit can pull down pin SNSOUT to pause operation of the SSL4120T for a burst-off time. Both controllers, or only the HBC controller, can be paused during the burst-off time:

- Burst-off level for HBC, $V_{burst(HBC)}$ (typ. 1 V).

  When V_{SNSOUT} drops below $V_{burst(HBC)}$, operation of the HBC controller will be suspended. Both the high-side and the low-side power switches will be off. The PFC continues to operate normally. When V_{SNSOUT} rises above $V_{burst(HBC)}$ again, the HBC controller will resume normal operation, without executing a soft start sequence.
- Burst-off level for PFC, $V_{burst(PFC)}$ (typ. 0.4 V).

  When V_{SNSOUT} drops below $V_{burst(PFC)}$, operation of the PFC controller will also be suspended (the HBC will have been paused already). When V_{SNSOUT} rises above $V_{burst(PFC)}$ again, the PFC controller will resume normal operation via a PFC soft start (see Section 7.7.6).

To ensure Burst mode is not activated before the output voltage becomes valid, a current from the SNSOUT pin (typ. 100 µA) will hold V_{SNSOUT} at $V_{pu(SNSOUT)}$, which is above both burst levels. The resistance between the SNSOUT pin and ground should therefore be greater than 20 kΩ.

7.7 PFC controller

The PFC controller converts the rectified universal mains voltage into an accurately regulated boost voltage of 400 V (DC). It operates in quasi-resonant or discontinuous conduction mode and is controlled via an on-time control system. The resulting mains harmonic current emissions of a typical application will easily meet the class-D MHR requirements.

The PFC controller uses valley switching to minimize losses. A primary stroke is only started once the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value.

7.7.1 PFC gate driver (pin GATEPFC)

The circuit driving the gate of the power MOSFET has a high current sourcing capability $I_{source(GATEPFC)}$ (typ. 500 mA) and a high current sink capability $I_{sink(GATEPFC)}$ (typ. 1.2 A). This permits fast turn-on and turn-off of the power MOSFET to ensure efficient operation. The driver is supplied from the regulated SUPREG supply.

7.7.2 PFC on-time control

The PFC operates under on-time control. The on-time of the PFC MOSFET is determined by:

- The error amplifier and the loop compensation via the voltage on pin COMPPFC

  At $V_{ton(COMPPFC)zero}$ (typ. 3.5 V), the on-time is reduced to zero. At $V_{ton(COMPPFC)max}$ the on-time is at a maximum
- Mains compensation via the voltage on pin SNSMAINS

7.7.2.1 PFC error amplifier (pins COMPPFC and SNSBOOST)

The boost voltage is divided via a high-ohmic resistive divider. It is fed to the SNSBOOST pin. The transconductance error amplifier, which compares the SNSBOOST voltage with an accurate trimmed reference voltage $V_{reg(SNSBOOST)}$, is connected to this pin. The output current is filtered by the external loop compensation network at the COMPPFC pin. In a typical application, the bandwidth of the regulation loop is set by a resistor and two capacitors.

The COMPPFC voltage is clamped at a maximum of $V_{clamp(COMPPFC)}$. This avoids a long recovery time in the event that the boost voltage rises above the regulation level for a period of time.

7.7.2.2 PFC mains compensation (pin SNSMAINS)

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application, this will result in a low bandwidth for low mains input voltages, while at high mains input voltages the MHR requirements may be hard to meet.

The SSL4120T contains a correction circuit to compensate for this effect. The average mains voltage is measured via the SNSMAINS pin and this information is fed to an internal compensation circuit. Figure 7 illustrates the relationship between the SNSMAINS voltage, the COMPPFC voltage, and the on-time. This compensation makes it is possible

to keep the regulation loop bandwidth constant over the full mains input range, yielding a fast transient response on load steps, while still complying with class-D MHR requirements.

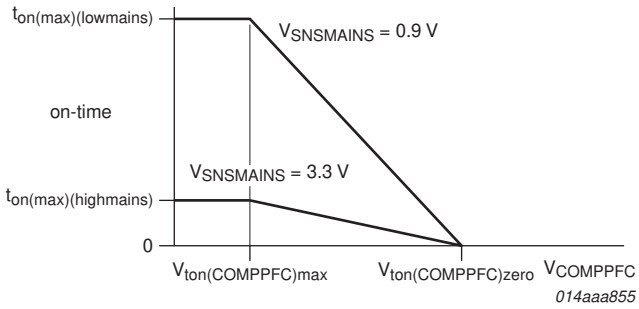


Fig 7. Relationship between on-time, SNSMAINS voltage and COMPPFC voltage

7.7.3 PFC demagnetization sensing (pin SNSAUXPFC)

The voltage on the SNSAUXPFC pin is used to detect transformer demagnetization. During the secondary stroke, the transformer is magnetized and current flows in the boost output. During this time, $V_{SNSAUXPFC} < V_{demag(SNSAUXPFC)}$ (typ. −100 mV) and the PFC MOSFET is kept off.

After some time, the transformer becomes demagnetized and current stops flowing in the boost output. From that moment, $V_{SNSAUXPFC} > V_{demag(SNSAUXPFC)}$ and valley detection is started. The MOSFET remains off.

To ensure switching continues under all circumstances, the MOSFET is forced to switch on if the magnetizing of the transformer ($V_{SNSAUXPFC} < V_{demag(SNSAUXPFC)}$) is not detected within $t_{to(mag)}$ (typ. 50 µs) after GATEPFC goes LOW.

It is recommended that a 5 kΩ series resistor be connected to this pin to protect the internal circuitry, against lightning for example. The resistor should be placed close to the IC on the printed circuit board to prevent incorrect switching due to external disturbances.

7.7.4 PFC valley sensing (pin SNSAUXPFC)

The PFC MOSFET is switched on for the next stroke to reduce switching losses and EMI if the voltage at the drain of the MOSFET is at its minimum (valley switching), see Figure 8.

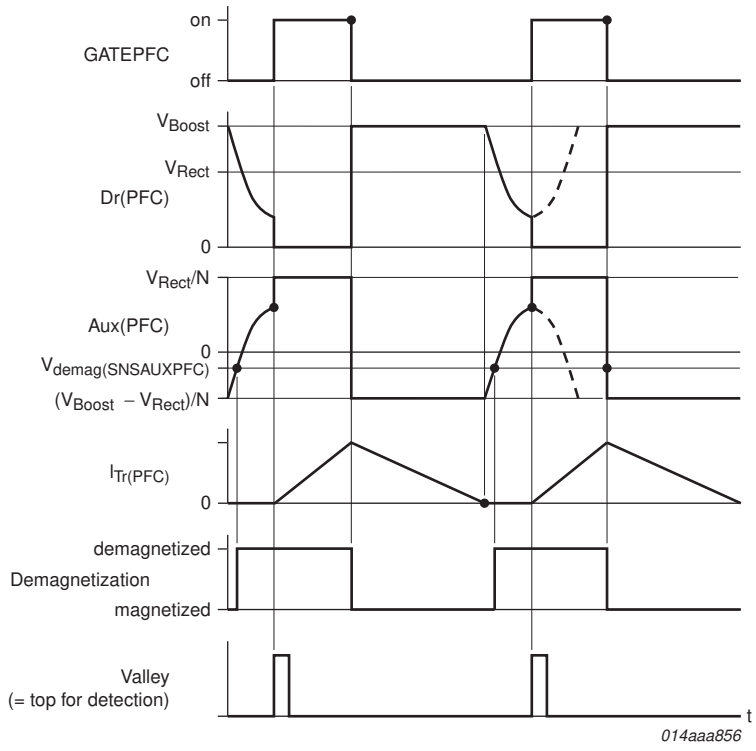


Fig 8. Demagnetization and valley detection

Valleys are detected by the valley sensing block connected to the SNSAUXPFC pin. This block measures the voltage at the auxiliary winding of the PFC transformer, which is a reduced and inverted copy of the MOSFET drain voltage. When a valley of the drain voltage (= top at SNSAUXPFC voltage) is detected, the MOSFET is switched on.

If no top is detected on the SNSAUXPFC pin (= valley at the drain) within $t_{to(vrec)}$ (typ. 4 µs) after demagnetization was detected, the MOSFET is forced to switch on.

7.7.5 PFC frequency and off-time limiting

For transformer optimization and to minimize switching losses, the switching frequency is limited to $f_{max(PFC)}$. If the frequency for quasi-resonant operation is above $f_{max(PFC)}$, the system will switch to Discontinuous conduction mode. The PFC MOSFET is switched on when the drain-source voltage is at a minimum (valley switching).

The minimum off-time is limited to $t_{off(PFC)min}$ to ensure proper control of the PFC MOSFET under all circumstances.

7.7.6 PFC soft start and soft stop (pin SNSCURPFC)

The PFC controller features a soft start function which slowly increases the primary peak current at start-up and a soft stop function which slowly decreases the transformer peak current, before operations are halted. This is to prevent transformer rattle at start-up or during Burst mode operation.

This is achieved by connecting a resistor $R_{ss(PFC)}$ and a capacitor $C_{ss(PFC)}$ between pin SNSCURPFC and the current sense resistor $R_{cur(PFC)}$. At start-up, an internal current source $I_{ch(ss)(PFC)}$ charges the capacitor to $V_{SNSCURPFC} = I_{ch(ss)(PFC)} \times R_{ss(PFC)}$. The voltage is limited to the maximum PFC soft start clamp voltage, $V_{clamp(ss)PFC}$. The additional voltage across the charged capacitor results in a reduced peak current. After start-up, the internal current source is switched-off, capacitor $C_{ss(PFC)}$ discharges across $R_{ss(PFC)}$ and the peak current increases.

The start level and the time constant of the rising primary current can be adjusted externally by changing the values of $R_{ss(PFC)}$ and $C_{ss(PFC)}$.

$$I_{Cur(PFC)(pk)} = \frac{V_{ocr(PFC)} - (I_{ch(ss)(PFC)} \times R_{ss(PFC)})}{R_{cur(PFC)}}$$

$$\tau = R_{ss(PFC)} \times C_{ss(PFC)}$$

Soft stop is achieved by switching on the internal current source $I_{ch(ss)(PFC)}$.This current charges $C_{ss(PFC)}$ and the increasing capacitor voltage reduces the peak current. The charge current will flow as long as the voltage on pin SNSCURPFC is below the maximum PFC soft start voltage (typ. 0.5 V). If $V_{SNSCURPFC}$ exceeds the maximum PFC soft start voltage, the soft start current source will start limiting the charge current. To accurately determine if the capacitor is charged, the voltage is only measured during the off-time of the PFC power switch. The operation of the PFC is stopped when $V_{SNSCURPFC} > V_{stop(ss)(PFC)}$.

7.7.7 PFC overcurrent regulation, OCR-PFC (pin SNSCURPFC)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor ($R_{cur(PFC)}$) connected to the source of the external MOSFET. The voltage is measured via the SNSCURPFC pin and is limited to $V_{ocr(PFC)}$.

A voltage peak will appear on $V_{SNSCURPFC}$ when the PFC MOSFET is switched on due to the discharging of the drain capacitance. The leading edge blanking time, $t_{leb(PFC)}$, ensures that the overcurrent sensing block will not react to this transitory peak.

7.7.8 PFC mains undervoltage protection/brownout protection, UVP-mains (pin SNSMAINS)

The voltage on the SNSMAINS pin is sensed continuously to prevent the PFC trying to operate at very low mains input voltages. PFC switching stops as soon as $V_{SNSMAINS}$ drops below $V_{uvp(SNSMAINS)}$. Mains undervoltage protection is also called brownout protection.

$V_{SNSMAINS}$ is clamped to a minimum value of $V_{pu(SNSMAINS)}$ for fast restart as soon as the mains input voltage recovers after a mains-dropout. The PFC (re)starts once $V_{SNSMAINS}$ exceeds the start level $V_{start(SNSMAINS)}$.

7.7.9 PFC boost overvoltage protection, OVP-boost (pin SNSBOOST)

An overvoltage protection circuit has been built in to prevent boost overvoltages during load steps and mains transients.

Switching of the power factor correction circuit is inhibited as soon as the voltage on the SNSBOOST pin rises above $V_{ovp(SNSBOOST)}$. PFC switching resumes as soon as $V_{SNSBOOST}$ drops below $V_{ovp(SNSBOOST)}$ again.

Overvoltage protection will also be triggered in the event of an open circuit at the resistor connected between SNSBOOST and ground.

7.7.10 PFC short circuit/open-loop protection, SCP/OLP-PFC (pin SNSBOOST)

The power factor correction circuit will not start switching until the voltage on the SNSBOOST pin rises above $V_{scp(SNSBOOST)}$. This acts as short circuit protection for the boost voltage (SCP-boost).

The SNSBOOST pin draws a small input current $I_{prot(SNSBOOST)}$. If this pin gets disconnected, the residual current will pull down $V_{SNSBOOST}$, triggering short circuit protection (SCP-boost). This combination creates an open-loop protection (OLP-PFC).

7.8 HBC controller

The HBC controller converts the 400 V boost voltage from the PFC into one or more regulated DC output voltages and drives two external MOSFETS in a half-bridge configuration connected to a transformer. The transformer, which has a leakage inductance and a magnetizing inductance, forms the resonant circuit in combination with the resonant capacitor and the load at the output. The regulation is realized via frequency control.

7.8.1 HBC high-side and low-side driver (pin GATEHS and GATELS)

Both drivers have identical driving capability. The output of each driver is connected to the equivalent gate of an external high-voltage power MOSFET.

The low-side driver is referenced to pin PGND and is supplied from SUPREG.

The high-side driver is floating. The reference for the high-side driver is pin HB, connected to the midpoint of the external half-bridge. The high-side driver is supplied from SUPHS which is connected to the external bootstrap capacitor C_{SUPHS}. The bootstrap capacitor is charged from SUPREG via external diode D_{SUPHS} when the low-side MOSFET is on.

7.8.2 HBC boost undervoltage protection, UVP-boost (pin SNSBOOST)

The voltage on the SNSBOOST pin is sensed continuously to prevent the HBC controller trying to operate at very low boost input voltages. Once $V_{SNSBOOST}$ drops below $V_{uvp(SNSBOOST)}$, HBC switching stops the next time GATELS goes HIGH. HBC switching resumes as soon as $V_{SNSBOOST}$ rises above $V_{start(SNSBOOST)}$.

7.8.3 HBC switch control

HBC switch control determines when the MOSFETs switch on and off. It uses the output from several other blocks.

- A divider is used to realize alternate switching of the high- and low-side MOSFETs for each oscillator cycle. The oscillator frequency is twice the half-bridge frequency.
- The controlled oscillator determines the switch-off point.
- Adaptive non-overlap time sensing determines the switch-on point. This is the adaptive non-overlap time function.

- Several protection circuits and the state of the SSHBC/EN input determine whether the resonant converter is allowed to start switching.

Figure 9 provides an overview of typical switching behavior.

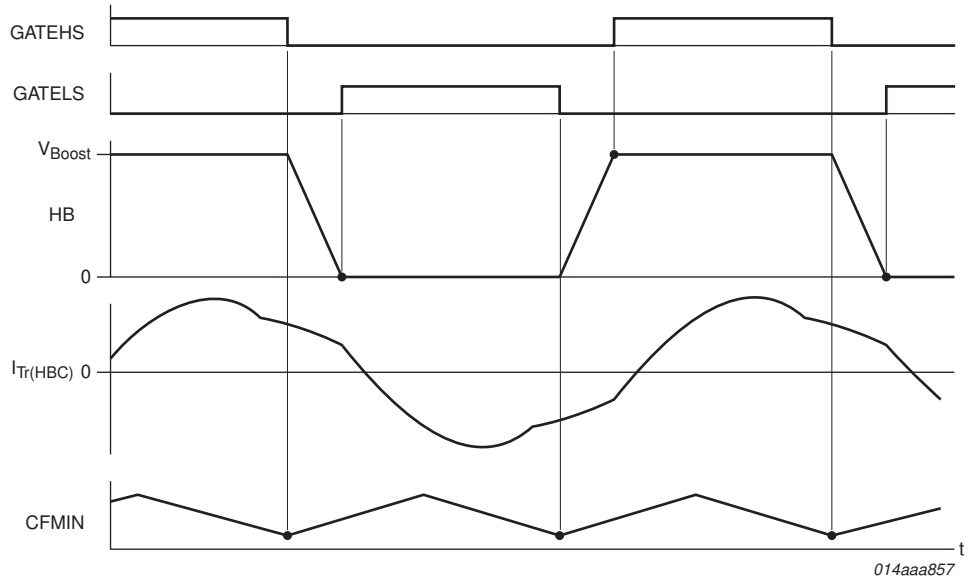


Fig 9. Switching behavior of the HBC

7.8.4 HBC Adaptive Non-Overlap (ANO) time function (pin HB)

7.8.4.1 Inductive mode (normal operation)

The high efficiency characteristic of a resonant converter is the result of Zero-Voltage Switching (ZVS) of the power MOSFETs, also called soft switching. To facilitate soft switching, a small non-overlap time is required between the on-times of the high- and low-side MOSFETs. During this non-overlap time, the primary resonant current (dis-)charges the capacitance of the half-bridge between ground and the boost voltage. After this (dis-)charge, the body diode of the MOSFET starts conducting and because the voltage across the MOSFET is zero, there are no switching losses when the MOSFET is switched on. This mode of operation is called inductive mode because the switching frequency is above the resonance frequency and the resonant tank has an inductive impedance.

The time required for the HB transition depends on the amplitude of the resonant current at the instant of switching. There is a complex relationship between this amplitude, the frequency, the boost voltage and the output voltage. Ideally the IC should switch the MOSFET on as soon as the HB transition has been completed. If it waits any longer, the HP voltage may swing back, especially at high output loads. The advanced adaptive non-overlap time function takes care of this timing, so that it's not necessary to chose a fixed dead time (which is always a compromise). This saves on external components.

Adaptive non-overlap time sensing measures the HB slope after one MOSFET has been switched off. Normally, the HB slope starts immediately (the voltage starts rising or falling). Once the transition at the HB node is complete, the slope ends (the voltage stops rising/falling). This is detected by the ANO time sensor and the other MOSFET is switched

on. In this way the non-overlap time is optimized automatically, minimizing switching losses, even if the HB transition cannot be fully completed. Figure 10 illustrates the operation of the adaptive non-overlap time function in Inductive mode.

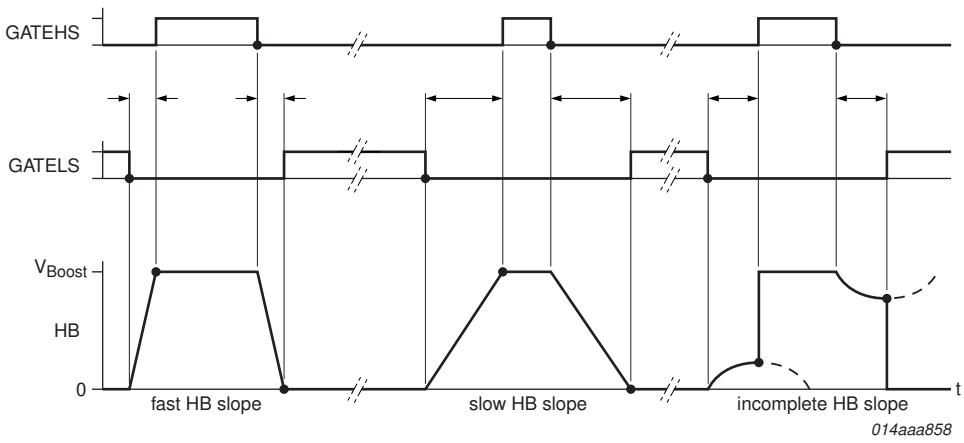


Fig 10. Adaptive non-overlap time function (normal inductive operation)

The non-overlap time depends on the HB slope, but has upper and lower limits.

An integrated minimum non-overlap time, $t_{no(min)}$, prevents cross conduction occurring under any circumstances.

The maximum non-overlap time is limited to the oscillator charge time. If the HB slope lasts longer than the oscillator charge time (= ¼ of HB switching period) the MOSFET is forced to switch on. In this case the MOSFET is not soft switching. This limitation ensures that, at very high switching frequencies, the MOSFET on-time is at least ¼ of the HB switching period.

7.8.4.2 Capacitive mode

The description above holds for normal operation with a switching frequency above the resonance frequency. When an error condition occurs (e.g. output short, load pulse too high) the switching frequency can be lower than the resonance frequency. The resonant tank then has a capacitive impedance. In Capacitive mode, the HB slope does not start after the MOSFET has switched off. Switching on the other MOSFET is not recommended in this situation. The absence of soft switching increases dissipation in the MOSFETs. In Capacitive mode, the body diode in the switched-off MOSFET may start conducting. Switching on the other MOSFET at this instant can result in the immediate destruction of the MOSFETs.

The advanced adaptive non-overlap time of the SSL4120T will always wait until the slope at the half-bridge node starts. It guarantees safe switching of the MOSFETs in all circumstances. Figure 11 illustrates the operation of the adaptive non-overlap time function in Capacitive mode.

In Capacitive mode, half the resonance period may elapse before the resonant current changes back to the correct polarity and starts charging the half-bridge node. The oscillator is slowed down until the half-bridge slope starts to allow this relatively long waiting time. See Section 7.8.5 for more details on the oscillator.

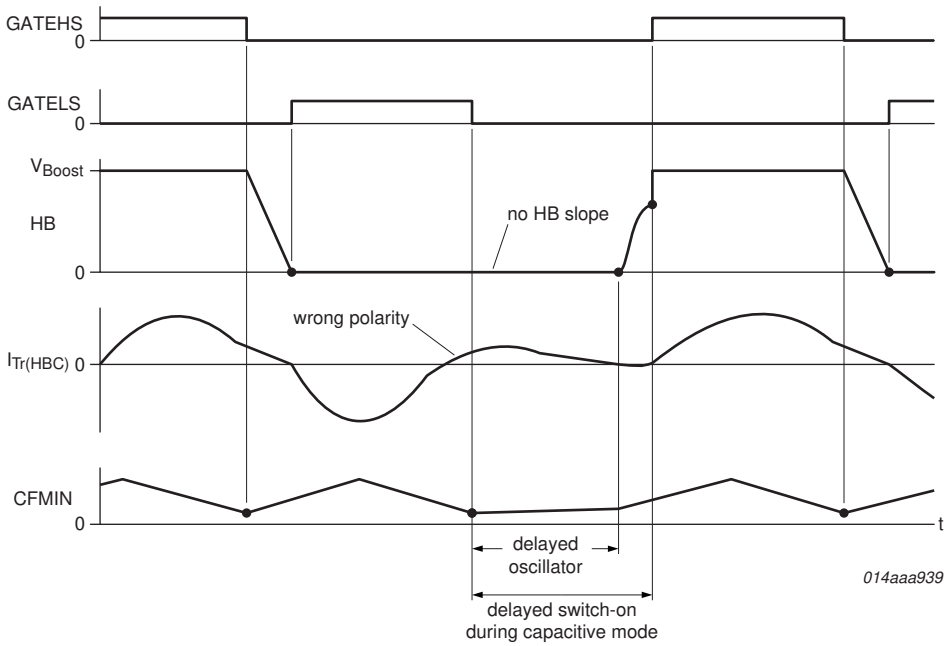


Fig 11. Adaptive non-overlap time function (capacitive operation)

The MOSFET will be forced to switch on if the half-bridge slope fails to start and the oscillator voltage reaches $V_{u(CFMIN)}$.

The switching frequency is increased to eliminate the problems associated with Capacitive mode operation. This is explained in Section 7.8.11.

7.8.5 HBC slope controlled oscillator (pins CFMIN and RFMAX)

The slope-controlled oscillator determines the switching frequency of the half-bridge. The oscillator generates a triangular waveform between $V_{u(CFMIN)}$ and $V_{l(CFMIN)}$ at the external capacitor C_{fmin}.

Figure 12 shows how the frequency is determined.

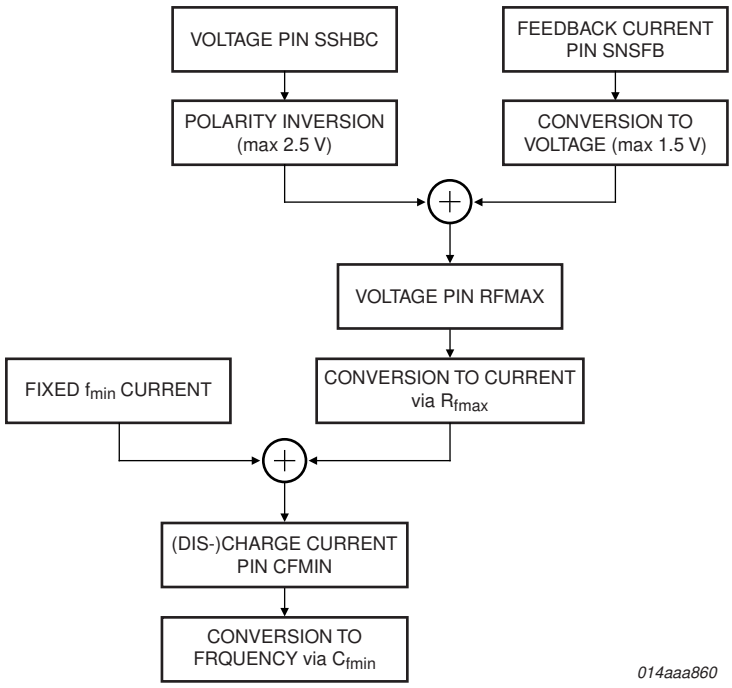


Fig 12. Determination of frequency

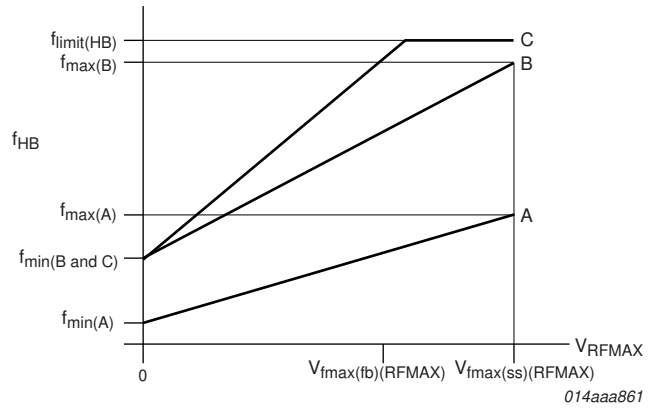
Two external components determine the frequency range:

- Capacitor C_{fmin} connected between pin CFMIN and ground sets the minimum frequency in combination with an internally trimmed current source $I_{osc(min)}$.
- Resistor R_{fmax} connected between pin RFMAX and ground sets the frequency range and thus the maximum frequency.

The oscillator frequency depends on the charge and discharge currents of C_{fmin}. The (dis-)charge current contains a fixed component, $I_{osc(min)}$, that determines the minimum frequency, and a variable component that is 4.9 times greater than the current in pin RFMAX. I_{RFMAX} is determined by the value of R_{fmax} and the voltage on pin RFMAX:

- The voltage on pin RFMAX is $V_{fmin(RFMAX)}$ (typ. 0 V) at the minimum frequency.
- The voltage on pin RFMAX is $V_{fmax(fb)(RFMAX)}$ (typ. 1.5 V) at the maximum feedback frequency.
- The voltage on pin RFMAX is $V_{fmax(ss)(RFMAX)}$ (typ. 2.5 V) at the maximum soft start frequency.

The maximum frequency of the oscillator is limited internally. The HB frequency is limited to $f_{limit(HB)}$ (min. 500 kHz). Figure 13 illustrates the relationship between V_{RFMAX}, R_{fmax}, C_{fmin} and f_{HB}.



A: C_{fmin} = high, R_{fmax} = high

B: C_{fmin} = low, R_{fmax} = low

C: C_{fmin} = low, R_{fmax} = too low

Fig 13. Function of R_{fmax} and C_{fmin}

The oscillator is controlled by the slope of the half-bridge. The oscillator charge current is initially set to a low value $I_{osc(red)}$ (typ. 30 µA). When the start of the half-bridge slope is detected, the charge current is increased to its normal value. This feature is used in combination with the adaptive non-overlap time function as described in Section 7.8.4.2 and Figure 11. Since the half-bridge slope normally starts directly after the MOSFET is switched off, the length of time the oscillator current is low will be negligible under normal operating conditions.

7.8.6 HBC feedback input (pin SNSFB)

In a typical power supply application, the output voltage is compared and amplified on the secondary side. The output of the error amplifier is transferred to the primary side via an opto-coupler. This opto-coupler can be connected directly to the SNSFB pin.

The SNSFB pin supplies the opto-coupler from an internal voltage source $V_{pu(SNSFB)}$ (typ. 8.4 V) with a series resistance $R_{O(SNSFB)}$. The series resistance allows spike filtering via an external capacitor. To ensure sufficient bias current for the opto-coupler, the feedback input has a threshold current $I_{fmin(SNSFB)}$ (typ. 0.66 mA) at which the frequency is at a minimum. The maximum frequency is reached at $I_{fmax(SNSFB)}$ (typ 2.2 mA). The maximum frequency that can be reached via the SNSFB pin is lower (typ. 60 %) than the maximum frequency that can be reached via the SSHBC/EN pin. Figure 14 shows the relationship between I_{SNSFB}, V_{SNSFB} and V_{RFMAX}.

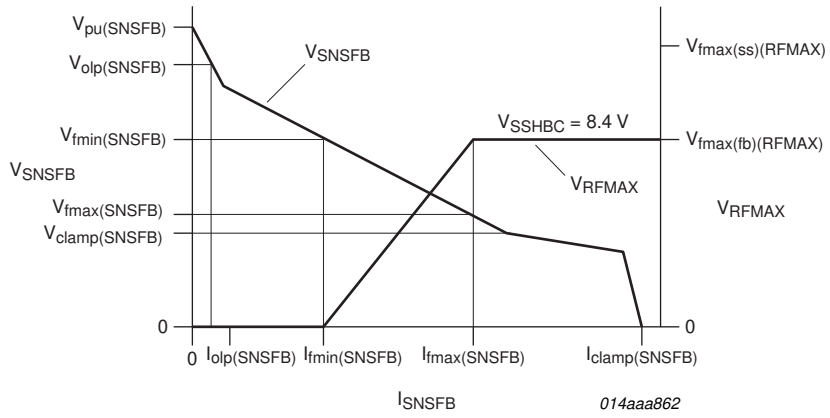


Fig 14. Transfer function of feedback input

Below the level for minimum frequency, V_{SNSFB} is clamped at $V_{clamp(SNSFB)}$ (typ. 3.2 V). This clamp enables a fast recovery of the output voltage regulation loop after an overshoot of the output voltage. The maximum current the clamp can deliver is $I_{clamp(SNSFB)}$ (typ. 7.3 mA).

7.8.7 HBC open-loop protection, OLP-HBC (pin SNSFB)

Under normal operating conditions, the opto-coupler current will be between $I_{fmin(SNSFB)}$ and $I_{fmax(SNSFB)}$ and will pull down the voltage at pin SNSFB. Due to an error in the feedback loop, the current could be less than $I_{fmin(SNSFB)}$ with the HBC controller delivering maximum output power.

The HBC controller features open-loop protection (OLP-HBC), which monitors the voltage on pin SNSFB. When V_{SNSFB} exceeds $V_{olp(SNSFB)}$, the protection timer is started. The Restart state is activated if the OLP condition is still present after the protection time has elapsed.

7.8.8 HBC soft start (pin SSHBC/EN)

The relationship between switching frequency and output current is not constant. It depends strongly on the output voltage and the boost voltage. This relationship can be complex. The SSL4120T contains a soft start function to ensure that the resonant converter starts or restarts with safe currents. This soft start function forces a start at such a high frequency that currents will be acceptable under all conditions. Soft start then slowly decreases the frequency. Normally, output voltage regulation will have taken over frequency control before soft start has reached its minimum frequency. Limiting the output current during start-up also limits the rate at which the output voltage rises and prevents an overshoot.

Soft start utilizes the voltage on pin SSHBC/EN. The timing of the soft start is set by external capacitor $C_{ss(HBC)}$. Pin SSHBC/EN is also used as an enable input. Soft start voltage levels are above the enable voltage thresholds.

7.8.8.1 Soft start voltage levels

The relationship between the soft start voltage at pin SSHBC/EN and the voltage at pin RFMAX, which is directly related to the frequency, is illustrated in Figure 15.