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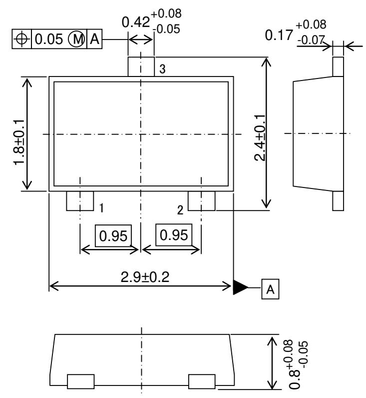
TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

SSM3J332R

○Power Management Switch Applications

Unit: mm

- 1.8-V drive
- Low ON-resistance: $R_{DS(ON)}$ = 144 mΩ (max) (@V_{GS} = -1.8 V)
  $R_{DS(ON)}$ = 72.0 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(ON)}$ = 50.0 mΩ (max) (@V_{GS} = -4.5 V)
  $R_{DS(ON)}$ = 42.0 mΩ (max) (@V_{GS} = -10 V)



1: Gate
2: Source
3: Drain

SOT-23F

JEDEC	―
JEITA	―
TOSHIBA	2-3Z1A

Weight: 11 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-30	V
Gate-Source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D (Note 1)	-6.0	A
	Pulse	I_{DP} (Note 1,2)	-24.0	
Power dissipation		P_D (Note 3)	1	W
		t < 10s	2	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	-55 to 150	°C

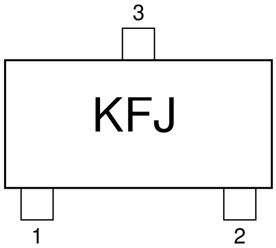
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

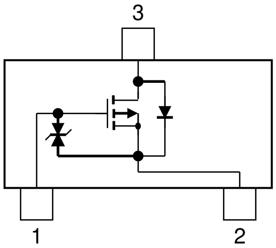
Note 2: PW ≤ 1ms, Duty ≤ 1%

Note 3: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Marking



Equivalent Circuit (Top View)



Start of commercial production
2010-08

Electrical Characteristics (Ta = 25°C)

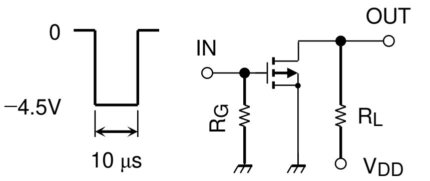
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)DSS}$	I_D = -10 mA, V_{GS} = 0 V	-30	—	—	V
		$V_{(BR)DSX}$	I_D = -10 mA, V_{GS} = 8 V (Note 5)	-22	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	—	—	-1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.5	—	-1.2	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -2.5 A (Note 4)	5.7	11.3	—	S
Drain–source ON-resistance		$R_{DS (ON)}$	I_D = -5.0 A, V_{GS} = -10 V (Note 4)	—	36.0	42.0	mΩ
			I_D = -4.0 A, V_{GS} = -4.5 V (Note 4)	—	42.5	50.0	
			I_D = -2.5 A, V_{GS} = -2.5 V (Note 4)	—	57.5	72.0	
			I_D = -0.5 A, V_{GS} = -1.8 V (Note 4)	—	76.5	144	
Input capacitance		C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V f = 1 MHz	—	560	—	pF
Output capacitance		C_{oss}		—	80	—	
Reverse transfer capacitance		C_{rss}		—	65	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -15 V, I_D = -2.0 A V_{GS} = 0 to -4.5 V, R_G = 10 Ω	—	15	—	ns
	Turn-off time	t_{off}		—	75	—	
Total Gate Charge		Q_g	V_{DD} = -15 V, I_D = -6.0 A, V_{GS} = -4.5 V	—	8.2	—	nC
Gate-Source Charge		Q_{gs1}		—	1.1	—	
Gate-Drain Charge		Q_{gd}		—	2.2	—	
Drain-Source forward voltage		V_{DSF}	I_D = 6.0 A, V_{GS} = 0 V (Note 4)	—	0.90	1.2	V

Note4: Pulse test

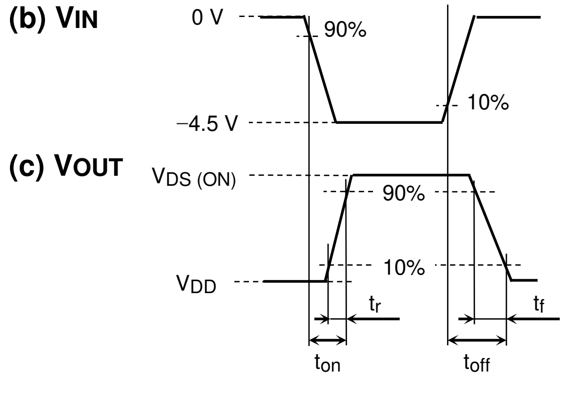
Note5: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

(a) Test Circuit



V_{DD} = -15 V
R_G = 10 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C



Notice on Usage

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1 mA for the SSM3J332R). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

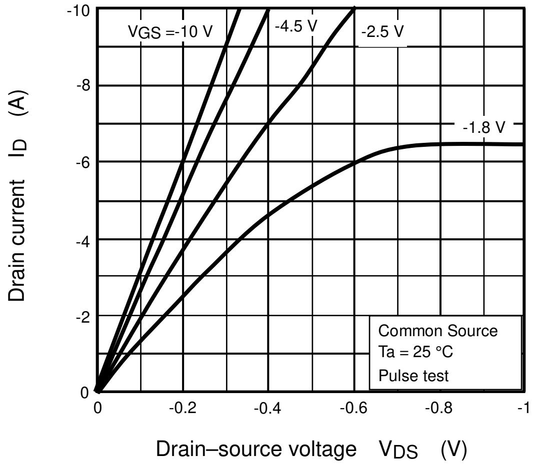
Take this into consideration when using the device.

Handling Precaution

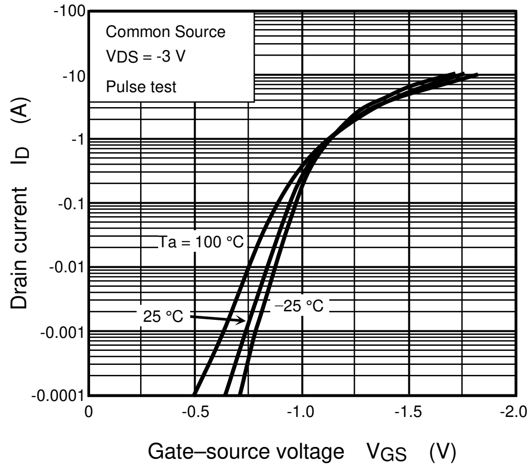
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th (ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

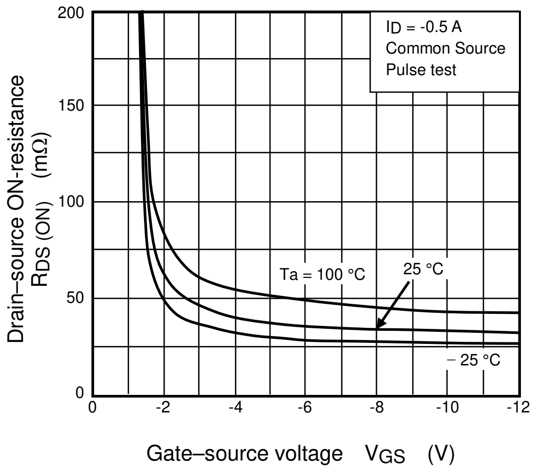
I_D – V_{DS}



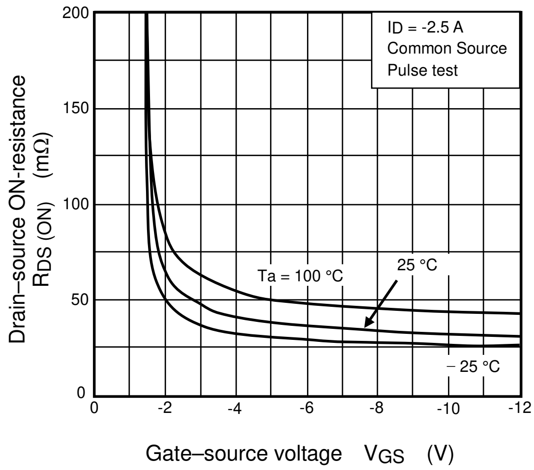
I_D – V_{GS}



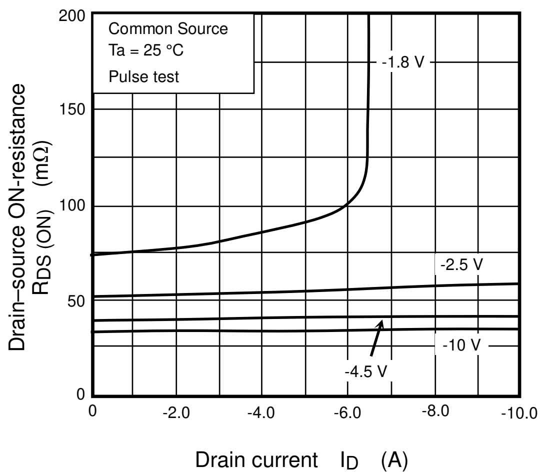
$R_{DS(ON)}$ – V_{GS}



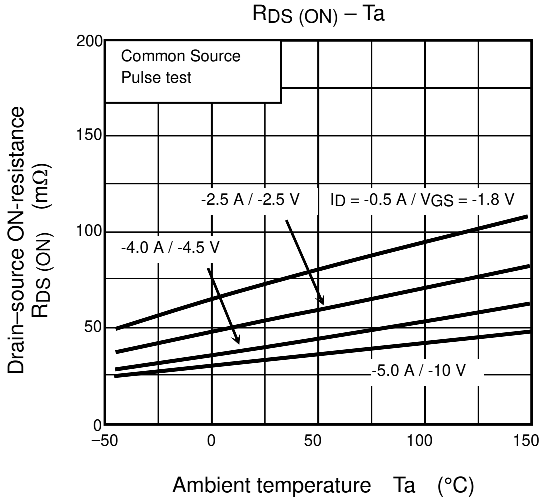
$R_{DS(ON)}$ – V_{GS}

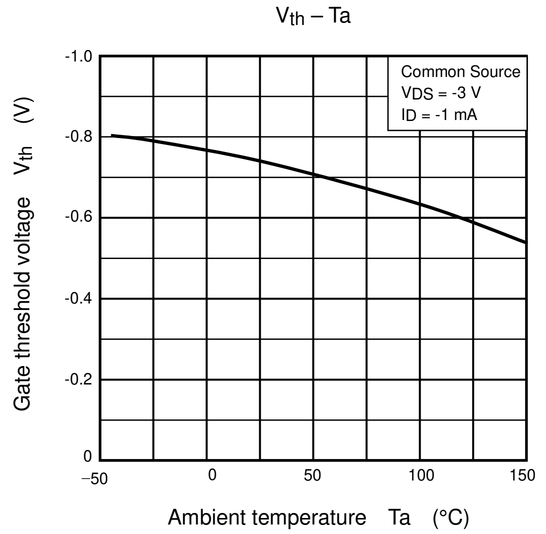


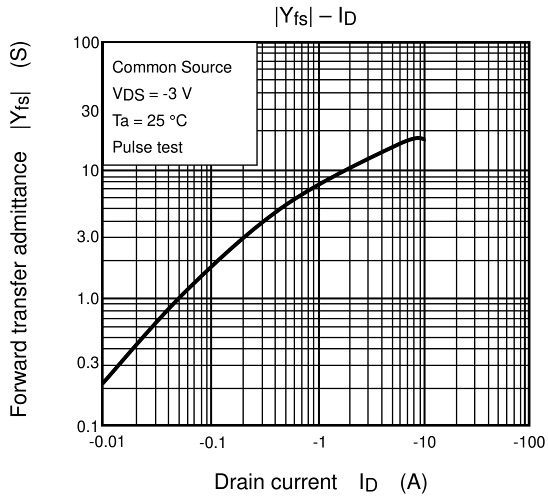
$R_{DS(ON)}$ – I_D

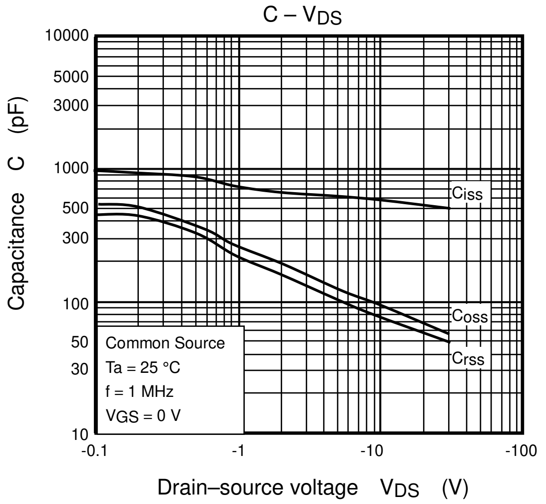


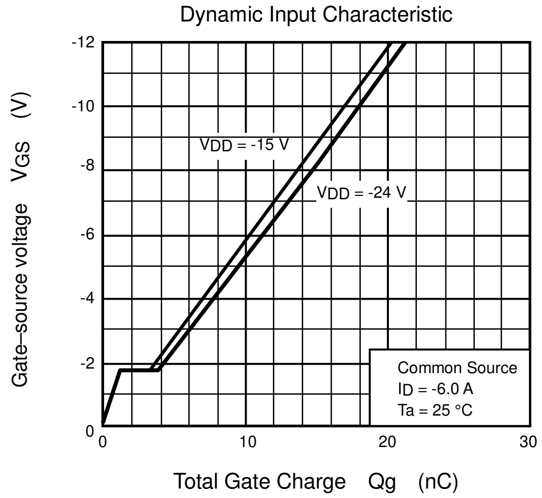
$R_{DS(ON)}$ – Ta

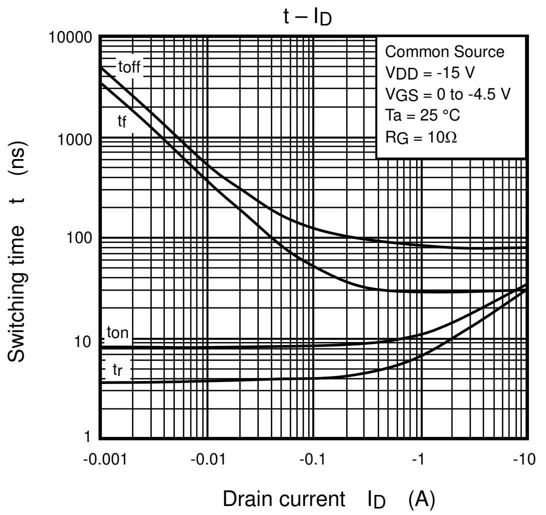


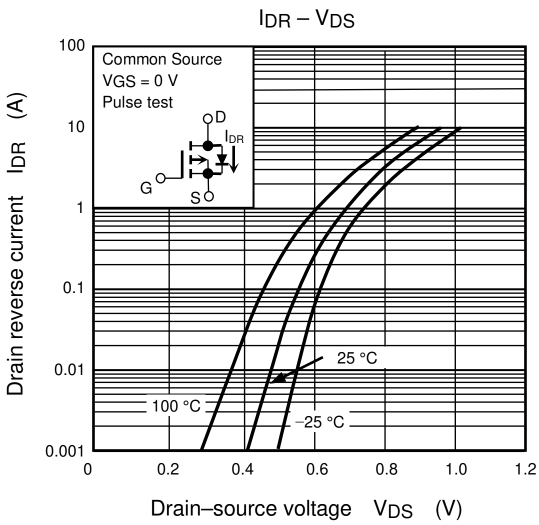

Vth – Ta
Common Source
VDS = -3 V
ID = -1 mA
Gate threshold voltage Vth (V)
-1.0
-0.8
-0.6
-0.4
-0.2
0
–50
0
50
100
150
Ambient temperature Ta (°C)

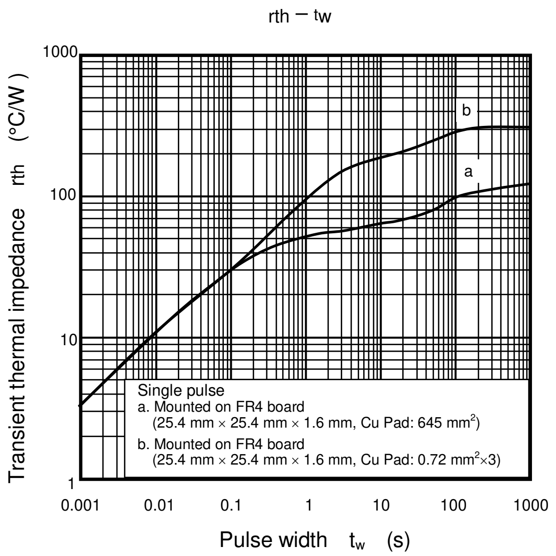

|Yfs| – ID
Common Source
VDS = -3 V
Ta = 25 °C
Pulse test
Forward transfer admittance |Yfs| (S)
100
30
10
3.0
1.0
0.3
0.1
-0.01
-0.1
-1
-10
-100
Drain current ID (A)

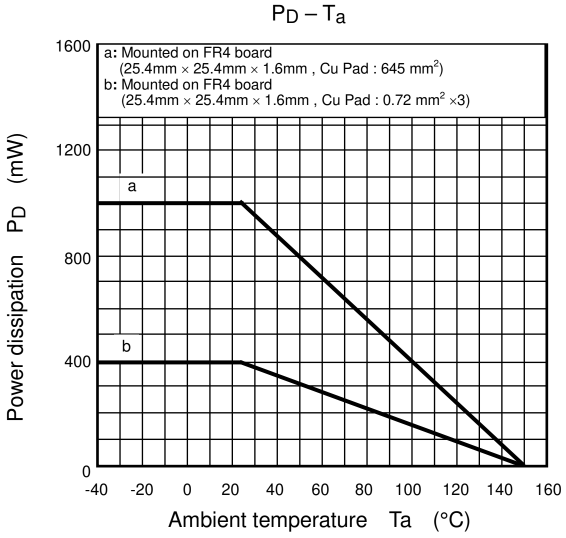

C – VDS
Ciss
Coss
Crss
Common Source
Ta = 25 °C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
10000
5000
3000
1000
500
300
100
50
30
10
-0.1
-1
-10
-100
Drain–source voltage VDS (V)

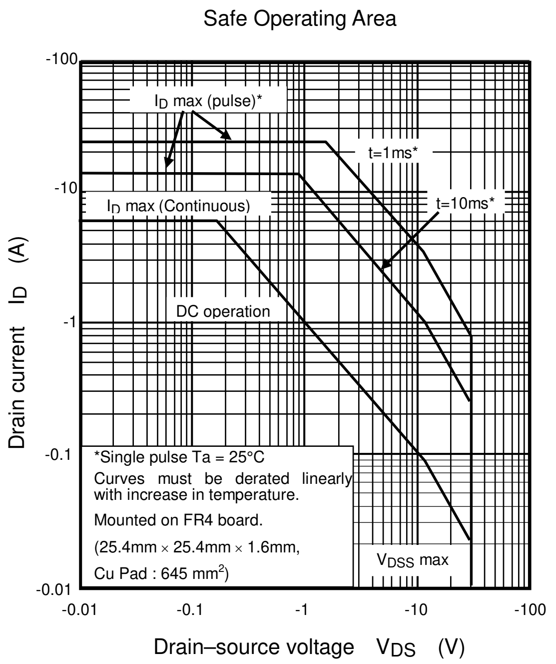

Dynamic Input Characteristic
VDD = -15 V
VDD = -24 V
Common Source
ID = -6.0 A
Ta = 25 °C
Gate–source voltage VGS (V)
-12
-10
-8
-6
-4
-2
0
0
10
20
30
Total Gate Charge Qg (nC)


t – ID
toff
tf
ton
tr
Common Source
VDD = -15 V
VGS = 0 to -4.5 V
Ta = 25 °C
RG = 10Ω
Switching time t (ns)
10000
1000
100
10
1
-0.001
-0.01
-0.1
-1
-10
Drain current ID (A)


IDR – VDS
Common Source
VGS = 0 V
Pulse test
D
IDR
G
S
25 °C
100 °C
–25 °C
Drain reverse current IDR (A)
100
10
1
0.1
0.01
0.001
0
0.2
0.4
0.6
0.8
1.0
1.2
Drain–source voltage VDS (V)


rth – tw
Transient thermal impedance rth (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)
a
b
Single pulse
a. Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm2)
b. Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.72 mm2×3)


PD – Ta
Power dissipation PD (mW)
1600
1200
800
400
0
-40
-20
0
20
40
60
80
100
120
140
160
Ambient temperature Ta (°C)
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 645 mm2)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 0.72 mm2 ×3)
a
b


Safe Operating Area
Drain current ID (A)
-100
-10
-1
-0.1
-0.01
-0.01
-0.1
-1
-10
-100
Drain–source voltage VDS (V)
ID max (pulse)*
t=1ms*
t=10ms*
ID max (Continuous)
DC operation
*Single pulse Ta = 25°C
Curves must be derated linearly with increase in temperature.
Mounted on FR4 board.
(25.4mm × 25.4mm × 1.6mm,
Cu Pad : 645 mm2)
VDSS max

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