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## 2.4 GHz WLAN Power Amplifier, 802.11b/g/n/256 QAM

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### Features

- High Gain:
  - Typically 38 dB gain across 2.4–2.5 GHz over temperature -40°C to +85°C
- Linear operation at both 3.3V and 5V
- High linear output power at 5V:
  - >30 dBm P1dB
  - Meets 802.11b ACPR requirements up to 28 dBm with 30% power-added efficiency
  - Meets 802.11g OFDM spectrum mask requirement up to 28 dBm
  - Typically 25 dBm with <3% EVM, 802.11g, 54 Mbps, 350 mA current
  - Typically 24 dBm with <2.5% EVM, 802.11n, MCS7-HT20, 50% duty cycle
  - Typically 23 dBm with <1.75% EVM, MCS9-VHT40, 50% duty cycle, 320 mA current
- High linear output power at 3.3V:
  - Meets 802.11b ACPR requirements up to 25 dBm with 27% power-added efficiency
  - Typically 21 dBm with <3% EVM, 802.11g, 54 Mbps, 240 mA current
  - Typically 20.5 dBm with <2.5% EVM, 802.11n, MCS7-HT20, 230 mA current
  - Typically 19 dBm with <1.75% EVM, MCS9-VHT40, 210 mA current
- High-speed power-up/down
  - Turn on/off time (10%-90%) <100 ns
- 10:1 VSWR survivability (unconditionally stable up to 28 dBm)
- On-chip power detection
  - >25 dB dynamic range, from 5 dBm to 30 dBm
  - VSWR- and temperature-insensitive
- Matched RF input/simple output matching
- Packages available
  - 16-contact UQFN (3mm x 3mm)
- All non-Pb (lead-free) devices are RoHS compliant

### Applications

- WLAN (IEEE 802.11b/g/n)
- WLAN 256 QAM
- AP router
- Cordless phones
- 2.4 GHz ISM wireless equipment

### 1.0 PRODUCT DESCRIPTION

SST12CP33 is a high-power, high-gain, WLAN 802.11b/g/n/256 QAM power amplifier (PA) based on the highly-reliable InGaP/GaAs HBT technology.

This PA can be easily configured for high-power applications with high power-added efficiency while operating over the 2.4-2.5 GHz frequency band. It can operate at both 3.3V and 5V  $V_{CC}$ , and typically provides 38 dB gain with 25% power-added efficiency @  $P_{OUT} = 28$  dBm for 802.11g at 5V.

SST12CP33 has excellent linearity, typically 25 dBm at 3% EVM with 54 Mbps 802.11g operation at 5V while meeting 802.11g spectrum mask at 28 dBm and 21 dBm at 3% EVM at 3.3V bias. SST12CP33 also has a single-ended power detector which lowers the users' cost for power control.

The power amplifier IC also features easy board-level usage along with high-speed power-up/-down control.

SST12CP33 is offered in 16-contact UQFN package. See [Figure 3-1](#) for pin assignments and [Table 3-1](#) for pin descriptions.

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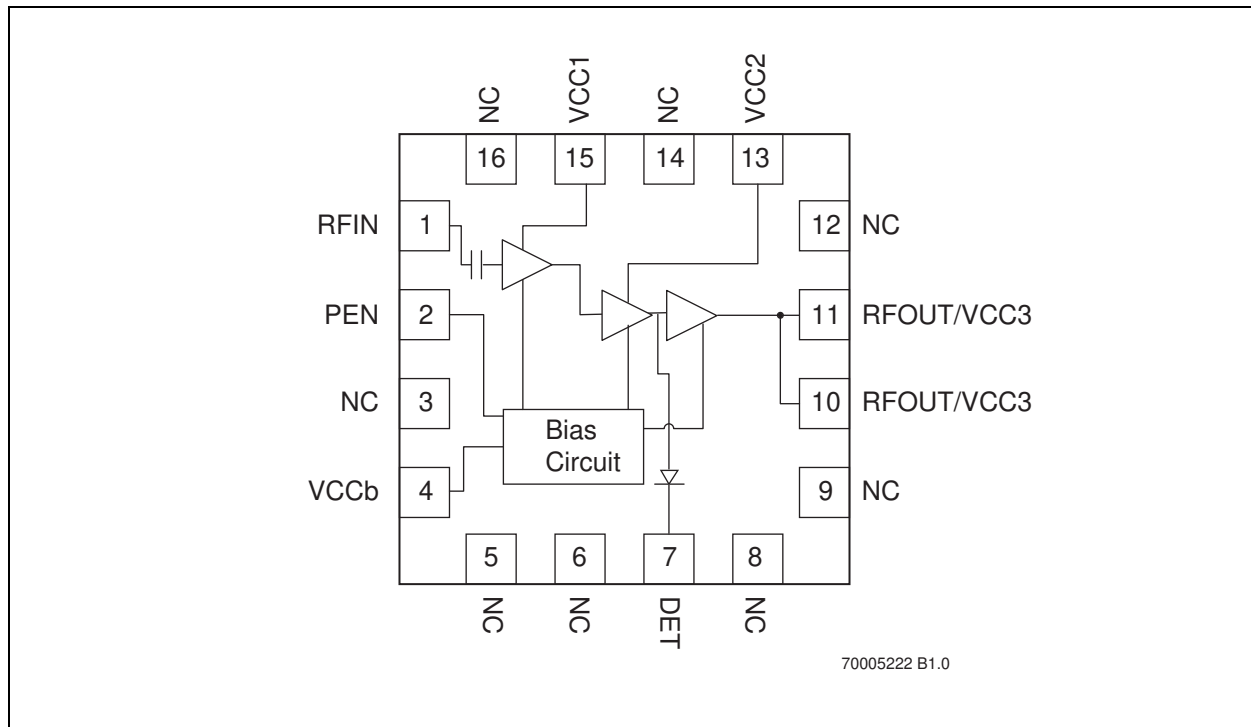
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## 2.0 FUNCTIONAL BLOCKS

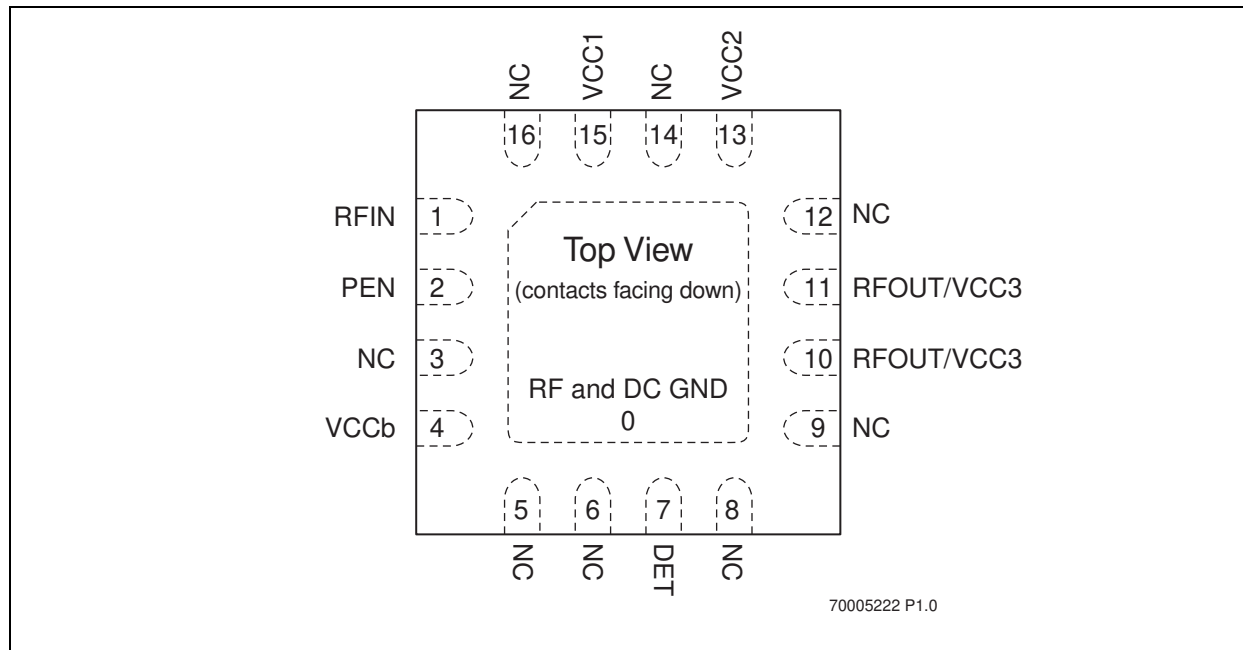
FIGURE 2-1: FUNCTIONAL BLOCK DIAGRAM





## 3.0 PIN ASSIGNMENTS

FIGURE 3-1: PIN ASSIGNMENTS FOR 16-CONTACT UQFN



## 3.1 Pin Descriptions

TABLE 3-1: PIN DESCRIPTION

Symbol	Pin No.	Pin Name	Type <sup>1</sup>	Function
GND	0	Ground		The center pad should be connected to RF ground
RFIN	1	RF <sub>IN</sub>	I	RF input, DC decoupled
PEN	2	PEN	PWR	PA enable and idle-current control
NC	3	No Connection		No Internal Connection
VCCb	4	Power Supply	PWR	Supply voltage for bias circuit
NC	5	No Connection		No Internal Connection
NC	6	No Connection		No Internal Connection
DET	7	V <sub>DET</sub>	O	On-chip power detector
NC	8	No Connection		No Internal Connection
NC	9	No Connection		No Internal Connection
RFOUT/VCC3	10	RF <sub>OUT</sub> & V <sub>CC3</sub>	O & PWR	RF output and PWR power supply 3 <sup>rd</sup> stage
RFOUT/VCC3	11	RF <sub>OUT</sub> & V <sub>CC3</sub>	O & PWR	RF output and PWR power supply 3 <sup>rd</sup> stage
NC	12	No Connection		No Internal Connection
VCC2	13	V <sub>CC2</sub>	PWR	PWR power supply, 2 <sup>nd</sup> stage
NC	14	NC		No Internal Connection
VCC1	15	V <sub>CC1</sub>	PWR	PWR power supply, 1 <sup>st</sup> stage
NC	16	No Connection		No Internal Connection

1. I=Input, O=Output

## 4.0 ELECTRICAL SPECIFICATIONS

The DC and RF specifications for the power amplifier are specified below. Refer to [Table 4-2](#) for the DC voltage and current specifications.

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pin 1 ( $P_{IN}$ ) <sup>1</sup>	+12 dBm
Supply voltage at pins 4, 10, 11, 13 and 15 ( $V_{CC}$ )	+6 V
Enable voltage to pin 2 ( $V_{PEN}$ )	+3.2 V
DC supply current ( $I_{CC}$ )	600 mA
Operating Temperature ( $T_A$ )	-40°C to +85°C
Storage Temperature ( $T_{STG}$ )	-40°C to +120°C
Maximum Junction Temperature ( $T_J$ )	+150°C
Surface Mount Solder Reflow Temperature	260°C for 10 seconds

1. Maximum input power for  $V_{CC} = 5V$  with 50% duty cycle, 802.11g 54 Mbps, with maximum output VSWR = 10:1. At  $V_{CC} > 5V$ , a 10 $\Omega$  resistor must be included on  $V_{CC1}$ , as shown in [Figures 5-8 and 5-9](#).

**TABLE 4-1: OPERATING RANGE**

Range	Ambient Temp	$V_{CC}$
Industrial	-40°C to +85°C	3.0V to 5.5V

**TABLE 4-2: DC ELECTRICAL CHARACTERISTICS AT 25°C,  $V_{CC} = 5V$**

Symbol	Parameter	Min.	Typ	Max.	Unit
$V_{CC}$	Supply Voltage	3.0	5.0	5.5	V
$I_{CC}$	DC Current				
	for 802.11g, 28 dBm, $V_{CC} = 5.0V$		440		mA
	for 802.11b, 28 dBm, $V_{CC} = 5.0V$		440		mA
	for 802.11g, 21 dBm, $V_{CC} = 3.3V$		240		mA
$I_{CQ}$	Idle Current, $V_{CC} = 5.0V$		275		mA
	Idle Current, $V_{CC} = 3.3V$		155		mA
$V_{PEN}$	Enable Voltage see <a href="#">Figure 5-8 on page 10</a>	2.9	2.95	3.1	V
$I_{PEN}$	Enable Current		8		mA

**TABLE 4-3: AC ELECTRICAL CHARACTERISTICS FOR CONFIGURATION AT  $V_{CC} = 5V$ ,  $V_{PEN} = 2.95V$ , 25°C, 50% DUTY CYCLE**

Symbol	Parameter	Min.	Typ	Max.	Unit
$F_{L-U}$	Frequency range in 802.11b/g/n/256 QAM applications	2400		2500	MHz
$P_{OUT}$	Output power at 3% EVM with 802.11g OFDM at 54 Mbps		25		dBm
	Output power at 2.5% EVM with 802.11n MCS7-HT20		24		dBm
	Output power at 1.75% EVM with 256 QAM MCS9-VHT40		23		dBm
	Output power meeting 802.11g spectral mask, 6 Mbps		28		dBm
	Output power meeting 802.11n HT20 spectral mask		27		dBm
	Output power meeting MCS0-HT40 spectral mask		26.5		dBm
	Output power meeting 802.11b spectral mask with 11 Mbps CCK		28		dBm
G	Power gain for 802.11b/g/n/256 QAM	37	39		dB
$G_{VAR}$	Gain variation over band			±0.5	dB
2f	Second Harmonic at 29 dBm, 802.11b mask compliance <sup>1</sup>		-50		dBm/MHz
3f	Third Harmonic at 29 dBm, 802.11b mask compliance <sup>1</sup>		-50		dBm/MHz

1. Harmonic rejection is possible with a simple LC filter, as shown in [Figure 5-9](#).

**TABLE 4-4: AC ELECTRICAL CHARACTERISTICS FOR CONFIGURATION AT  $V_{CC} = 3.3V$ ,  $V_{PEN} = 2.9V$ , 25°C, 50% DUTY CYCLE**

Symbol	Parameter	Min.	Typ	Max.	Unit
$F_{L-U}$	Frequency range in 802.11b/g/n/256 QAM applications	2400		2500	MHz
$P_{OUT}$	Output power at 3% EVM with 802.11g OFDM at 54 Mbps		21		dBm
	Output power at 2.5% EVM with 802.11n MCS7-HT20		20.5		dBm
	Output power at 2.5% EVM with 802.11n MCS7-HT40		20		dBm
	Output power at 1.75% EVM with 256 QAM MCS9-VHT40		18.5		dBm
	Output power meeting 802.11b spectral mask with 11 Mbps CCK		25		dBm
G	Power gain for 802.11b/g/n/256 QAM	35	37		dB
$G_{VAR}$	Gain variation over band			-0.5	dB
2f	Second Harmonic at 25 dBm, 802.11b mask compliance <sup>1</sup>		-60		dBm/MHz
3f	Third Harmonic at 25 dBm, 802.11b mask compliance <sup>1</sup>		-60		dBm/MHz

1. Harmonic rejection is possible with a simple LC filter, as shown in [Figure 5-9](#).

## 5.0 TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions:  $V_{CC} = 5.0V$ ,  $V_{PEN} = 2.95V$ ,  $T_A = 25^\circ C$ , IEEE 802.11g, 54 Mbps, 50% duty cycle unless otherwise specified

FIGURE 5-1: S-PARAMETER

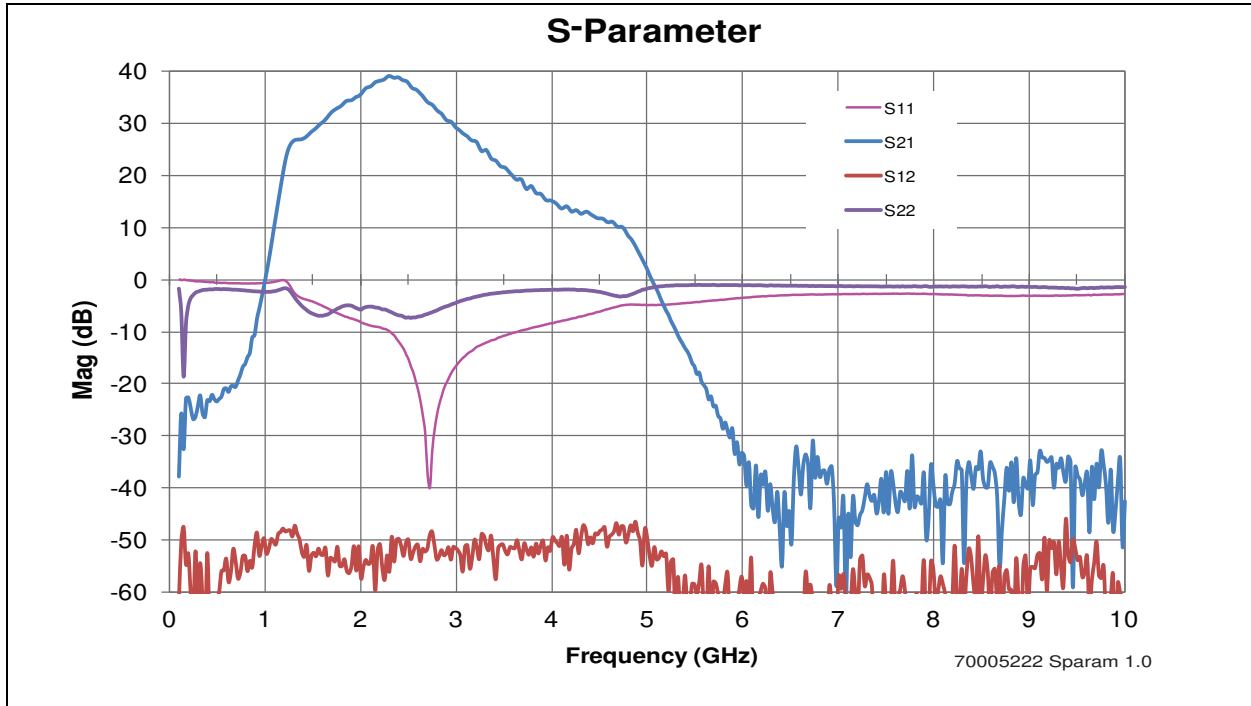


FIGURE 5-2: DYNAMIC EVM VERSUS OUTPUT POWER

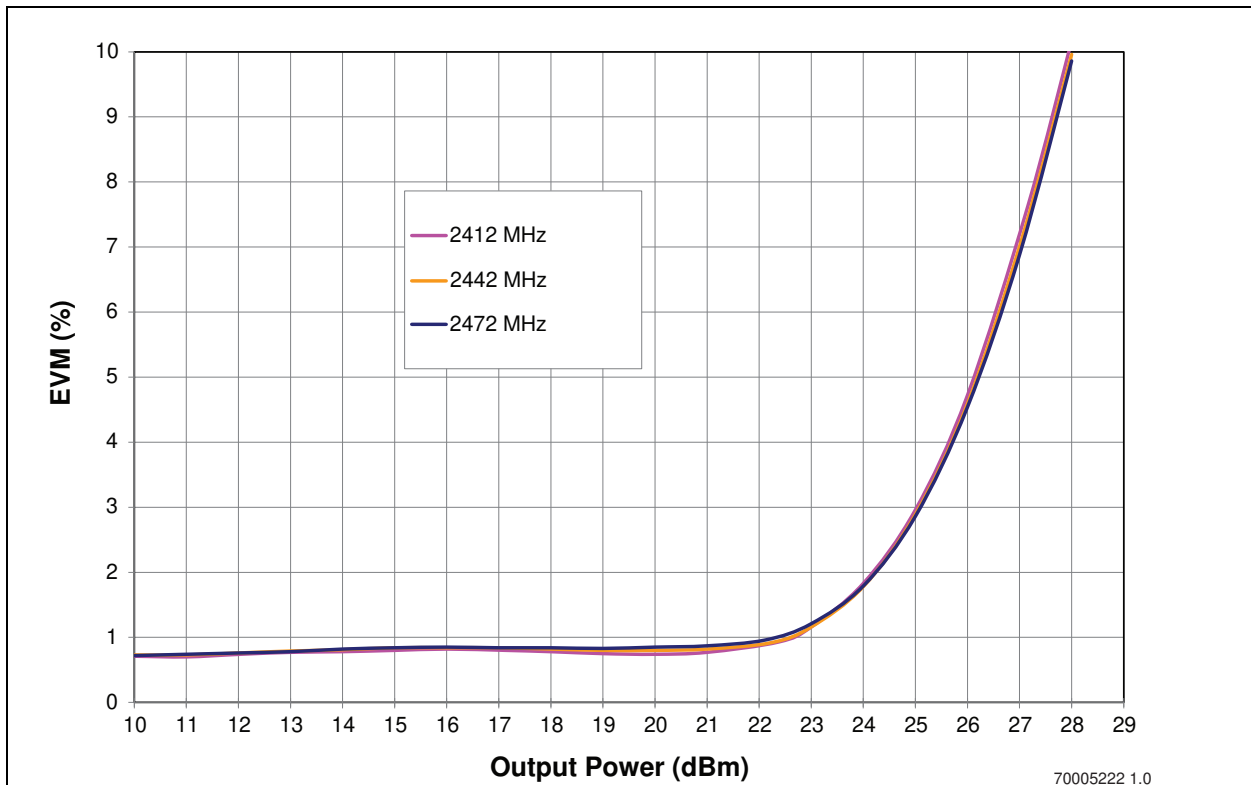
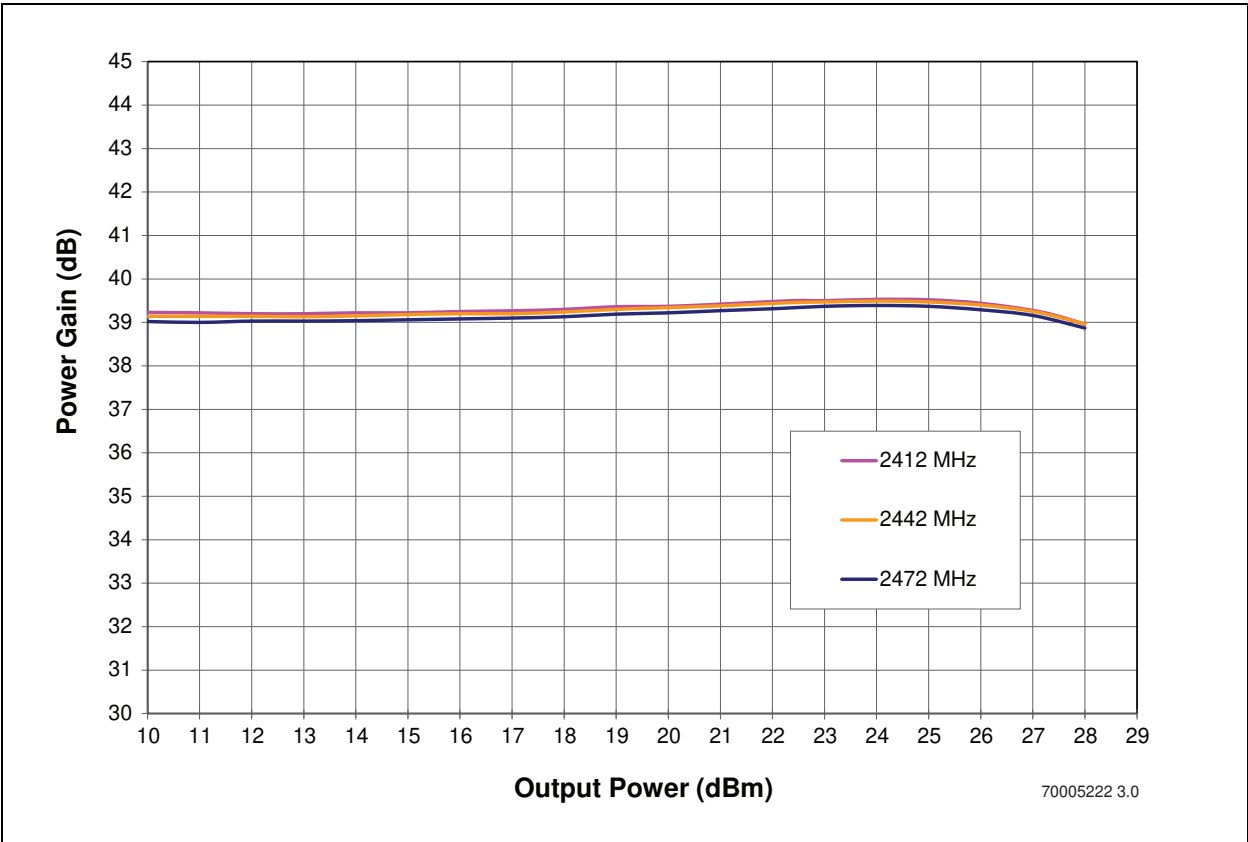




FIGURE 5-3: DYNAMIC EVM VERSUS OUTPUT POWER 802.11AC, MCS9-VHT40, 50% DUTY CYCLE



FIGURE 5-4: POWER GAIN VERSUS OUTPUT POWER



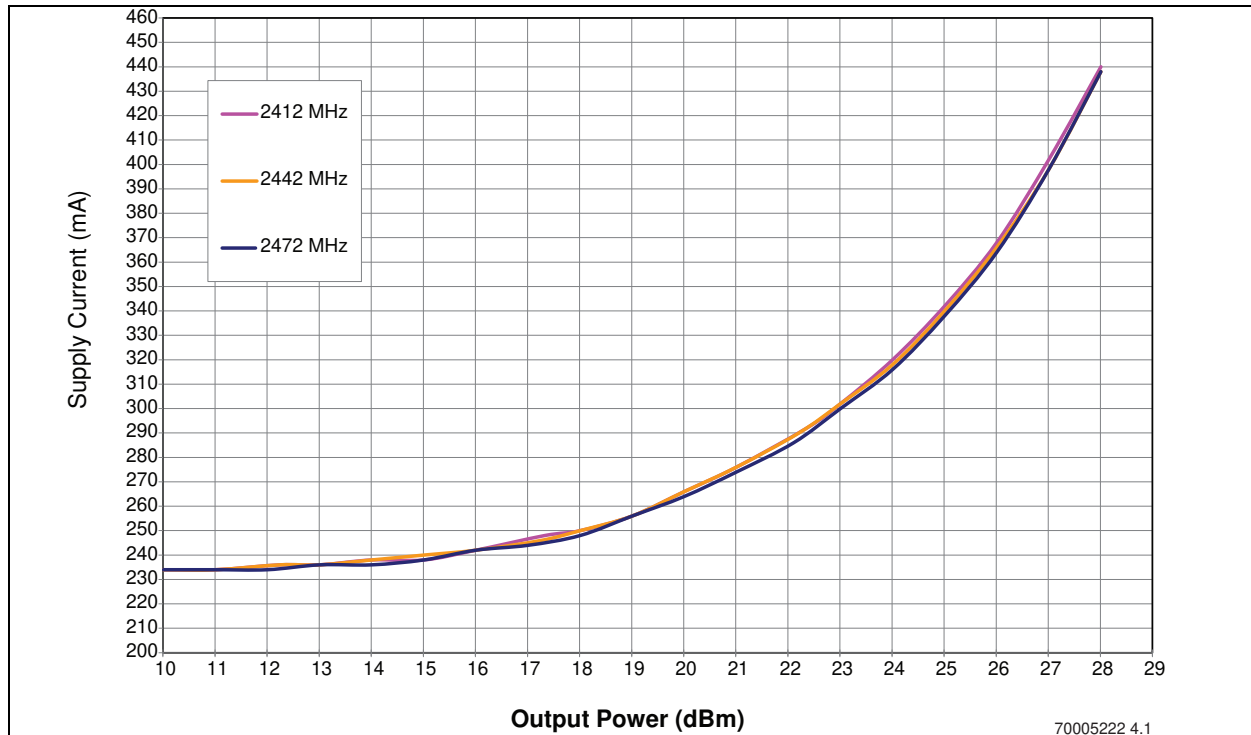
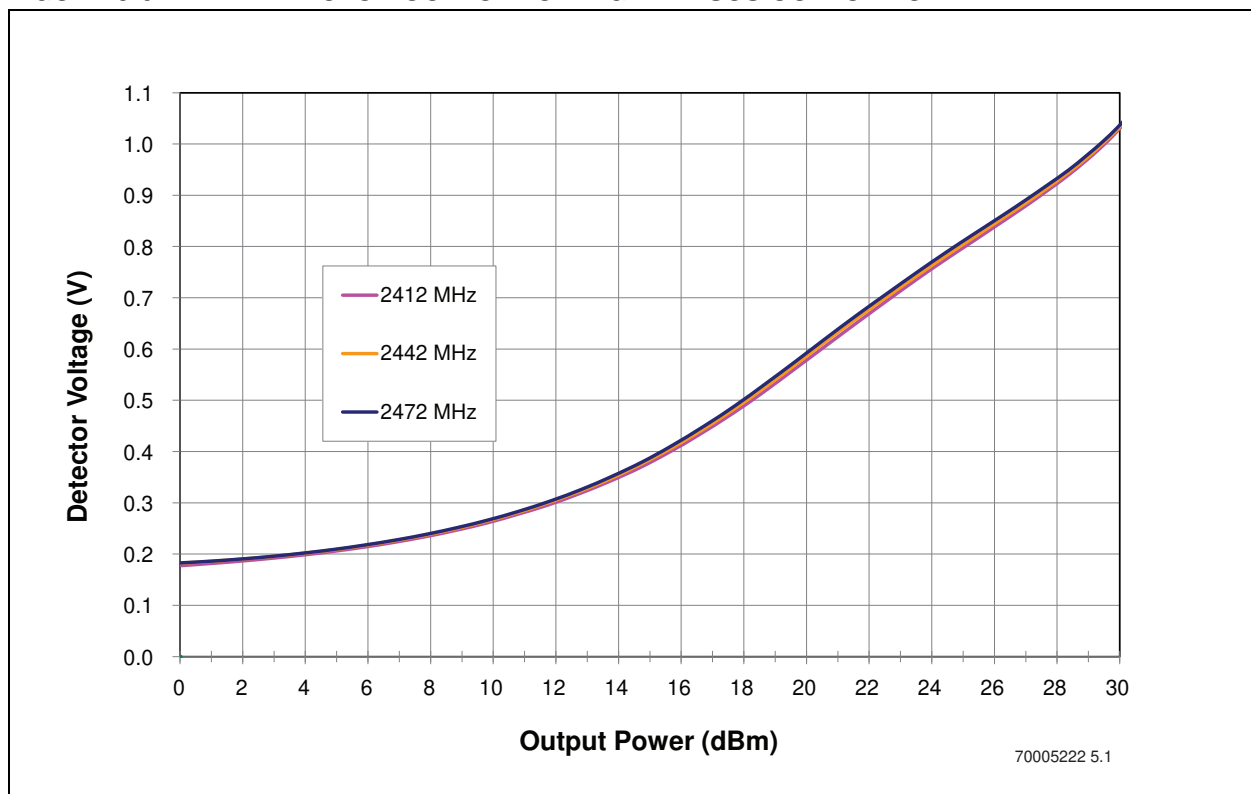
**FIGURE 5-5: DC CURRENT VERSUS OUTPUT POWER****FIGURE 5-6: DETECTOR OUTPUT VOLTAGE VERSUS OUTPUT POWER**

FIGURE 5-7: DYNAMIC EVM VERSUS OUTPUT POWER (WITH HARMONIC FILTER), MCS7-HT40

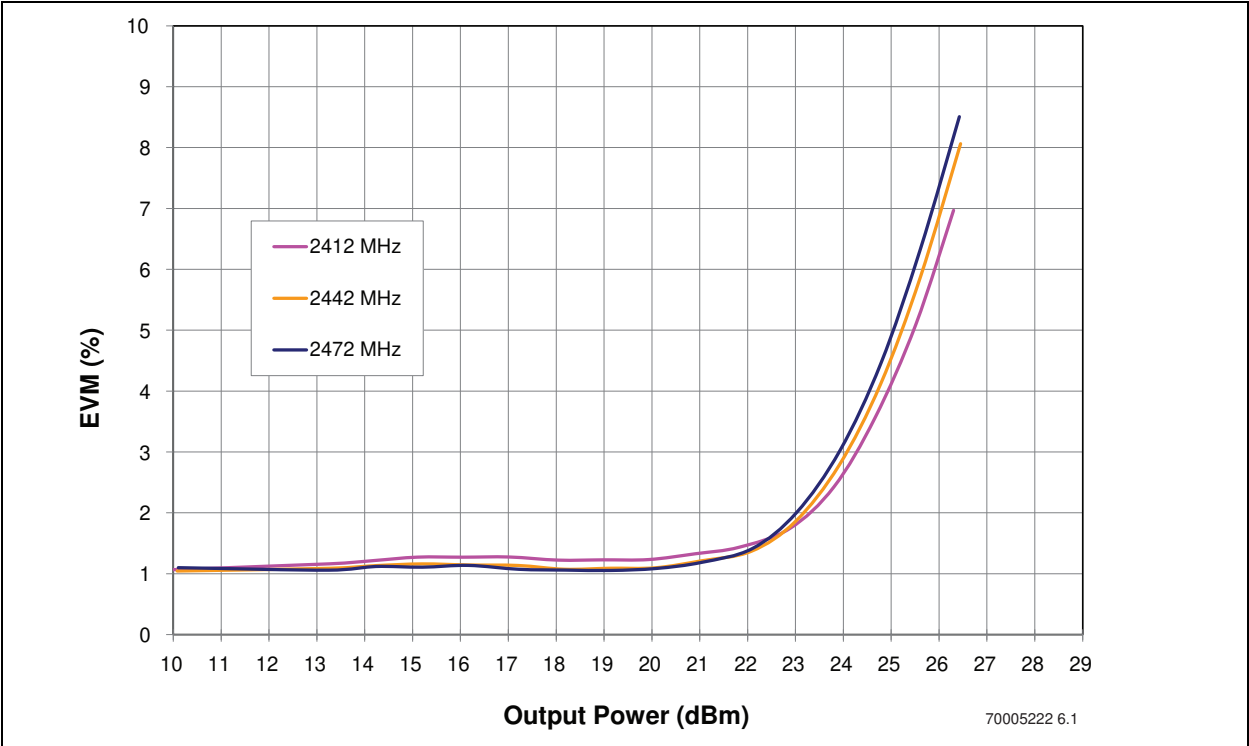
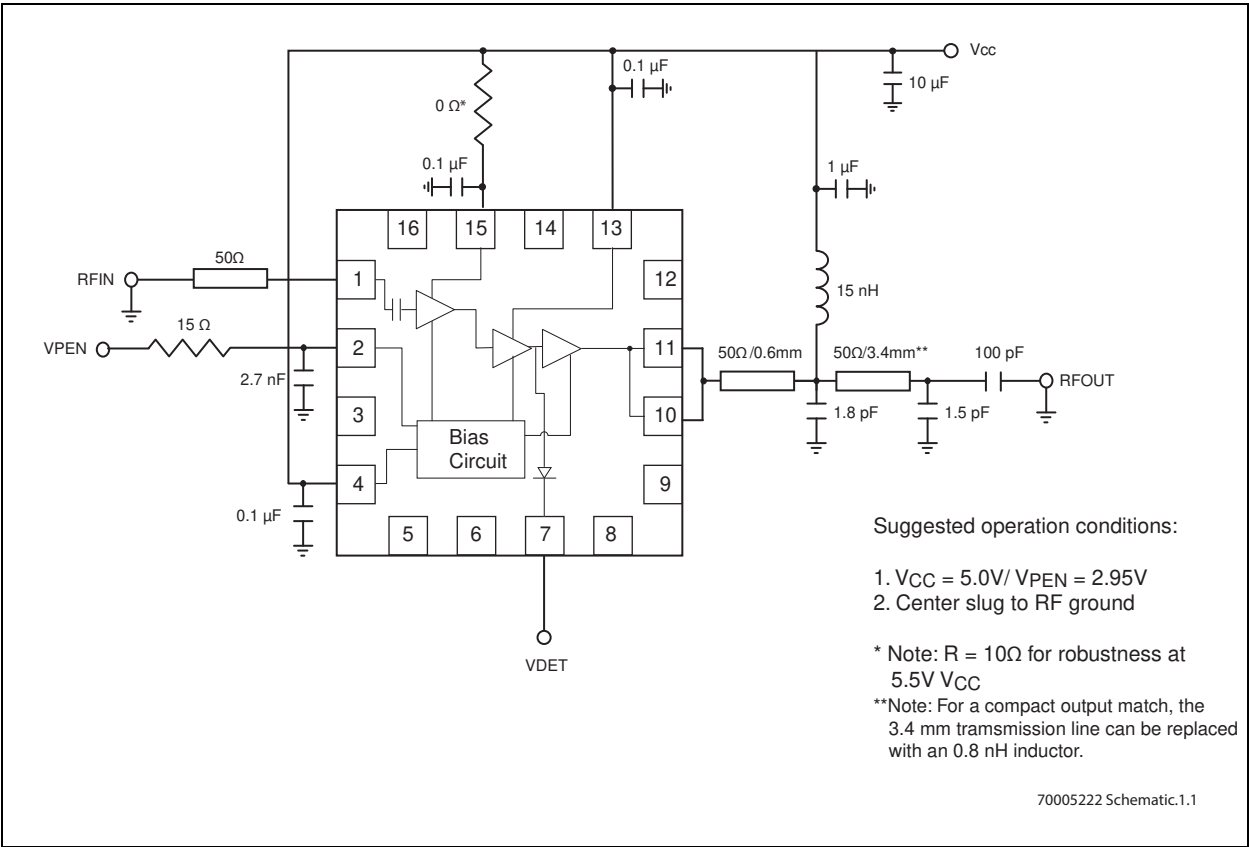
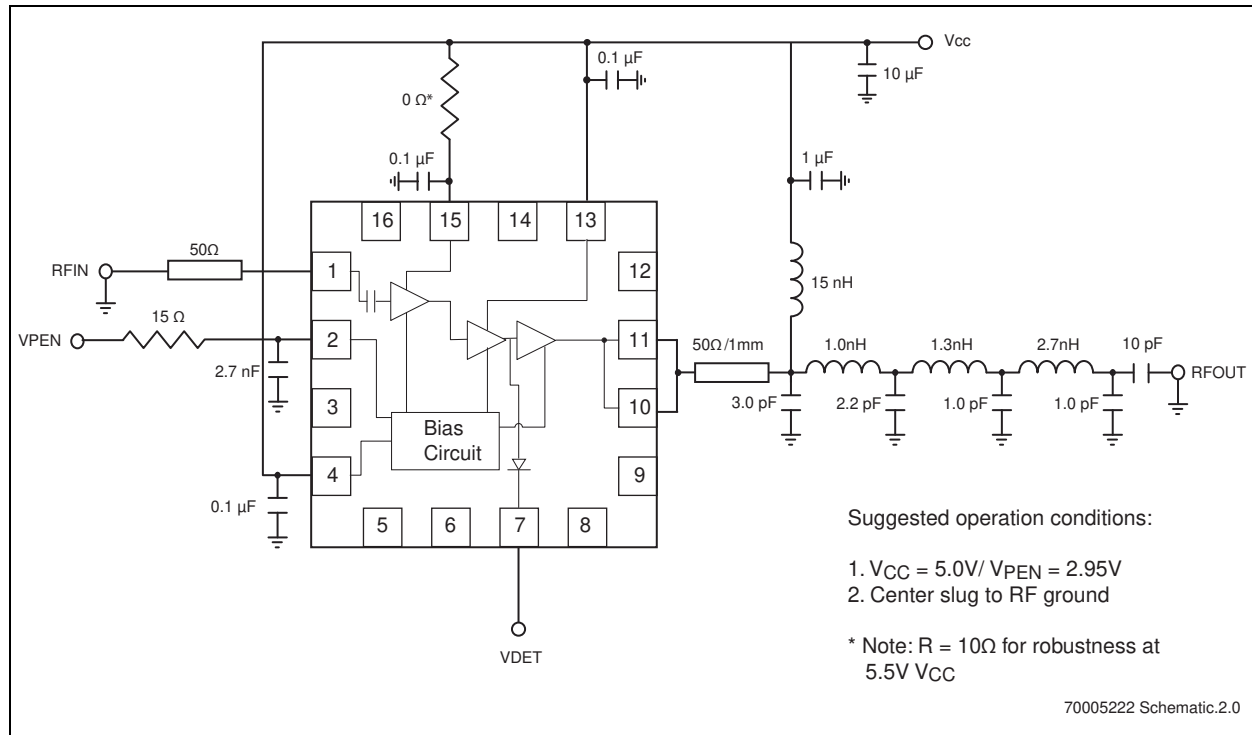


FIGURE 5-8: TYPICAL SCHEMATIC FOR 256 QAM APPLICATIONS

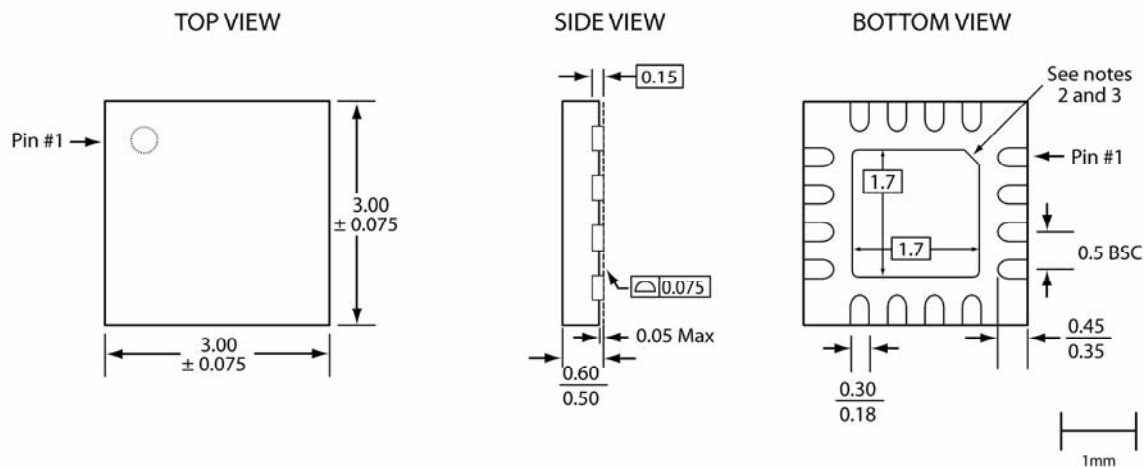


**FIGURE 5-9: SCHEMATIC WITH HARMONIC FILTER FOR 256 QAM APPLICATIONS**

## 6.0 PACKAGING DIAGRAMS

### 16-Lead Ultra Thin Quad Flatpack No-Leads (QUCE/F) - 3x3 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



16-uqfn-3x3-QUC-0.0

**Note:**

1. Complies with JEDEC JEP95 MO-248D, variant UEED-4 except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

**TABLE 6-1: REVISION HISTORY**

Revision	Description	Date
A	<ul style="list-style-type: none"><li>Initial release of data sheet</li></ul>	Apr 2015
B	<ul style="list-style-type: none"><li>Added <a href="#">Table 4-4 on page 6</a></li><li>Removed “Preliminary” status</li><li>Added 3.3V information</li></ul>	Jul 2015



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<div> <div>Device:</div> <div>SST12CP33</div> <div>= 2.4 GHz High-Gain, High-Efficiency Power Amplifier</div> </div> <div> <div>Package:</div> <div>QUCE</div> <div>= UQFN (3mm x 3mm), 0.6 max thickness 16-contact</div> </div> <div> <div>Evaluation Kit</div> <div>K</div> <div>= Evaluation Kit</div> </div> <div>Flag</div>	

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