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SST26WF064C

1.8V, 64 Mbit Serial Quad I/O (SQI) Flash Memory

Features

- Single Voltage Read and Write Operations
  - 1.65-1.95V
- Serial Interface Architecture
  - Mode 0 and Mode 3
  - Nibble-wide multiplexed I/O's with SPI-like serial command structure
  - x1/x2/x4 Serial Peripheral Interface (SPI) Protocol
  - Dual-Transfer Rate (DTR) Operation
- High Speed Clock Frequency
  - 104 MHz max
  - 54 MHz max (DTR)
- Burst Modes
  - Continuous linear burst
  - 8/16/32/64 Byte linear burst with wrap-around
- Superior Reliability
  - Endurance: 100,000 Cycles (min)
  - Greater than 100 years Data Retention
- Low Power Consumption:
  - Active Read current: 15 mA (typical @ 104 MHz)
  - Standby current: 10 µA (typical)
  - Deep Power-Down current: 2.5 µA (typical)
- Fast Erase Time
  - Sector/Block Erase: 18 ms (typ), 25 ms (max)
  - Chip Erase: 35 ms (typ), 50 ms (max)
- Page-Program
  - 256 Bytes per page in x1 or x4 mode
- End-of-Write Detection
  - Software polling the BUSY bit in status register
- Flexible Erase Capability
  - Uniform 4 KByte sectors
  - Four 8 KByte top and bottom parameter overlay blocks
  - One 32 KByte top and bottom overlay block
  - Uniform 64 KByte overlay blocks
- Write-Suspend
  - Suspend Program or Erase operation to access another block/sector
- Software Reset (RST) mode
- Hardware Reset Pin
- Supports JEDEC-compliant Serial Flash Discoverable Parameter (SFDP) table
- Software Protection
  - Individual-Block Write Protection with permanent lock-down capability
    - 64 KByte blocks, two 32 KByte blocks, and eight 8 KByte parameter blocks
  - Read Protection on top and bottom 8 KByte parameter blocks
- Security ID
  - One-Time Programmable (OTP) 2 KByte, Secure ID
    - 64 bit unique, factory pre-programmed identifier
    - User-programmable area
- Temperature Range
  - Industrial: -40°C to +85°C
- Packages Available
  - 8-contact WDFN (6mm x 5mm)
  - 8-lead SOIJ (5.28 mm)
  - 16-lead SOIC (7.50 mm)
  - 24-ball TBGA (8mm x 6mm)
- All devices are RoHS compliant

Product Description

The Serial Quad I/O™ (SQI™) family of flash-memory devices features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package. The SST26WF064C also supports full command-set compatibility to traditional Serial Peripheral Interface (SPI) protocol. System designs using SQI flash devices occupy less board space and ultimately lower system costs.

All members of the 26 Series, SQI family are manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST26WF064C significantly improves performance and reliability, while lowering power consumption. These devices write (Program or Erase) with a single power supply of 1.65-1.95V. The total energy consumed is a function of the applied voltage, current, and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time. Therefore, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

The SST26WF064C is offered in 8-contact WDFN (6 mm x 5 mm), 8-lead SOIJ (5.28 mm), 16-lead SOIC (7.50 mm), and 24-ball TBGA (8mm x 6mm) packages. See Figure 2-1 for pin assignments.

The following configuration is available upon order:

- SST26WF064C default at power-up has the WP# and RESET#/HOLD# pins enabled, with the SIO2 and SIO3 pins disabled, to initiate SPI-protocol.

See "I/O Configuration (IOC)" on page 13 for more information about configuring the WP#, RESET/HOLD#, SIO2, and SIO3 pins.

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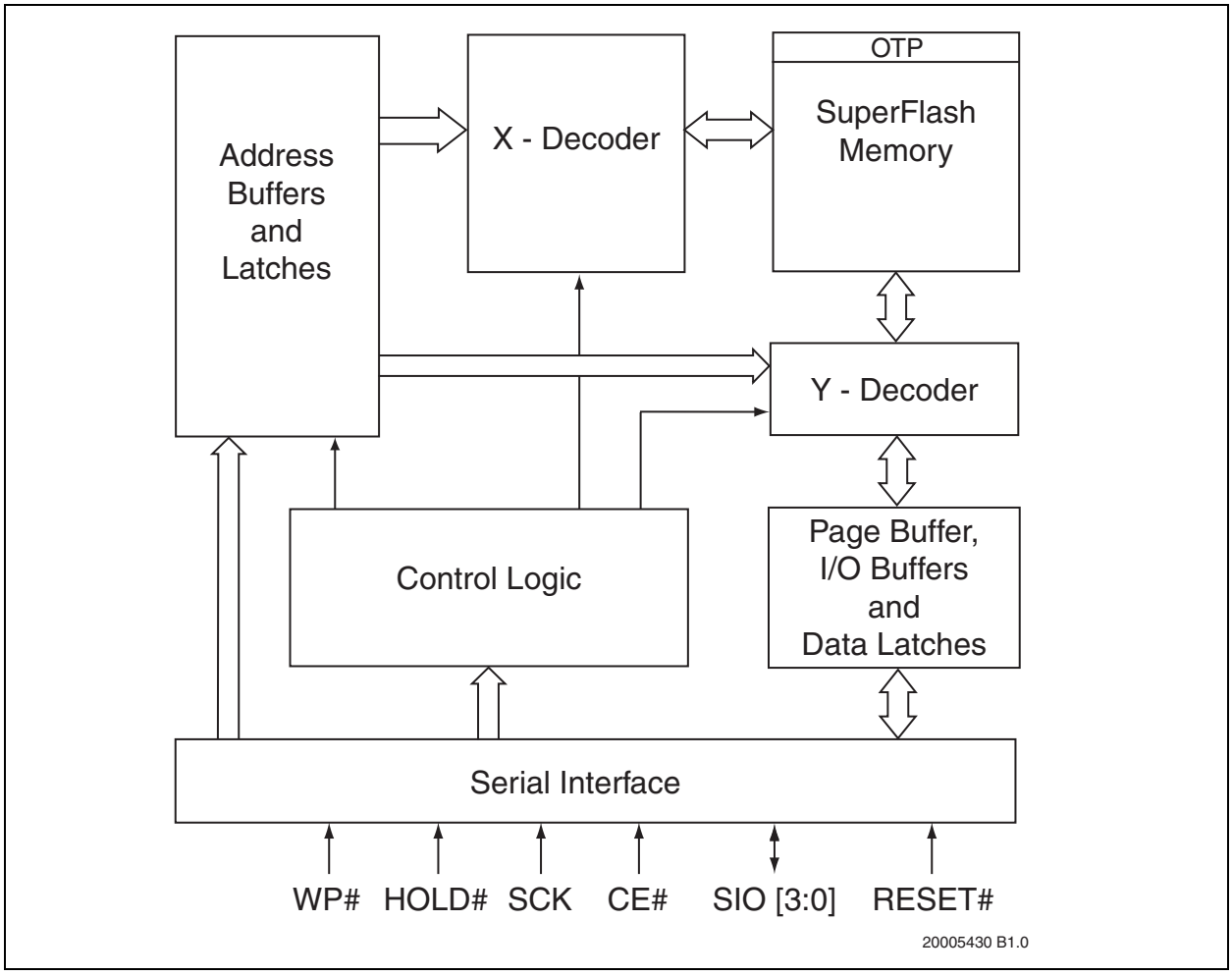
1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN DESCRIPTIONS

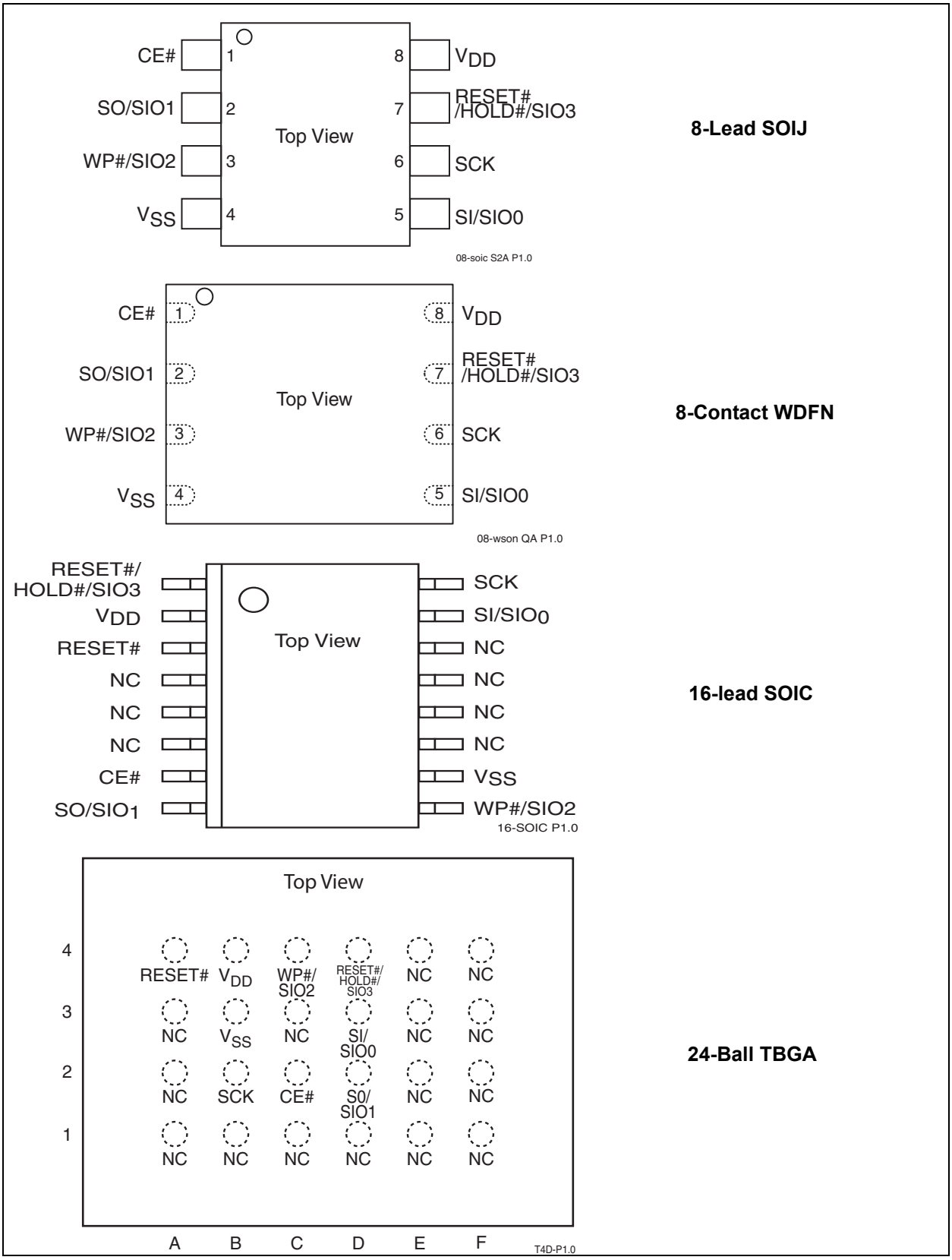


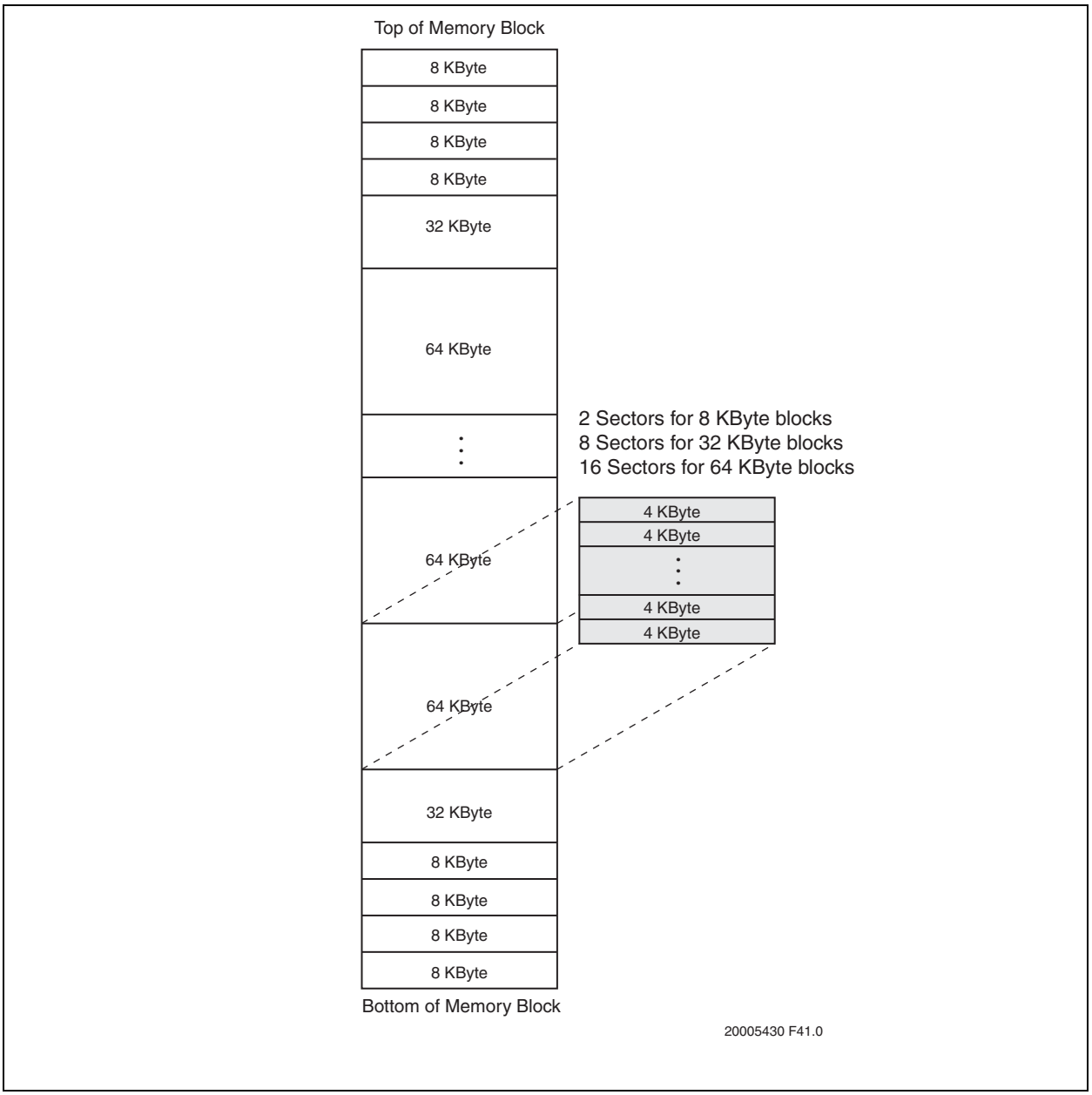
TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	Provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SIO[3:0]	Serial Data Input/Output	Transfer commands, addresses, or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. The Enable Quad I/O (EQIO) command instruction configures these pins for Quad I/O mode.
SI	Serial Data Input for SPI mode	Transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a power on reset or hardware reset.
SO	Serial Data Output for SPI mode	Transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. SO is the default state after a power on reset or hardware reset.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence; or in the case of Write operations, for the command/data input sequence.
WP#	Write Protect	The WP# pin is used in conjunction with the WPEN and IOC bits in the configuration register to prohibit Write operations to the Block-Protection register. This pin only works in SPI, single-bit and dual-bit Read mode.
HOLD#	Hold	Temporarily stops serial communication with the SPI Flash memory while the device is selected. This pin only works in SPI, single-bit and dual-bit Read mode and must be tied high when not in use.
RESET#	Reset	Reset the operation and internal logic of the device.
V_{DD}	Power Supply	Provide power supply voltage.
V_{SS}	Ground	

3.0 MEMORY ORGANIZATION

The SST26WF064C SQI memory array is organized in uniform, 4 KByte erasable sectors with the following erasable blocks: eight 8 KByte parameters, two 32 KByte overlays, and one hundred twenty-six 64 KByte overlay blocks. See Figure 3-1.

FIGURE 3-1: MEMORY MAP



4.0 DEVICE OPERATION

The SST26WF064C supports both Serial Peripheral Interface (SPI) bus protocol and a 4-bit multiplexed SQI bus protocol. To provide backward compatibility to traditional SPI Serial Flash devices, the device's initial state after a power-on reset is SPI mode which supports multi-I/O (x1/x2/x4) Read/Write commands. A command instruction configures the device to SQI mode. The dataflow in the SQI mode is similar to the SPI mode, except it uses four multiplexed I/O signals for command, address, and data sequence.

SQI Flash Memory supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus master is in stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) is sampled at the rising edge of the SCK clock signal for input, and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals as shown in Figure 4-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 4-2. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

The SST26WF064C also supports Dual-Transfer Rate (DTR) SPI and SQI commands, during which data is sampled on both the rising and the falling edge of the clock, and data is driven out on both the rising and falling edge of the clock.

FIGURE 4-1: SPI PROTOCOL (TRADITIONAL 25 SERIES SPI DEVICE)

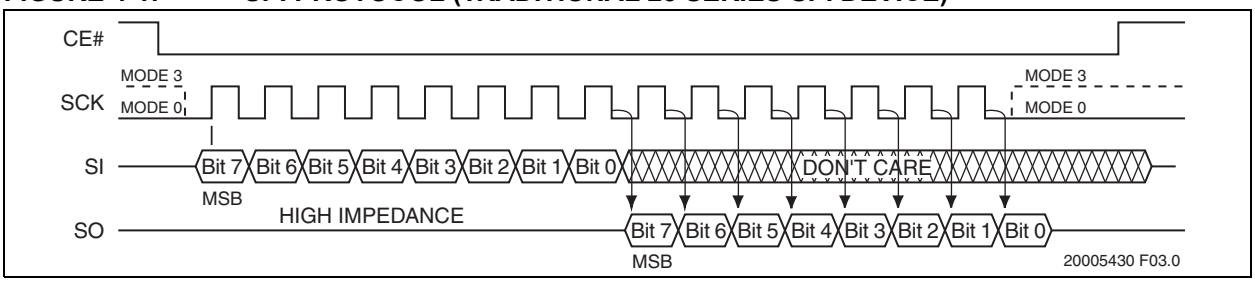
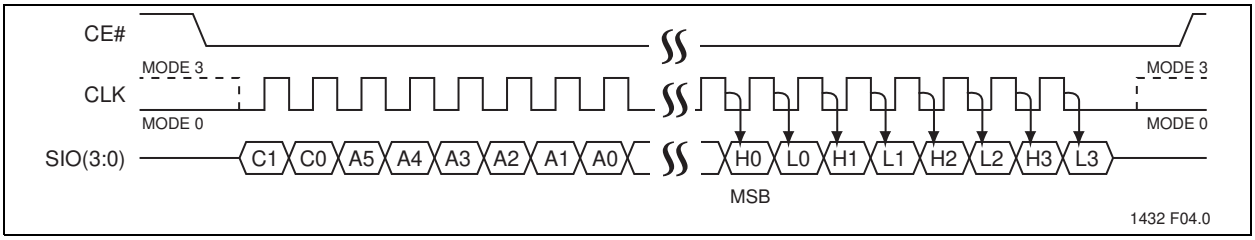


FIGURE 4-2: SQI SERIAL QUAD I/O PROTOCOL



4.1 Device Protection

The SST26WF064C offers a flexible memory protection scheme that allows the protection state of each individual block to be controlled separately. In addition, the Write-Protection Lock-Down register prevents any change of the lock status during device operation. To avoid inadvertent writes during power-up, the device is write-protected by default after a power-on reset cycle. A Global Block-Protection Unlock command offers a single command cycle that unlocks the entire memory array for faster manufacturing throughput.

For extra protection, there is an additional non-volatile register that can permanently write-protect the Block-Protection register bits for each individual block. Each of the corresponding lock-down bits are one time programmable (OTP)—once written, they cannot be erased. Data that had been previously programmed into these blocks cannot be altered by programming or erase and is not reversible

4.1.1 INDIVIDUAL BLOCK PROTECTION

The SST26WF064C has a Block-Protection register which provides a software mechanism to write-lock the individual memory blocks and write-lock, and/or read-lock, the individual parameter blocks. The Block-Protection register is 144 bits wide: two bits each for the eight 8 KByte parameter blocks (write-lock and read-lock), and one bit each for the remaining 32 KByte and 64 KByte overlay blocks (write-lock). See Table 5-6 for address range protected per register bit.

Each bit in the Block-Protection register (BPR) can be written to a '1' (protected) or '0' (unprotected). For the parameter blocks, the most significant bit is for read-lock, and the least significant bit is for write-lock. Read-locking the parameter blocks provides additional security for sensitive data after retrieval (e.g., after initial boot). If a block is read-locked all reads to the block return data 00H.

The Write Block-Protection Register command is a two-cycle command which requires that Write-Enable (WREN) is executed prior to the Write Block-Protection Register command. The Global Block-Protection Unlock command clears all write protection bits in the Block-Protection register.

4.1.2 WRITE-PROTECTION LOCK-DOWN (VOLATILE)

To prevent changes to the Block-Protection register, use the Lock-Down Block-Protection Register (LBPR) command to enable Write-Protection Lock-Down. Once Write-Protection Lock-Down is enabled, the Block-Protection register can not be changed. To avoid inadvertent lock down, the WREN command must be executed prior to the LBPR command.

To reset Write-Protection Lock-Down, performing a power cycle or hardware reset on the device is required. The Write-Protection Lock-Down status may be read from the Status register.

4.1.3 WRITE-LOCK LOCK-DOWN (NON-VOLATILE)

The non-Volatile Write-Lock Lock-Down register is an alternate register that permanently prevents changes to the block-protect bits. The non-Volatile Write-Lock Lock-Down register (nVWLDR) is 136 bits wide per device: one bit each for the eight 8-KByte parameter blocks, and one bit each for the remaining 32 KByte and 64 KByte overlay blocks. See Table 5-6 for address range protected per register bit.

Writing '1' to any or all of the nVWLDR bits disables the change mechanism for the corresponding Write-Lock bit in the BPR, and permanently sets this bit to a '1' (protected) state. After this change, both bits will be set to '1', regardless of the data entered in subsequent writes to either the nVWLDR or the BPR. Subsequent writes to the nVWLDR can only alter available locations that have not been previously written to a '1'. This method provides write-protection for the corresponding memory-array block by protecting it from future program or erase operations.

Writing a '0' in any location in the nVWLDR has no effect on either the nVWLDR or the corresponding Write-Lock bit in the BPR.

Note that if the Block-Protection register had been previously locked down, see "Write-Protection Lock-Down (Volatile)", the device must be power cycled before using the nVWLDR. If the Block-Protection Register is locked down and the Write nVWLDR command is accessed, the command will be ignored.

4.2 Hardware Write Protection

The hardware Write Protection pin (WP#) is used in conjunction with the WPEN and IOC bits in the configuration register to prohibit write operations to the Block-Protection and Configuration registers. The WP# pin function only works in SPI single-bit and dual-bit read mode when the IOC bit in the configuration register is set to '0'.

The WP# pin function is disabled when the WPEN bit in the configuration register is '0'. This allows installation of the SST26WF064C in a system with a grounded WP# pin while still enabling Write to the Block-Protection register. The Lock-Down function of the Block-Protection Register supersedes the WP# pin, see Table 4-1 for Write Protection Lock-Down states.

The factory default setting at power-up of the WPEN bit is '0', disabling the Write Protect function of the WP# after power-up. WPEN is a non-volatile bit; once the bit is set to '1', the Write Protect function of the WP# pin continues to be enabled after power-up. The WP# pin only protects the Block-Protection Register and Configuration Register from changes. Therefore, if the WP# pin is set to low before or after a Program or Erase command, or while an internal Write is in progress, it will have no effect on the Write command.

The IOC bit takes priority over the WPEN bit in the configuration register. When the IOC bit is '1', the function of the WP# pin is disabled and the WPEN bit serves no function. When the IOC bit is '0' and WPEN is '1', setting the WP# pin active low prohibits Write operations to the Block Protection Register.

TABLE 4-1: WRITE PROTECTION LOCK-DOWN STATES

WP#	IOC	WPEN	WPLD	Block Protection Register	Configuration Register
L	0	1	1	Protected	Protected
L	0	0	1	Protected	Writable
L	0	1	0	Protected	Protected
L	0[1]	0[2]	0	Writable	Writable
H	0	X	1	Protected	Writable
H	0	X	0	Writable	Writable
X	1	X	1	Protected	Writable
X	1	0[2]	0	Writable	Writable

1. Default at power-up Register settings for SST26WF064C
2. Factory default setting is '0'. This is a non-volatile bit; default at power-up is the value set prior to power-down.

4.3 Security ID

The SST26WF064C offers a 2 KByte Security ID (Sec ID) feature. The Security ID space is divided into two parts – one factory-programmed, 64-bit segment and one user-programmable segment. The factory-programmed segment is programmed during manufacturing with a unique number and cannot be changed. The user-programmable segment is left unprogrammed for the customer to program as desired.

Use the Program Security ID (PSID) command to program the Security ID using the address shown in Table 5-5. The Security ID can be locked using the Lockout Security ID (LSID) command. This prevents any future write operations to the Security ID.

The factory-programmed portion of the Security ID can't be programmed by the user; neither the factory-programmed nor user-programmable areas can be erased.

4.4 Hold Operation

The HOLD# pin pauses active serial sequences without resetting the clocking sequence. The RESET#/HOLD#/SIO3 pin provides HOLD capability when configured as a HOLD pin. One factory configuration is available: The SST26WF064C ships with the IOC bit set to '0' and the HOLD# pin function enabled. The HOLD# pin is always disabled in SQI mode and only works in SPI single-bit and dual-bit read mode.

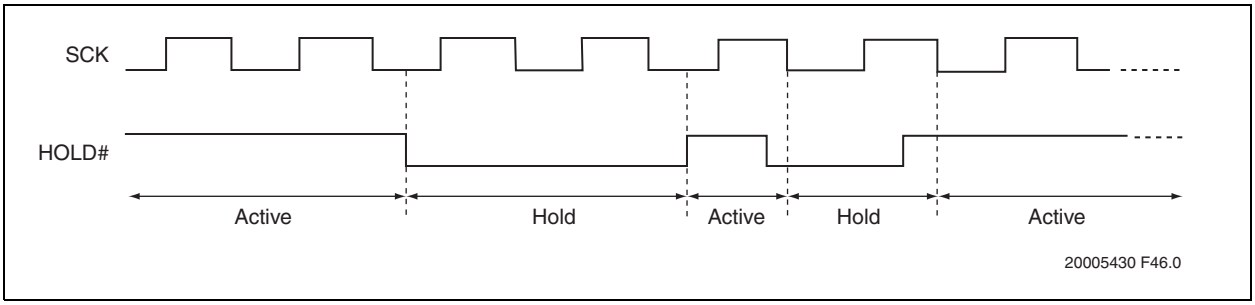
To activate the Hold mode, CE# must be in active low state. The Hold mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The Hold mode ends when the HOLD# signal's rising edge coincides with the SCK active low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active low state, then the device exits Hold mode when the SCK next reaches the active low state. See Figure 4-3.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active high during a Hold condition, it resets the internal logic of the device. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low.

FIGURE 4-3: HOLD CONDITION WAVEFORM.



4.5 Reset Operation

The SST26WF064C supports both hardware and software reset operations. Hardware reset is only allowed using SPI x1 and x2 protocol in 8-pin SOIC and 8-contact WDFN packages. 16-lead SOIC and 24-ball TBGA packages have a dedicated Hardware Reset pin which is allowed in all modes of operations. Software reset commands 66H and 99H are supported in all package options and protocols. See Table 4-2 on page 10 for hardware and software reset functionality.

A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.

4.5.1 HARDWARE RESET OPERATION

To configure the RESET#/HOLD#/SIO3 pin as a RESET# pin in 8-pin SOIC and 8-contact WDFN packages, bit 6 of the configuration register must be set to '1'. The factory default setting of bit 6 is '0'–HOLD# pin enabled. This is a non-volatile bit, so the register value at power-up will be the value prior to power-down. Any pin marked with only RESET# (16-lead SOIC and 24-ball TFBGA packages) is a dedicated RESET# pin and has the same functionality as the multiplex I/O pins.

Driving the RESET# pin high puts the device in normal operating mode. The RESET# pin must be driven low for a minimum of T_{RST} time to reset the device. The SIO1 pin (SO) is in high impedance state while the device is in reset. A successful Reset operation will reset the protocol to SPI mode, clear status register bits (BUSY=0, WEL=0, WSE=0, WSP=0 and WPLD=0) except SEC bit, reset the burst length to 8 Bytes, and write-protect Block-Protection Register bits. A device

reset during an active Program or Erase operation aborts the operation, and data of the targeted address range may be corrupted or lost due to the aborted Erase or Program operation

4.5.2 SOFTWARE RESET OPERATION

The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

Once the Reset-Enable and Reset commands are successfully executed, the device returns to normal operation Read mode and then does the following: resets the protocol to SPI mode, resets the burst length to 8 Bytes, clears all the bits, except for bit 4 (WPLD) and bit 5 (SEC), in the Status register to their default states, and clears bit 1 (IOC) in the configuration register to its default state.

TABLE 4-2: HARDWARE AND SOFTWARE FUNCTIONALITY

Situation	After Power Cycle	After Hardware Reset	After Software Reset
Write Protection bits in protection register	are set to 1	are set to 1	are not affected
Read Protection bits in protection register	are set to 0	are set to 0	are not affected
If the device was in SQI mode and was in a Read mode with configuration bits M[7:0] = AXH, then it will enter SPI mode	Yes	Yes	Mode Read has to be exited before Reset command will be accepted
If the device was in SQI mode and was not in a Read mode with configuration bits M[7:0] = AXH, then it will enter SPI mode	Yes	Yes	Yes
Read Burst length is reset to 8 bytes	Yes	Yes	Yes
Status register:			
Busy=0, WEL=0, WSE=0, WSP=0	Yes	Yes	Yes
WPLD in status register	equal to 0	equal to 0	is not affected
SEC bit	is not affected.	is not affected.	is not affected.
Configuration register:			
If the device was in SQI mode and was in a Read mode with configuration bits M[7:0] = AXH, then the IOC bit	will equal to 0	will equal to 0	Mode Read has to be exited before Reset command will be accepted
If the device was in SQI mode and was not in a Read mode with configuration bits M[7:0] = AXH, then the IOC bit	will equal to 0	will equal to 0	will equal to 0
BPNV bit, RSTHLD bit and WPEN bit	is not affected.	is not affected.	is not affected.

4.6 Status Register

The Status register is a read-only register that provides the following status information: whether the flash memory array is available for any Read or Write operation, if the device is write-enabled, whether an erase or program operation is suspended, and if the Block-Protection register and/or Security ID are locked down. During an internal Erase or Program operation, the Status register may be read to determine the completion of an operation in progress. Table 4-3 describes the function of each bit in the Status register.

TABLE 4-3: STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	Write-Enable Latch status 1 = Device is write-enabled 0 = Device is not write-enabled	0	R
2	WSE	Write Suspend-Erase status 1 = Erase suspended 0 = Erase is not suspended	0	R
3	WSP	Write Suspend-Program status 1 = Program suspended 0 = Program is not suspended	0	R
4	WPLD	Write Protection Lock-Down status 1 = Write Protection Lock-Down enabled 0 = Write Protection Lock-Down disabled	0	R
5	SEC[1]	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0[1]	R
6	RES	Reserved for future use	0	R
7	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R

1. The Security ID status will always be ‘1’ at power-up after a successful execution of the Lockout Security ID instruction, otherwise default at power-up is ‘0’.

4.6.1 WRITE-ENABLE LATCH (WEL)

The Write-Enable Latch (WEL) bit indicates the status of the internal memory’s Write-Enable Latch. If the WEL bit is set to ‘1’, the device is write enabled. If the bit is set to ‘0’ (reset), the device is not write enabled and does not accept any memory Program or Erase, Protection Register Write, or Lock-Down commands. The Write-Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Reset
- Write-Disable (WRDI) instruction
- Page-Program instruction completion
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Write-Block-Protection register instruction
- Lock-Down Block-Protection register instruction
- Program Security ID instruction completion
- Lockout Security ID instruction completion
- Write-Suspend instruction
- SPI Quad Page Program
- Write Status Register

4.6.2 WRITE SUSPEND ERASE STATUS (WSE)

The Write Suspend-Erase status (WSE) indicates when an Erase operation has been suspended. The WSE bit is ‘1’ after the host issues a suspend command during an Erase operation. Once the suspended Erase resumes, the WSE bit is reset to ‘0’.

4.6.3 WRITE SUSPEND PROGRAM STATUS (WSP)

The Write Suspend-Program status (WSP) bit indicates when a Program operation has been suspended. The WSP is ‘1’ after the host issues a suspend command during the Program operation. Once the suspended Program resumes, the WSP bit is reset to ‘0’.

4.6.4 WRITE PROTECTION LOCK-DOWN STATUS (WPLD)

The Write Protection Lock-Down status (WPLD) bit indicates when the Block-Protection register is locked-down to prevent changes to the protection settings. The WPLD is ‘1’ after the host issues a Lock-Down Block-Protection command. After a power cycle, the WPLD bit is reset to ‘0’.

4.6.5 SECURITY ID STATUS (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a Write command. The SEC is ‘1’ after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to ‘0.’

4.6.6 BUSY

The Busy bit determines whether there is an internal Erase or Program operation in progress. If the BUSY bit is ‘1’, the device is busy with an internal Erase or Program operation. If the bit is ‘0’, no Erase or Program operation is in progress.

4.7 Configuration Register

The Configuration register is a Read/Write register that stores a variety of configuration information. See Table 4-4 for the function of each bit in the register.

TABLE 4-4: CONFIGURATION REGISTER

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	RES	Reserved	0	R
1	IOC	I/O Configuration 1 = WP# and RESET# or HOLD# pins disabled 0 = WP# and RESET# or HOLD# pins enabled	0[1]	R/W
2	RES	Reserved	0	R
3	BPNV	Block-Protection Volatility State 1 = No memory block has been permanently locked 0 = Any block has been permanently locked	1	R
4	RES	Reserved	0	R
5	RES	Reserved	0	R
6	RSTHLD	RESET# pin or HOLD# pin Enable 1 = RESET# pin enabled 0 = HOLD# pin enabled	0[2]	R/W
7	WPEN	Write-Protection Pin (WP#) Enable 1 = WP# enabled 0 = WP# disabled	0[2]	R/W

1. SST26WF064C default at Power-up is ‘0’
2. Factory default setting. This is a non-volatile bit; default at power-up will be the setting prior to power-down.

4.7.1 I/O CONFIGURATION (IOC)

The I/O Configuration (IOC) bit re-configures the I/O pins. The IOC bit is set by writing a ‘1’ to Bit 1 of the Configuration register. When IOC bit is ‘0’ the WP# pin and HOLD# pin are enabled (SPI or Dual Configuration setup). When IOC bit is set to ‘1’ the SIO2 pin and SIO3 pin are enabled (SPI Quad I/O Configuration setup). The IOC bit must be set to ‘1’ before issuing the following SPI commands: SQOR (6BH), SQIOR (EBH), RBSPI (ECH), SPI Quad page program (32H), SQOR-DTR (6DH), and SQIOR-DTR (EDH). Without setting the IOC bit to ‘1’, those SPI commands are not valid. The I/O configuration bit does not apply when in SQI mode. The default at power-up for the SST26WF064C is ‘0’.

4.7.2 BLOCK-PROTECTION VOLATILITY STATE (BPNV)

The Block-Protection Volatility State bit indicates whether any block has been permanently locked with the non-Volatile Write-Lock Lock-Down register (nVWLDR). When no bits in the nVWLDR have been set (the default state from the factory) the BPNV bit is `1'; when one or more bits in the nVWLDR are set to `1' the BPNV bit will also be `0' from that point forward, even after power-up.

4.7.3 RESET/HOLD ENABLE (RSTHLD)

The Reset/Hold Enable (RSTHLD) bit is a non-volatile bit that configures RESET#/HOLD#/SIO3 pin to be either Reset# pin or Hold# pin.

4.7.4 WRITE-PROTECT ENABLE (WPEN)

The Write-Protect Enable (WPEN) bit is a non-volatile bit that enables the WP# pin.

The Write-Protect (WP#) pin and the Write-Protect Enable (WPEN) bit control the programmable hardware write-protect feature. Setting the WP# pin to low, and the WPEN bit to ‘1’, enables Hardware write-protection. To disable Hardware write protection, set either the WP# pin to high or the WPEN bit to ‘0’. There is latency associated with writing to the WPEN bit. Poll the BUSY bit in the Status register, or wait T_{WPEN}, for the completion of the internal, self-timed Write operation. When the chip is hardware write protected, only Write operations to Block-Protection and Configuration registers are disabled.See “Hardware Write Protection” on page 8 and Table 4-1 for more information about the functionality of the WPEN bit.

5.0 INSTRUCTIONS

Instructions are used to read, write (erase and program), and configure the SST26WF064C. The complete list of the instructions is provided in Table 5-1.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26WF064C (1 OF 2)

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq
			SPI	SQI				
Configuration								
NOP	No Operation	00H	X	X	0	0	0	104 MHz
RSTEN	Reset Enable	66H	X	X	0	0	0	
RST[4]	Reset Memory	99H	X	X	0	0	0	
EQIO	Enable Quad I/O	38H	X		0	0	0	
RSTQIO[5]	Reset Quad I/O	FFH	X	X	0	0	0	
RDSR	Read Status Register	05H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
WRSR	Write Status Register	01H	X	X	0	0	2	
RDCR	Read Configuration Register	35H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
Read								
Read	Read Memory	03H	X		3	0	1 to ∞	40 MHz
High-Speed Read	Read Memory at Higher Speed	0BH		X	3	3	1 to ∞	104 MHz
			X		3	1	1 to ∞	
SQOR[6]	SPI Quad Output Read	6BH	X		3	1	1 to ∞	
SQIOR[7]	SPI Quad I/O Read	EBH	X		3	3	1 to ∞	
SDOR[8]	SPI Dual Output Read	3BH	X		3	1	1 to ∞	
SDIOR[9]	SPI Dual I/O Read	BBH	X		3	1	1 to ∞	80 MHz
SB	Set Burst Length	C0H	X	X	0	0	1	104 MHz
RBSQI	SQI nB Burst with Wrap	0CH		X	3	3	n to ∞	
RBSPI[7]	SPI nB Burst with Wrap	ECH	X		3	3	n to ∞	
High-Speed Read - DTR[10]	Read Memory at Higher Speed - DTR	0DH	X		12	6	1 to ∞	54 MHz
				X	3	6	1 to ∞	
SQOR - DTR[10,11]	SPI Quad Output Read - DTR	6DH	X		12	6	1 to ∞	
SQIOR - DTR[10,11]	SPI Quad I/O Read - DTR	EDH	X		3	6	1 to ∞	
SDOR - DTR[10]	SPI Dual-Output Read - DTR	3DH	X		12	6	1 to ∞	
SDIOR - DTR[10]	SPI Dual-I/O Read - DTR	BDH	X		6	6	1 to ∞	
Identification								
JEDEC-ID	JEDEC-ID Read	9FH	X		0	0	3 to ∞	104 MHz
Quad J-ID	Quad I/O J-ID Read	AFH		X	0	1	3 to ∞	
SFDP	Serial Flash Discoverable Parameters	5AH	X		3	1	1 to ∞	

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26WF064C (CONTINUED) (2 OF 2)

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq
			SPI	SQI				
Write								
WREN	Write Enable	06H	X	X	0	0	0	104 MHz
WRDI	Write Disable	04H	X	X	0	0	0	
SE[12]	Erase 4 KBytes of Memory Array	20H	X	X	3	0	0	
BE[13]	Erase 64, 32 or 8 KBytes of Memory Array	D8H	X	X	3	0	0	
CE	Erase Full Array	C7H	X	X	0	0	0	
PP	Page Program	02H	X	X	3	0	1 to 256	
SPI Quad PP[7]	SPI Quad Page Program	32H	X		3	0	1 to 256	104 MHz
WRSU	Suspends Program/ Erase	B0H	X	X	0	0	0	
WRRE	Resumes Program/ Erase	30H	X	X	0	0	0	
Protection								
RBPR	Read Block-Protection Register	72H	X		0	0	1 to 18	104 MHz
				X	0	1	1 to 18	
WBPR	Write Block-Protection Register	42H	X	X	0	0	1 to 18	
LBPR	Lock Down Block-Protection Register	8DH	X	X	0	0	0	
nVWLDR	non-Volatile Write Lock-Down Register	E8H	X	X	0	0	1 to 18	
ULBPR	Global Block Protection Unlock	98H	X	X	0	0	0	
RSID	Read Security ID	88H	X		2	1	1 to 2048	
				X	2	3	1 to 2048	
PSID	Program User Security ID area	A5H	X	X	2	0	1 to 256	
LSID	Lockout Security ID Programming	85H	X	X	0	0	0	
Power Saving								
DPD	Deep Power-down Mode	B9H	X	X	0	0	0	104 MHz
RDPD	Release from Deep Power-down and Read ID	ABH	X	X	3	0	1 to ∞	

1. Command cycle is two clock periods in SQI mode and eight clock periods in SPI mode.
2. Address bits above the most significant bit of each density can be V_{IL} or V_{IH}.
3. Address, Dummy/Mode bits, and Data cycles are two clock periods in SQI and eight clock periods in SPI mode.
4. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
5. Device accepts eight-clock command in SPI mode, or two-clock command in SQI mode.
6. Data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
7. Address, Dummy/Mode bits, and data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
8. Data cycles are four clock periods.
9. Address, Dummy/Mode bits, and Data cycles are four clock periods.
10. For DTR commands, the number of clocks is listed for address and dummy.
11. IOC bit must be set to '1' before issuing the command.
12. Sector Addresses: Use A_{MS} - A_{12}, remaining address are don't care, but must be set to V_{IL} or V_{IH}.
13. Blocks are 64 KByte, 32 KByte, or 8KByte, depending on location. Block Erase Address: A_{MS} - A_{16} for 64 KByte; A_{MS} - A_{15} for 32 KByte; A_{MS} - A_{13} for 8 KByte. Remaining addresses are don't care, but must be set to V_{IL} or V_{IH}.

5.1 No Operation (NOP)

The No Operation command only cancels a Reset-Enable command. NOP has no impact on any other command.

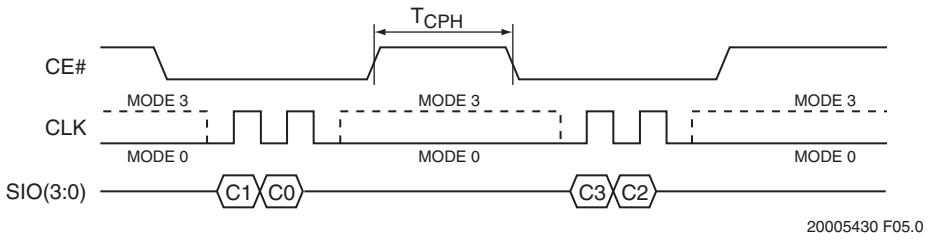
5.2 Reset-Enable (RSTEN) and Reset (RST)

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) followed by Reset (RST).

To reset the SST26WF064C, the host drives CE# low, sends the Reset-Enable command (66H), and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99H), and drives CE# high, see Figure 5-1.

A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations. See Table 8-3 on page 54 for Rest timing parameters.

FIGURE 5-1: RESET SEQUENCE



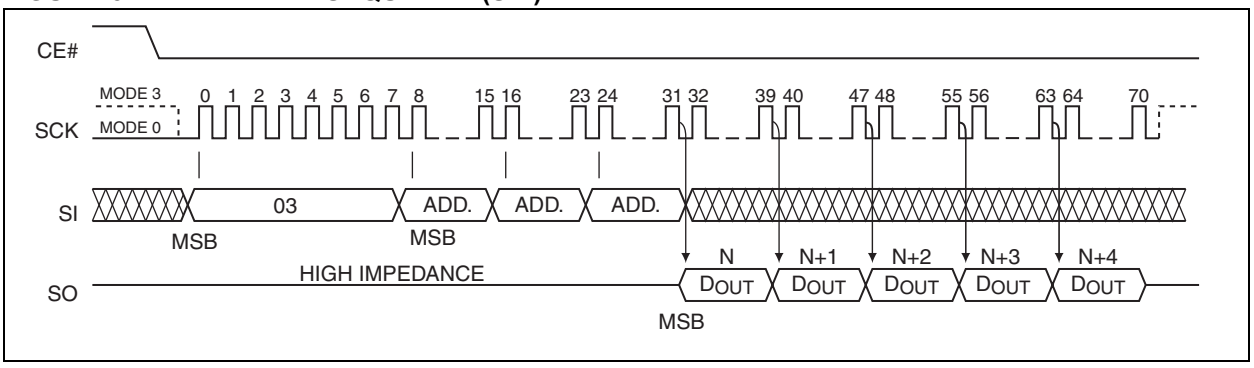
Note: C[1:0] = 66H; C[3:2] = 99H

5.3 Read (40 MHz)

The Read instruction, 03H, is supported in SPI bus protocol only with clock frequencies up to 40 MHz. This command is not supported in SQI bus protocol. The device outputs the data starting from the specified address location, then continuously streams the data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically return to the beginning (wrap-around) of the address space.

Initiate the Read instruction by executing an 8-bit command, 03H, followed by address bits A[23:0]. CE# must remain active low for the duration of the Read cycle. See Figure 5-2 for Read Sequence.

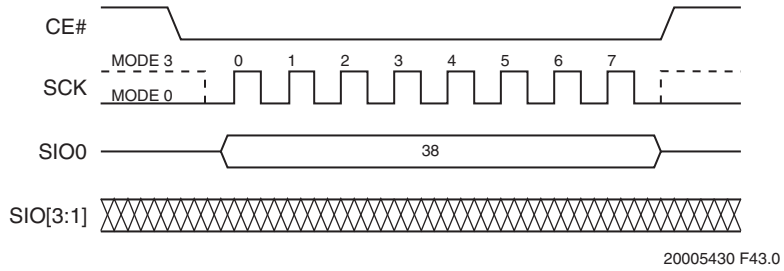
FIGURE 5-2: READ SEQUENCE (SPI)



5.4 Enable Quad I/O (EQIO)

The Enable Quad I/O (EQIO) instruction, 38H, enables the flash device for SQI bus operation. Upon completion of the instruction, all instructions thereafter are expected to be 4-bit multiplexed input/output (SQI mode) until a power cycle or a “Reset Quad I/O instruction” is executed. See Figure 5-3.

FIGURE 5-3: ENABLE QUAD I/O SEQUENCE



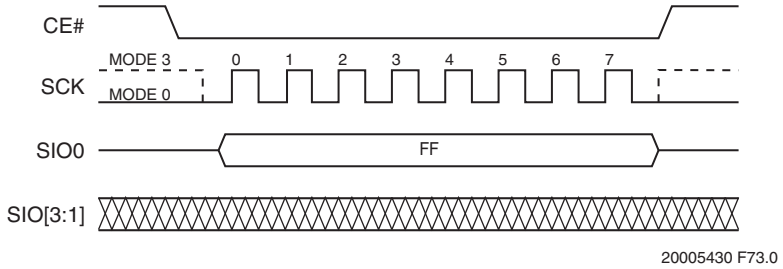
Note: SIO[3:1] must be driven V_{IH}

5.5 Reset Quad I/O (RSTQIO)

The Reset Quad I/O instruction, FFH, resets the device to 1-bit SPI protocol operation or exits the Set Mode configuration during a read sequence. This command allows the flash device to return to the default I/O state (SPI) without a power cycle, and executes in either 1-bit or 4-bit mode. If the device is in the Set Mode configuration, while in SQI High-Speed Read mode, the RSTQIO command will only return the device to a state where it can accept new SQI command instruction. An additional RSTQIO is required to reset the device to SPI mode.

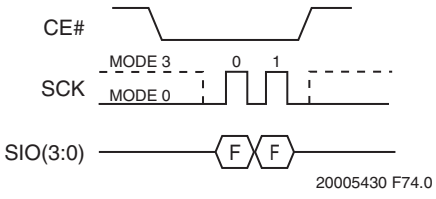
To execute a Reset Quad I/O operation, the host drives CE# low, sends the Reset Quad I/O command cycle (FFH) then, drives CE# high. Execute the instruction in either SPI (8 clocks) or SQI (2 clocks) command cycles. For SPI, SIO[3:1] are don't care for this command, but should be driven to V_{IH} or V_{IL}. See Figures 5-4 and 5-5.

FIGURE 5-4: RESET QUAD I/O SEQUENCE (SPI)



Note: SIO[3:1]

FIGURE 5-5: RESET QUAD I/O SEQUENCE (SQI)

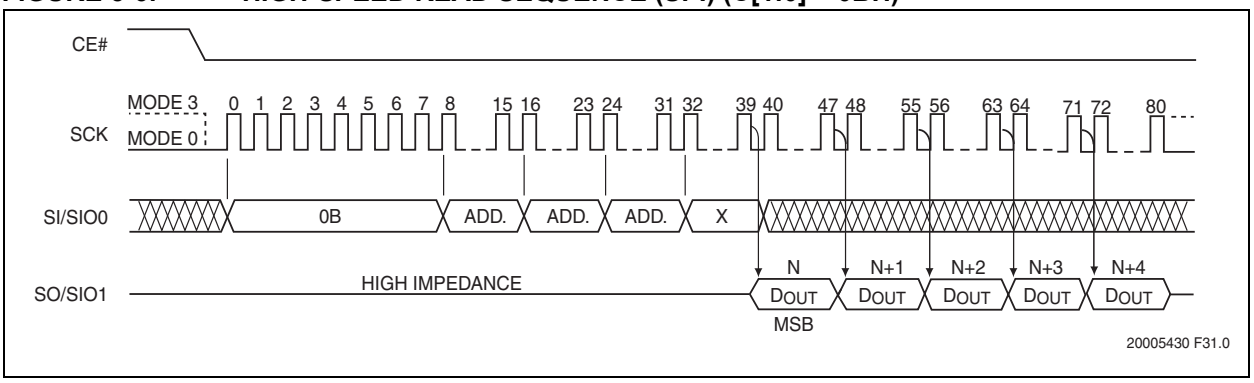


5.6 High-Speed Read (104 MHz)

The High-Speed Read instruction, 0BH, is supported in both SPI bus protocol and SQI protocol. On power-up, the device is set to use SPI.

Initiate High-Speed Read by executing an 8-bit command, 0BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active low for the duration of the High-Speed Read cycle. See Figure 5-6 for the High-Speed Read sequence for SPI bus protocol.

FIGURE 5-6: HIGH-SPEED READ SEQUENCE (SPI) (C[1:0] = 0BH)



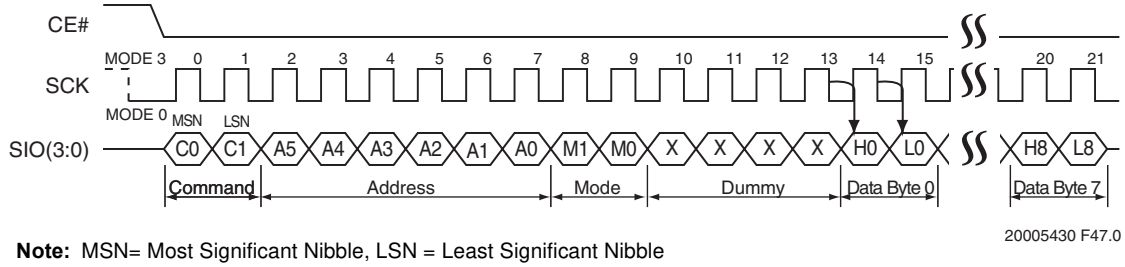
In SQI protocol, the host drives CE# low then sends the Read command cycle command, 0BH, followed by three address cycles, a Set Mode Configuration cycle, and two dummy cycles. Each cycle is two nibbles (clocks) long, most significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to address location 000000H. During this operation, blocks that are Read-locked will output data 00H.

The Set Mode Configuration bits M[7:0] indicates if the next instruction cycle is another SQI High-Speed Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, 0BH, and does not require the op-code to be entered again. The host may initiate the next Read cycle by driving CE# low, then sending the four-bits input for address A[23:0], followed by the Set Mode configuration bits M[7:0], and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. While in the Set Mode configuration, the RSTQIO command will only return the device to a state where it can accept new SQI command instruction. An additional RSTQIO is required to reset the device to SPI mode. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

FIGURE 5-7: HIGH-SPEED READ SEQUENCE (SQI)



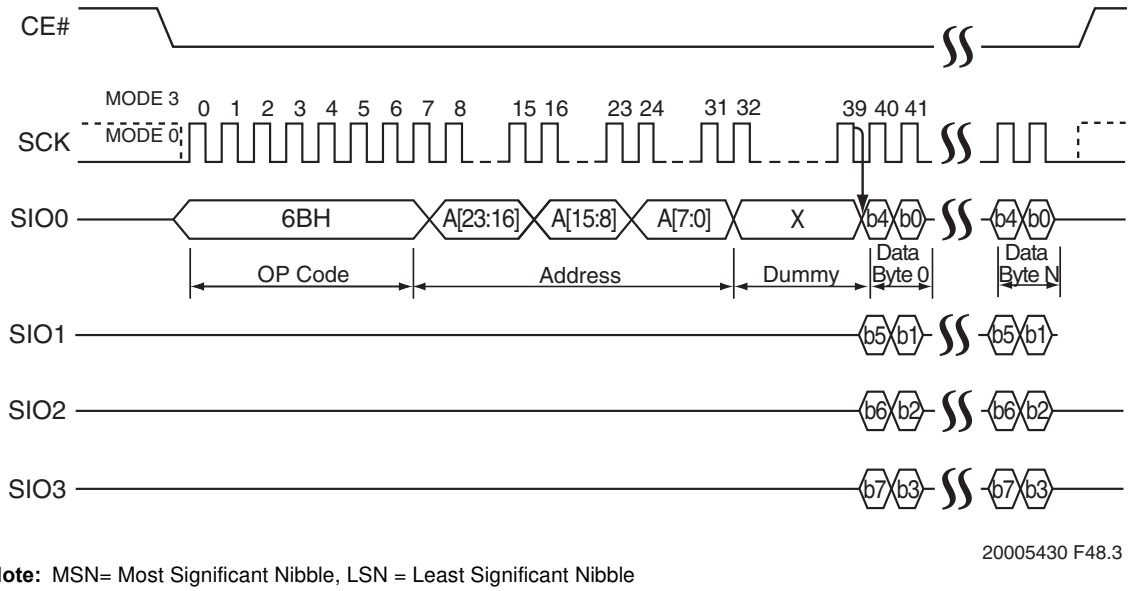
Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble
Hx = High Data Nibble, Lx = Low Data Nibble C[1:0] = 0BH

5.7 SPI Quad-Output Read

The SPI Quad-Output Read instruction supports up to 104 MHz frequency. The SST26WF064C requires the IOC bit in the configuration register to be set to '1' prior to executing the command. Initiate SPI Quad-Output Read by executing an 8-bit command, 6BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active low for the duration of the SPI Quad Output Read. See Figure 5-8 for the SPI Quad Output Read sequence.

Following the dummy byte, the device outputs data from SIO[3:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

FIGURE 5-8: SPI QUAD OUTPUT READ



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

5.8 SPI Quad I/O Read

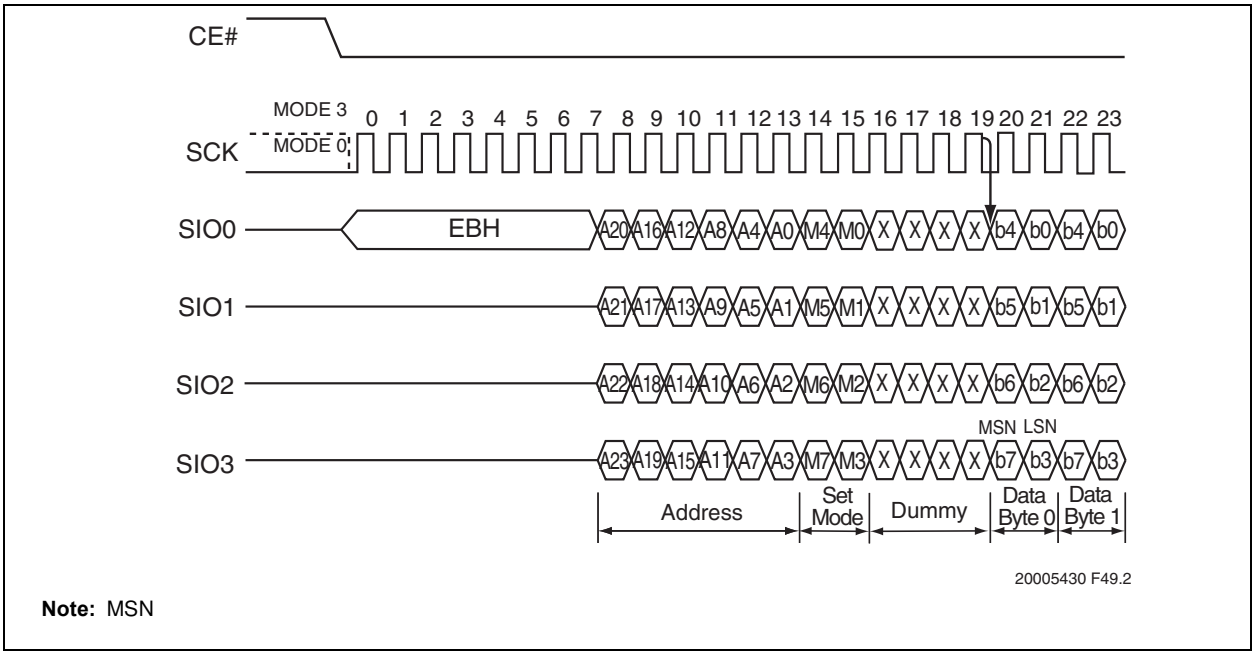
The SPI Quad I/O Read (SQIOR) instruction supports up to 104 MHz frequency. The SST26WF064C requires the IOC bit in the configuration register to be set to '1' prior to executing the command. Initiate SQIOR by executing an 8-bit command, EBH. The device then switches to 4-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0], and two dummy bytes.CE# must remain active low for the duration of the SPI Quad I/O Read. See Figure 5-9 for the SPI Quad I/O Read sequence.

Following the dummy bytes, the device outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

The Set Mode Configuration bits M[7:0] indicates if the next instruction cycle is another SPI Quad I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, EBH, and does not require the op-code to be entered again. The host may set the next SQIOR cycle by driving CE# low, then sending the four-bit wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0], and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

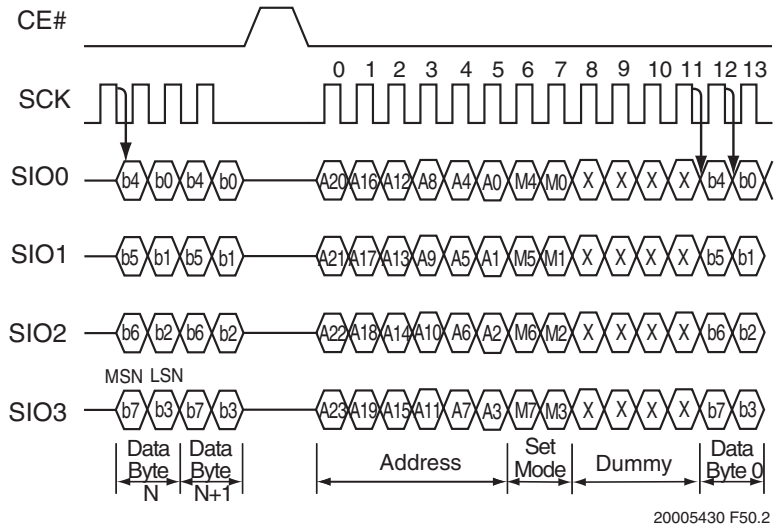
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

FIGURE 5-9: SPI QUAD I/O READ SEQUENCE



Note: MSN

FIGURE 5-10: BACK-TO-BACK SPI QUAD I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSN= Most Sig-

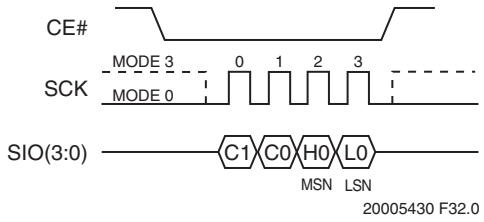
5.9 Set Burst

The Set Burst command specifies the number of bytes to be output during a Read Burst command before the device wraps around. It supports both SPI and SQI protocols. To set the burst length the host drives CE# low, sends the Set Burst command cycle (C0H) and one data cycle, then drives CE# high. After power-up or reset, the burst length is set to eight Bytes (00H). See Table 5-2 for burst length data and Figures 5-11 and 5-12 for the sequences.

TABLE 5-2: BURST LENGTH DATA

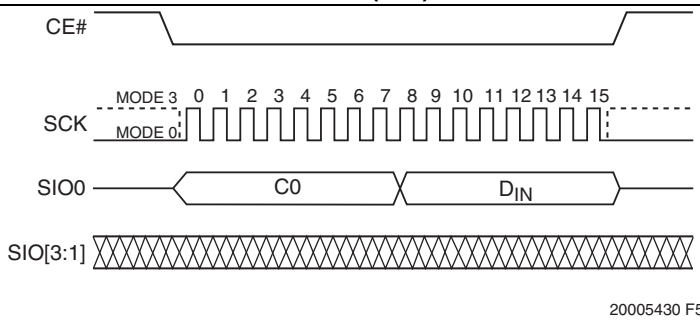
Burst Length	High Nibble (H0)	Low Nibble (L0)
8 Bytes	0h	0h
16 Bytes	0h	1h
32 Bytes	0h	2h
64 Bytes	0h	3h

FIGURE 5-11: SET BURST LENGTH SEQUENCE (SQI)



Note: MSN = Most Significant Nibble,
LSN = Least Significant Nibble, C[1:0] = C0H

FIGURE 5-12: SET BURST LENGTH SEQUENCE (SPI)



Note: SIO[3:1] must be

5.10 SQI Read Burst with Wrap (RBSQI)

SQI Read Burst with wrap is similar to High Speed Read in SQI mode, except data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SQI Read Burst operation, drive CE# low then send the Read Burst command cycle (0CH), followed by three address cycles, and then three dummy cycles. Each cycle is two nibbles (clocks) long, most significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSQI, the internal address pointer automatically increments until the last byte of the burst is reached, then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length, see Table 5-3. For example, if the burst length is eight Bytes, and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are Read-locked will output data 00H.

5.11 SPI Read Burst with Wrap (RBSPI)

SPI Read Burst with Wrap (RBSPI) is similar to SPI Quad I/O Read except the data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SPI Read Burst with Wrap operation, drive CE# low, then send the Read Burst command cycle (ECH), followed by three address cycles, and then three dummy cycles.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSPI, the internal address pointer automatically increments until the last byte of the burst is reached, then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length, see Table 5-3. For example, if the burst length is eight Bytes, and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are Read-locked will output data 00H.

TABLE 5-3: BURST ADDRESS RANGES

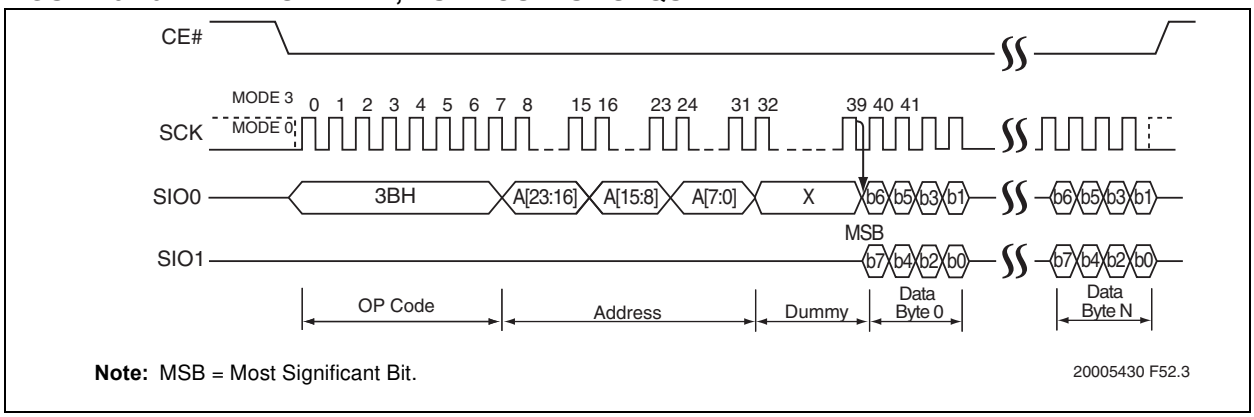
Burst Length	Burst Address Ranges
8 Bytes	00-07H, 08-0FH, 10-17H, 18-1FH...
16 Bytes	00-0FH, 10-1FH, 20-2FH, 30-3FH...
32 Bytes	00-1FH, 20-3FH, 40-5FH, 60-7FH...
64 Bytes	00-3FH, 40-7FH, 80-BFH, C0-FFH

5.12 SPI Dual-Output Read

The SPI Dual-Output Read instruction supports up to 104 MHz frequency. Initiate SPI Dual-Output Read by executing an 8-bit command, 3BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active low for the duration of the SPI Dual-Output Read operation. See Figure 5-13 for the SPI Quad Output Read sequence.

Following the dummy byte, the SST26WF064C outputs data from SIO[1:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

FIGURE 5-13: FAST READ, DUAL-OUTPUT SEQUENCE



Note: MSB = Most Significant Bit.

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5.13 SPI Dual I/O Read

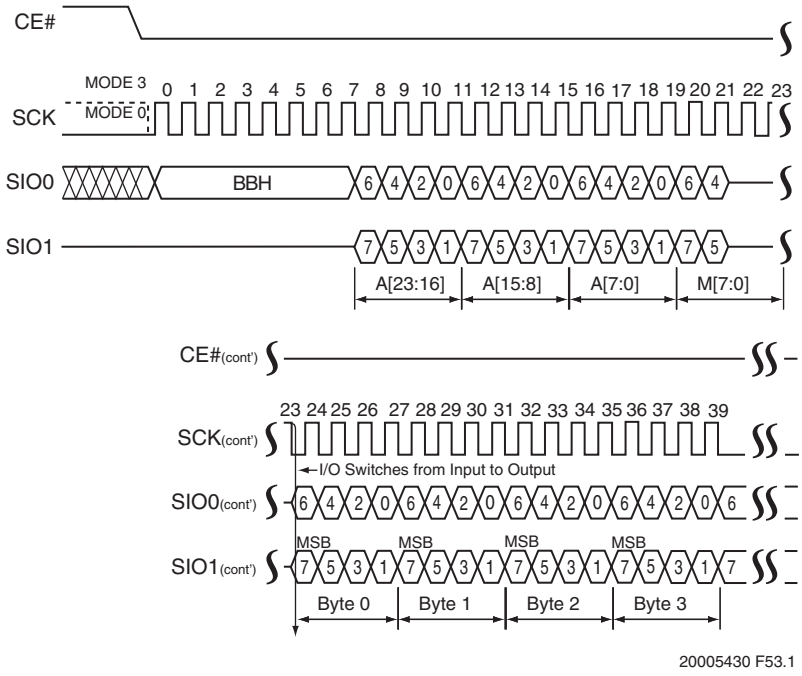
The SPI Dual I/O Read (SDIOR) instruction supports up to 80 MHz frequency. Initiate SDIOR by executing an 8-bit command, BBH. The device then switches to 2-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0]. CE# must remain active low for the duration of the SPI Dual I/O Read. See Figure 5-14 for the SPI Dual I/O Read sequence.

Following the Set Mode configuration bits M[7:0], the SST26WF064C outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Dual I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another SDIOR command, BBH, and does not require the op-code to be entered again. The host may set the next SDIOR cycle by driving CE# low, then sending the two-bit wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0]. After the Set Mode configuration bits, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

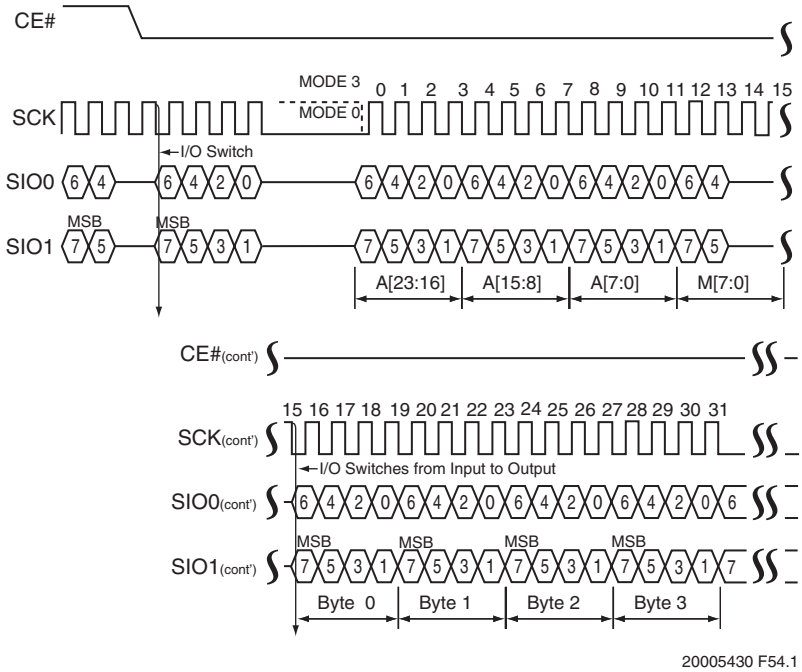
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-15 for the SPI Dual I/O Read sequence when M[7:0] = AXH.

FIGURE 5-14: SPI DUAL I/O READ SEQUENCE



Note: MSN=

FIGURE 5-15: BACK-TO-BACK SPI DUAL I/O READ SEQUENCES WHEN M[7:0] = AXH

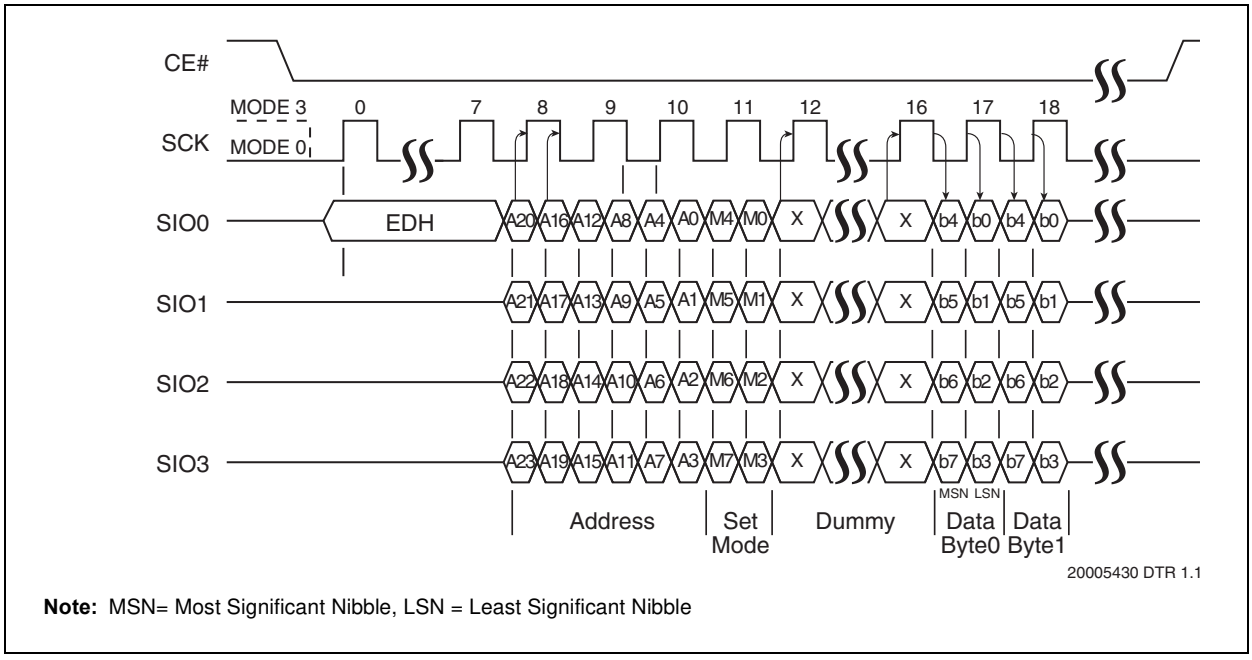


Note: MSN= Most

5.14 Dual-Transfer Rate (DTR)

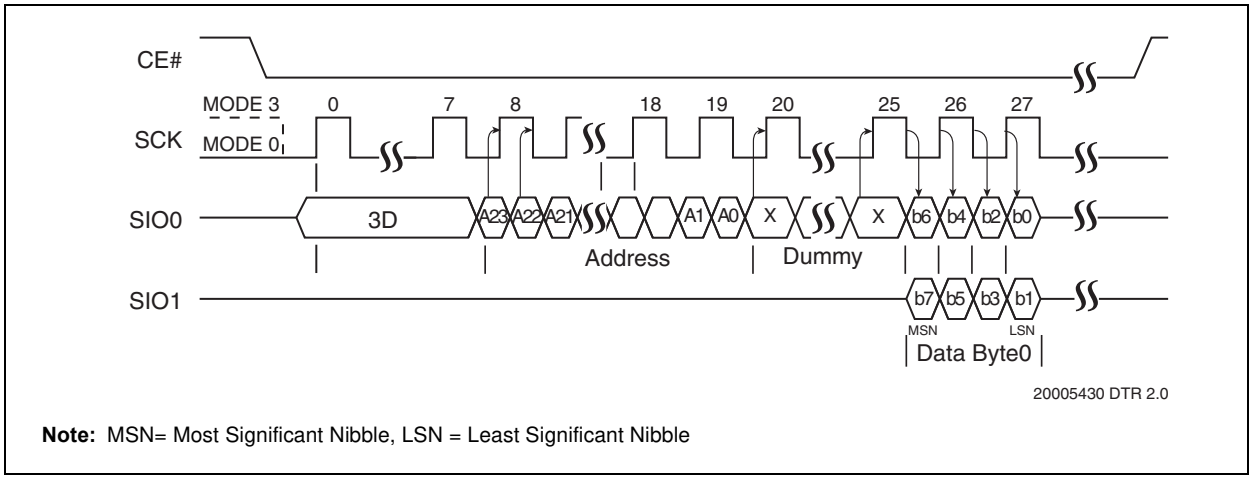
Initiate all Dual-Transfer Rate read modes by executing an 8-bit DTR Read command. The device then switches to dual-data rate for the address, set mode configuration bits M[7:0], and dummy clock cycles. Following the dummy bytes, the device outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

The Set Mode Configuration bits M[7:0] indicate if the next instruction cycle is another DTR Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another DTR Read command, and does not require the op-code to be entered again. Set the next DTR cycle by driving CE# low, then sending the address A[23:0], followed by the Set Mode configuration bits M[7:0], and dummy clock cycles. After the dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

FIGURE 5-16: SPI QUAD I/O READ – DTR



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

FIGURE 5-17: SPI DUAL OUTPUT READ – DTR