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1.35V/1.5V REGISTERING CLOCK DRIVER WITH PARITY TEST AND QUAD CHIP SELECT

SSTE32882HLB

Description

This 28-bit 1:2, or 26-bit 1:2 and 4-bit 1:1, registering clock driver with parity is designed for 1.35V and 1.5V V_{DD} operation.

All inputs are 1.35V and 1.5V CMOS compatible, except the reset ($\overline{RESET}$) and MIRROR inputs which are LVCMOS. All outputs are 1.35V and 1.5V CMOS edge-controlled drivers optimized to drive single terminated 25Ω to 50Ω traces in DDR3 RDIMM applications, except the open-drain error ($\overline{ERROUT}$) output. The clock outputs (Yn and $\overline{Yn}$) and control net outputs QnCKEn, $\overline{QnCSn}$ and QnODTn are designed with a different strength and skew to compensate for different loading and equalize signal travel speed.

The SSTE32882HLB has two basic modes of operation associated with the Quad Chip Select Enable ($\overline{QCSEN}$) input. When the $\overline{QCSEN}$ input pin is open (or pulled high), the component has two chip select inputs, $\overline{DCS0}$ and $\overline{DCS1}$, and two copies of each chip select output, $\overline{QACS0}$, $\overline{QACS1}$, $\overline{QBCS0}$ and $\overline{QBCS1}$. This is the "QuadCS disabled" mode. When the $\overline{QCSEN}$ input pin is pulled low, the component has four chip select inputs $\overline{DCS[3:0]}$, and four chip select outputs, $\overline{QCS[3:0]}$. This is the "QuadCS enabled" mode. Through the remainder of this specification, $\overline{DCS[n:0]}$ will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{QxCS[n:0]}$ will indicate all of the chip select outputs.

The SSTE32882HLB includes a high-performance, low-jitter, low-skew buffer that distributes a differential clock input (CK and $\overline{CK}$) to four differential pairs of clock outputs (Yn and $\overline{Yn}$), and to one differential pair of feedback clock outputs (FBOUT and $\overline{FBOUT}$). The clock outputs are controlled by the input clocks (CK and $\overline{CK}$), the feedback clocks (FBIN and $\overline{FBIN}$), and the analog power inputs (AV_{DD} and AV_{SS}). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

The SSTE32882HLB operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low. The data is either driven to the corresponding device outputs if exactly one of the $\overline{DCS[n:0]}$ input signals is driven low.

Based on the control register settings, the device can change its output characterisitics to match different DIMM net topologies. The timing can be changed to compensate for different flight time of signals within the target application. By disabling unused outputs the power consumption is reduced.

The SSTE32882HLB accepts a parity bit from the memory controller on the parity (PAR_IN) input, compares it with the data received on the DIMM-independent data inputs (DAn, DBAn, $\overline{DRAS}$, $\overline{DCAS}$, and $\overline{DWE}$), and indicates whether a parity error has occurred on the open-drain $\overline{ERROUT}$ pin (active low). The convention is even parity; i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

The DIMM-dependent signals (DCKEn, DODTn, and $\overline{DCSn}$) are not included in the parity check computation.

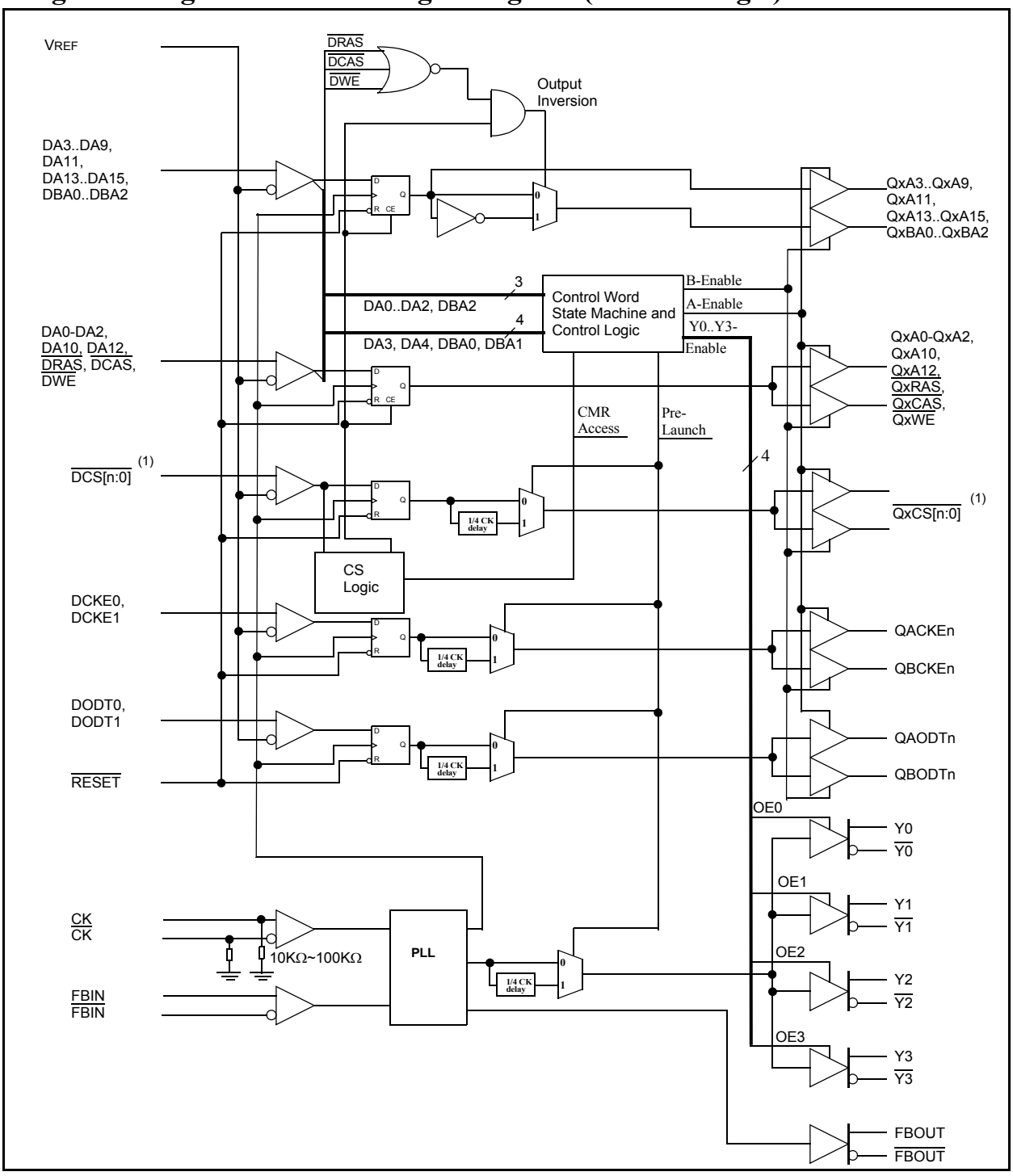
To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power-up.

The SSTE32882HLB is available in a 176-ball BGA with 0.65mm ball pitch in a 11 x 20 grid. It is also available in a 176-ball Thin-Profile Fine-Pitch BGA with 0.65mm ball pitch in an 8x22 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a-way that two devices can be placed back-to-back for four Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

Features

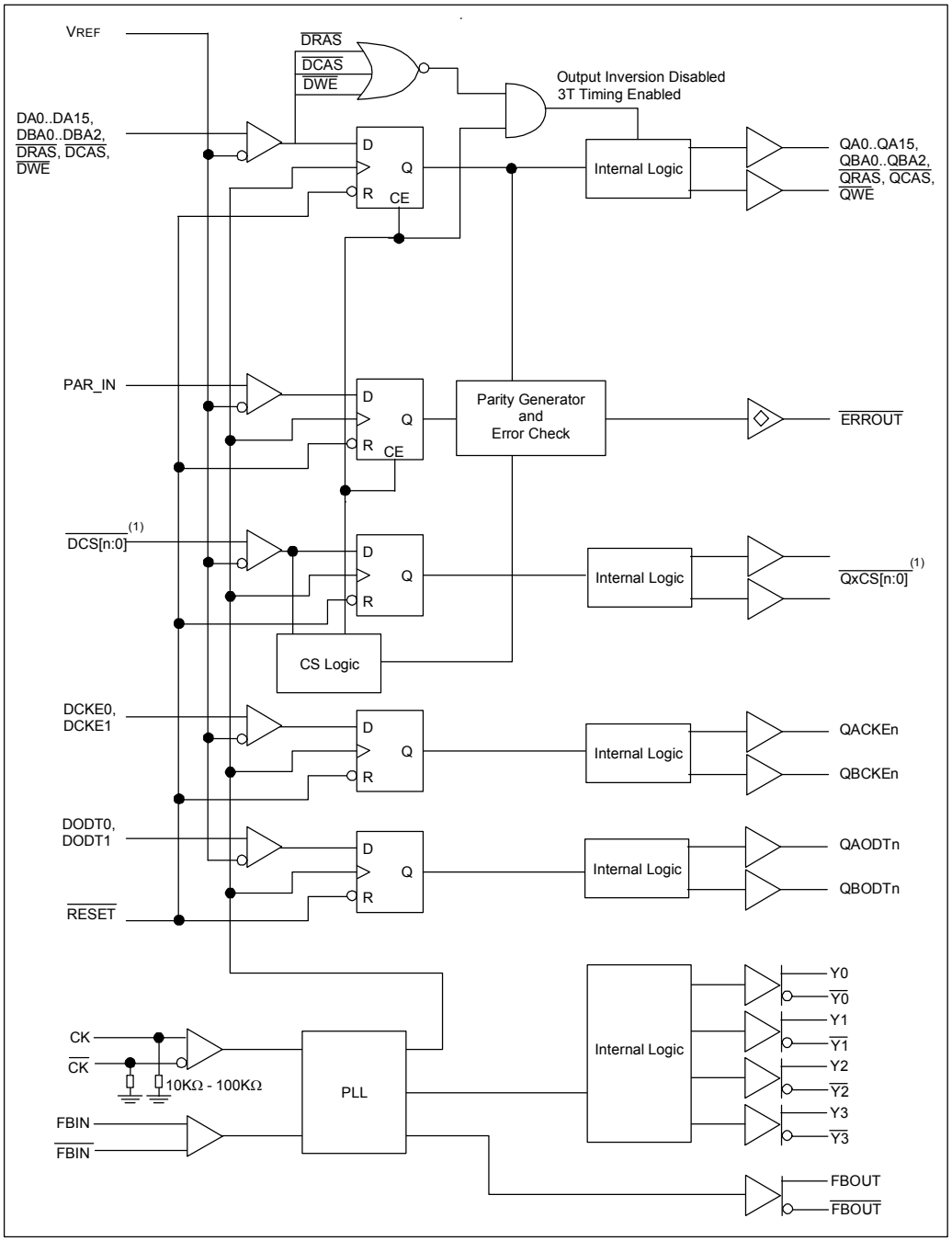
- Pinout optimizes DDR3 RDIMM PCB layout
- 1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs support stacked DDR3 RDIMMs
- Phase Lock Loop clock driver for buffering one differential clock pair (CK and $\overline{CK}$) and distributing to four differential outputs
- Supports LVCMOS switching levels on the $\overline{RESET}$ and MIRROR inputs
- Checks priority on DIMM-independent data inputs
- Supports dynamic 1T/3T timing transaction and output inversion feature for improved timing performance during normal operations and MRS command pass-through
- Supports CKE Power Down operation modes
- Supports Quad Chip Select operation features
- $\overline{RESET}$ input disables differential input recievers, resets all registers, and disables all output drivers except $\overline{ERROUT}$ and QnCKEn
- Provides access to internal control words for configuring the device features and adapting in different RDIMM and system applications
- Latch-up performance exceeds 100mA
- ESD > 2000V per MIL-STD883, Method 3015; ESD > 200V using machine model (c = 200pF, R = 0)
- Available in 176 Ball Grid Array package

Block Diagram - Register and PLL Logic Diagram (Positive Logic)



1 $\overline{\text{DCS}}$[n:0] indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{\text{QxCS}}$[n:0] indicates all of the chip select outputs.

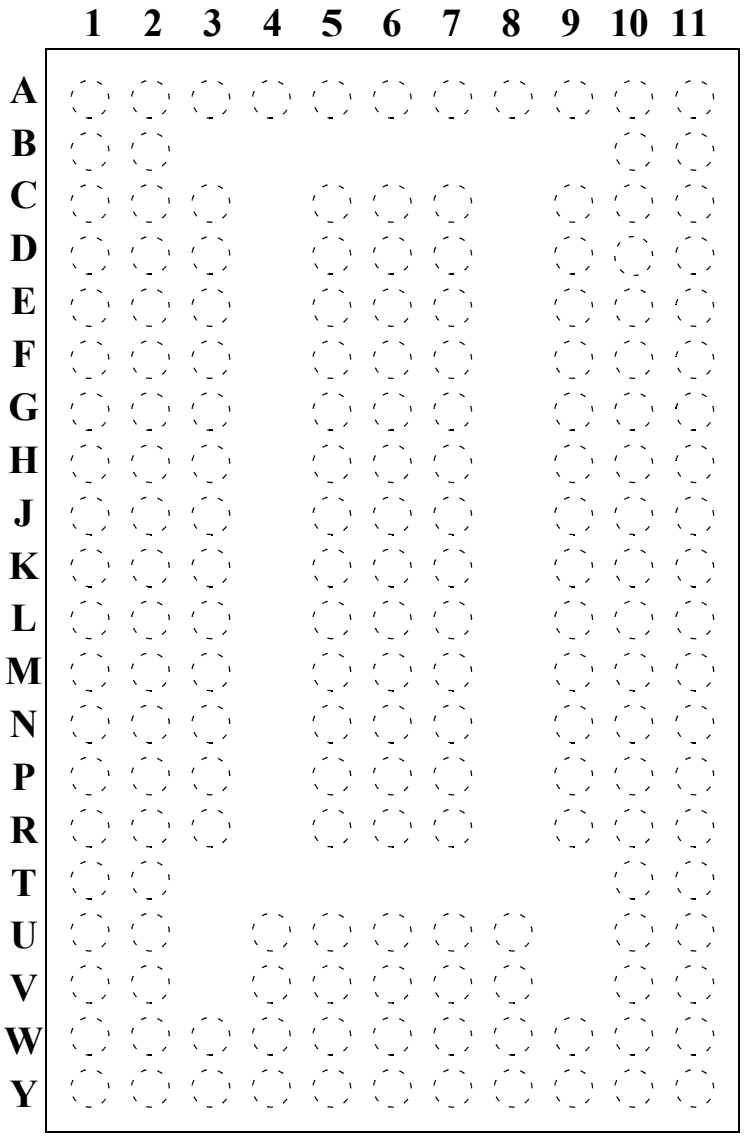
Block Diagram - Parity Logic Diagram (Positive Logic)



1 $\overline{\text{DCS[n:0]}}$ indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{\text{QxCS[n:0]}}$ indicates all of the chip select outputs.

Pinout Configuration

Package options include a 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 11 x 20 grid, 8.0mm x 13.5mm. It uses the mechanical outline MO-246 variation F. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no-ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.



176-ball Thin Profile Fine Pitch BGA (TFBGA) 11x20 Grid

Top View

Pin Descriptions

The device has symmetric pinout with the inputs on the south side and the outputs on the east and west sides. This allows back-to-back mounting on both sides of the PCB if more than one device is needed.

Ball Assignment: MIRROR = LOW, $\overline{\text{QCSEN}}$ = HIGH or float

This table specifies the pinout for SSTE32882HLB in the front configuration (QuadCS mode disabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Also, balls Y2 and R6 are "do not use" balls reserved for $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$ in the QuadCS mode, and must not be connected on the system. The device is designed to tolerate floating on these pins. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DODT1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DODT0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Ball Assignment: MIRROR = HIGH, $\overline{\text{QCSEN}}$ = HIGH or float

This table specifies the pinout for SSTE32882HLB in the back configuration (QuadCS mode disabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Also, balls Y10 and R6 are "do not use" balls reserved for $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$ in the QuadCS mode, and must not be connected on the system. The device is designed to tolerate floating on these pins. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	RSVD	DA7

Ball Assignment: MIRROR = LOW, $\overline{\text{QCSEN}}$ = LOW

This table specifies the pinout for SSTE32882HLB in the front configuration (QuadCS mode enabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QCS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	$\overline{\text{DCS3}}$	DA2		DA1	DA10	DODT1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DODT0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	$\overline{\text{DCS2}}$	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Ball Assignment: MIRROR = HIGH, $\overline{\text{QCSEN}}$ = LOW

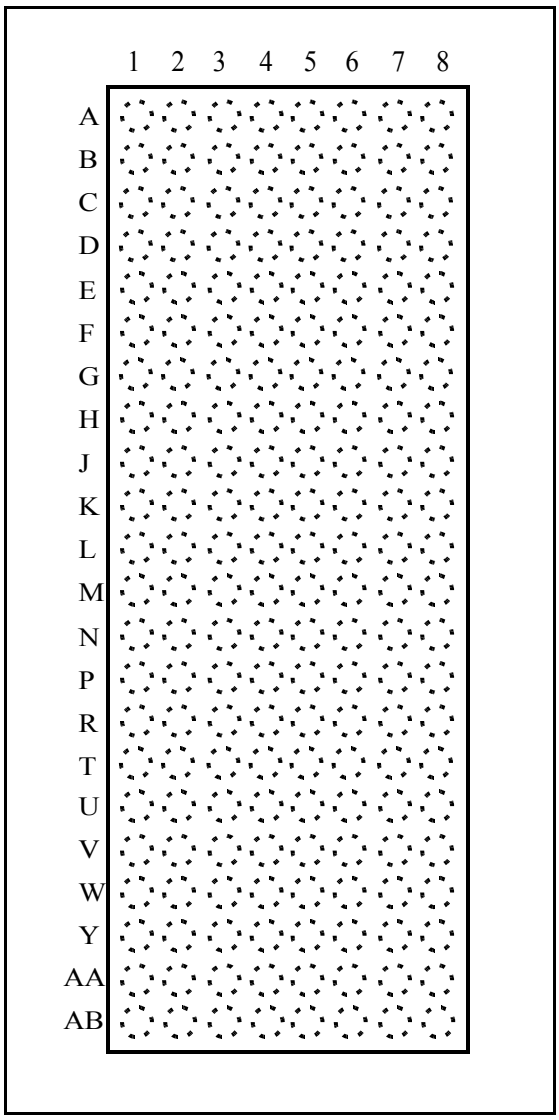
This table specifies the pinout for SSTE32882HLB in the back configuration (QuadCS mode enabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QCS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	$\overline{\text{DCS3}}$	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	$\overline{\text{DCS2}}$	DA7

Pinout configuration narrow package[1]

As an option, the device is available as a176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 8 x 22 grid, 6.0mm x 15mm. It is using the mechanical outline MO-246 variation B. Equivalent to the 11 x 20 grid configuration the device pinout supports outputs on the outer two left and right columns. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias.



176-ball Thin Profile Fine Pitch BGA (TFBGA) 8x22 Grid

Top View

1. This package may only be used in new DIMM designs. It is not intended for use in the existing DIMM's.

Ball Assignment; MIRROR=LOW, $\overline{\text{QCSEN}}$=HIGH (or Float)

The table below specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	$\overline{\text{RESET}}$	$\overline{\text{ERROUT}}$	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD	VDD	VDD	VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD	VDD	VDD	VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD	VDD	VDD	VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	VSS	VSS	VSS	VSS	QBODT1	$\overline{\text{QBRAS}}$
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	$\overline{\text{DCS0}}$	DCKE0	VSS	VSS	VSS	VSS	DODT0	$\overline{\text{DCS1}}$
U	DA12	DA3	$\overline{\text{Y1}}$	PVSS	PVDD	$\overline{\text{Y0}}$	DA4	$\overline{\text{DCAS}}$
V	DA5	DA9	Y1	PVSS	PVDD	Y0	$\overline{\text{DWE}}$	DA2
W	DA8	DA15	$\overline{\text{Y3}}$	PVSS	PVDD	$\overline{\text{Y2}}$	DA1	DBA0
Y	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	RSVD	$\overline{\text{FBIN}}$	$\overline{\text{CK}}$	RSVD	$\overline{\text{FBOUT}}$	PAR_IN	$\overline{\text{DRAS}}$
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA0

Pins A6, AA2, AA5, AB2 and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Ball Assignment; MIRROR=HIGH, $\overline{\text{QCSEN}}$=HIGH (or Float)

The table below specifies the pinout for SSTE32882 in back configuration with QuadCS mode disabled.

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	$\overline{\text{RESET}}$	$\overline{\text{ERROUT}}$	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD	VDD	VDD	VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD	VDD	VDD	VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD	VDD	VDD	VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	VSS	VSS	VSS	VSS	QBODT1	$\overline{\text{QBRAS}}$
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	$\overline{\text{DCS1}}$	DODT0	VSS	VSS	VSS	VSS	DCKE0	$\overline{\text{DCS0}}$
U	$\overline{\text{DCAS}}$	DA4	$\overline{\text{Y1}}$	PVSS	PVDD	$\overline{\text{Y0}}$	DA3	DA12
V	DA2	$\overline{\text{DWE}}$	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	$\overline{\text{Y3}}$	PVSS	PVDD	$\overline{\text{Y2}}$	DA15	DA8
Y	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	$\overline{\text{DRAS}}$	PAR_IN	$\overline{\text{FBIN}}$	$\overline{\text{CK}}$	RSVD	$\overline{\text{FBOUT}}$	RSVD	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA6

Pins A6, AA5, AA7, AB2 and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Ball Assignment; MIRROR=LOW, $\overline{\text{QCSEN}}$=LOW

The table below specifies the pinout for SSTE32882 in front configuration with QuadCS mode enabled.

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	$\overline{\text{RESET}}$	$\overline{\text{ERROUT}}$	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD	VDD	VDD	VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QCS0}}$	VDD	VDD	VDD	VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD	VDD	VDD	VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	VSS	VSS	VSS	VSS	QBODT1	$\overline{\text{QBRAS}}$
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	$\overline{\text{DCS0}}$	DCKE0	VSS	VSS	VSS	VSS	DODT0	$\overline{\text{DCS1}}$
U	DA12	DA3	$\overline{\text{Y1}}$	PVSS	PVDD	$\overline{\text{Y0}}$	DA4	$\overline{\text{DCAS}}$
V	DA5	DA9	Y1	PVSS	PVDD	Y0	$\overline{\text{DWE}}$	DA2
W	DA8	DA15	$\overline{\text{Y3}}$	PVSS	PVDD	$\overline{\text{Y2}}$	DA1	DBA0
Y	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	$\overline{\text{DCS2}}$	$\overline{\text{FBIN}}$	$\overline{\text{CK}}$	RSVD	$\overline{\text{FBOUT}}$	PAR_IN	$\overline{\text{DRAS}}$
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	$\overline{\text{DCS3}}$	DA0

Pins A6, AA5 and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Ball Assignment; MIRROR=HIGH, $\overline{\text{QCSEN}}$=LOW)

The table below specifies the pinout for SSTE32882 in back configuration with QuadCS mode enabled.

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	1	2	3	4	5	6	7	8
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	$\overline{\text{RESET}}$	$\overline{\text{ERROUT}}$	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD	VDD	VDD	VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QCS0}}$	VDD	VDD	VDD	VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD	VDD	VDD	VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	VSS	VSS	VSS	VSS	QBODT1	$\overline{\text{QBRAS}}$
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	$\overline{\text{DCS1}}$	DODT0	VSS	VSS	VSS	VSS	DCKE0	$\overline{\text{DCS0}}$
U	$\overline{\text{DCAS}}$	DA4	$\overline{\text{Y1}}$	PVSS	PVDD	$\overline{\text{Y0}}$	DA3	DA12
V	DA2	$\overline{\text{DWE}}$	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	$\overline{\text{Y3}}$	PVSS	PVDD	$\overline{\text{Y2}}$	DA15	DA8
Y	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	$\overline{\text{DRAS}}$	PAR_IN	$\overline{\text{FBIN}}$	$\overline{\text{CK}}$	RSVD	$\overline{\text{FBOUT}}$	$\overline{\text{DCS2}}$	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	$\overline{\text{DCS3}}$	DA6

Pins A6, AA5 and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Terminal Functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKEn, DODTn	1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register function pins not associated with Chip Select.
Chip Select gated inputs	DAn, DBAn, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$	1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register inputs, re-driven only when either chip select is LOW. If both chip selects are low the register maintains the state of the previous input clock cycle at its outputs
Chip Select inputs	$\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$	1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be low when a valid address/command is present which should be re-driven.
	$\overline{\text{DCS2}}$, $\overline{\text{DCS3}}$	1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register Chip Select signals when QuadCS mode is enabled. $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$ inputs are disabled when QuadCS mode is disabled.
Re-driven outputs	QxAn, QxBAn, $\overline{\text{QxCSn}}$, QxCKEn, QxODTn, $\overline{\text{QxRAS}}$, $\overline{\text{QxCAS}}$, $\overline{\text{QxWE}}$	1.35V/1.5V CMOS Outputs[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. x is A or B; outputs are grouped as A or B and may be enabled or disabled via RC0.
Parity input	PAR_IN	1.35V/1.5V CMOS Inputs[1]	Input parity is received on pin PAR_IN and should maintain parity across the Chip Select Gated inputs (see above), at the rising edge of the input clock, one input clock cycle after corresponding data and one or both chip selects are LOW.
Parity error output	$\overline{\text{ERROUT}}$	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{\text{ERROUT}}$ will be active for two clock cycles, and delayed by 3 clock cycles to the corresponding input data
Clock inputs	CK, $\overline{\text{CK}}$	1.35V/1.5V CMOS Inputs[1]	Differential master clock input pair to the PLL; has weak internal pull-down resistors (10KΩ~100KΩ) .
Feedback	FBIN, $\overline{\text{FBIN}}$	1.35V/1.5V CMOS Inputs[1]	Feedback clock input
Clock	FBOUT, $\overline{\text{FBOUT}}$	1.35V/1.5V CMOS Outputs[2]	Feedback clock output
Clock Outputs	Yn, $\overline{\text{Yn}}$	1.35V/1.5V CMOS Outputs[2]	Re-driven Clock
Miscellaneous inputs	$\overline{\text{RESET}}$	CMOS[3]	Active low asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float. Once $\overline{\text{RESET}}$ becomes high the Q outputs get enabled and are driven LOW ($\overline{\text{ERROUT}}$ is driven high) until the first access has been performed. $\overline{\text{RESET}}$ also resets the $\overline{\text{ERROUT}}$ signal.
	MIRROR	CMOS[3]	Selects between two different ballouts for front or back operation. When the MIRROR input is high, the device Input Bus Termination (IBT) is turned off on all inputs, except the $\overline{\text{DCSn}}$ and DODTn inputs.
	$\overline{\text{QSCEN}}$	CMOS[3]	Enables the QuadCS mode. The $\overline{\text{QSCEN}}$ input has a weak internal pullup resistor (10KΩ - 100KΩ).

Signal Group	Signal Name	Type	Description
Power	Vrefca[1]	Reference Voltage	Input reference voltage for the differential data inputs, VDD/2 (0.75V) nominal.
	Vdd	Register Power	Power supply voltage (Register)
	Vss	Register Ground	Ground (Register)
	AVdd	Analog Power	Analog supply voltage (PLL)
	AVss	Analog Ground	Analog ground (PLL)
	PVdd	PLL Power	Clock logic and clock output driver power supply (PLL)
	PVss	PLL Ground	Clock logic and clock output driver ground (PLL)
	RSVD	I/O	Reserved pins, must be left floating (PLL)

1 1.35V/1.5V CMOS inputs use VREFCA as the switching point reference for these recievers.
2 These outputs are optimized for memory applications to drive DRAM inputs to 1.35V/1.5V signaling levels.
3 Voltage levels according standard JESD8-11A, wide range, non terminated logic.

Function Table (Each Flip Flop) with QuadCS Mode Disabled

Inputs								Outputs[1]				
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CK[2]	$\overline{\text{CK}}$[2]	ADDR[3]	CMD[4]	CTRL[5]	Qn[6]	$\overline{\text{QxCS0}}$	$\overline{\text{QxCS1}}$	QxODTn	QxCKEn
H	L	L	↑	↓	Control Word	Control Word	Control Word	Q_0	H	H	Q_0	Q_0
H	X	X	L or H	H or L	X	X	X	Q_0	Q_0	Q_0	Q_0	Q_0
H	L	H	↑	↓	X	X	X	Follows Input	L	H	Follows Input	Follows Input
H	X	X	L	L	X	X	X	float	float	float	float	L
H	H	L	↑	↓	X	X	X	Follows Input	H	L	Follows Input	Follows Input
H	H	H	↑	↓	X or float	X or float	X	Q_0 or float[7]	H	H	Follows Input	Follows Input
L	X or float	X or float	X or float	X or float	X or float	X or float	X or float	float	float	float	float	L

1 Q_0 means the output does not change state.
2 It is illegal to hold both the CK and $\overline{\text{CK}}$ inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when $\overline{\text{RESET}}$ is driven HIGH.
3 ADDR = DA[15:0], DBA[2:0]
4 CMD = $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$.
5 CTRL = DODTn, DCKEn.
6 Qn = QxAn, $\overline{\text{QxRAS}}$, $\overline{\text{QxCAS}}$, $\overline{\text{QxWE}}$, and QxBAn.
7 Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state (Q_0) is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated.

Function Table (Each Flip Flop) with QuadCS Mode Enabled

Inputs					Outputs			
$\overline{\text{RESET}}$	DCS[3:0]	CK[1]	$\overline{\text{CK}}$[1]	A/C/E[2]	Qn	QCS[3:0]	QxODTn	QxCKEn
H	LLHH	↑	↓	Control Word	No change	HHHH	No change	No change
H	HHLL							
H	LLLL							
H	XXXX	L or H	H or L	X	No change	No change	No change	No change
H	LHHH	↑	↓	Dn	Dn	LHHH	DODTn	DCKEn
H	HLHH	↑	↓	Dn	Dn	HLHH	DODTn	DCKEn
H	HHLH	↑	↓	Dn	Dn	HHLH	DODTn	DCKEn
H	HHHL	↑	↓	Dn	Dn	HHHL	DODTn	DCKEn
H	LHLH	↑	↓	Dn	Dn	LHLH	DODTn	DCKEn
H	HLLH	↑	↓	Dn	Dn	HLLH	DODTn	DCKEn
H	LHHL	↑	↓	Dn	Dn	LHHL	DODTn	DCKEn
H	HLHL	↑	↓	Dn	Dn	HLHL	DODTn	DCKEn
H	XXXX	L	L	X	float	float	float	L
H	HHHH	↑	↓	X	No change or float[3]	HHHH	DODTn	DCKEn
H	LLLH	↑	↓	X	Ilegal Input States			
H	LLHL							
H	LHLL							
H	HLLL							
L	X or float	X or float	X or float	X or float	float	float	float	L

1 It is illegal to hold both the CK and $\overline{\text{CK}}$ inputs at static logic high levels or static complementary logic levels (low and high) when $\overline{\text{RESET}}$ is driven high.

2 A/C/E = DA0..DA15, DBA0..DBA2, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, DODTn, DCKEn

3 Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

Parity, Low Power and Standby with QuadCS Mode Disabled

Inputs							Output
RESET	**DCS0**	**DCS1**	**CK[1]**	**$\overline{CK}$[1]**	**Σ of C/A[2]**	**PAR_IN[3]**	**ERROUT[4]**
H	L	X	↑	↓	Even	L	H
H	L	X	↑	↓	Odd	L	L
H	L	X	↑	↓	Even	H	L
H	L	X	↑	↓	Odd	H	H
H	X	L	↑	↓	Even	L	H
H	X	L	↑	↓	Odd	L	L
H	X	L	↑	↓	Even	H	L
H	X	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	H[5]
H	X	X	L or H	H or L	X	X	$\overline{ERROUT}_0$
H	X	X	L	L	X	X	H[6]
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

1 It is illegal to hold both the CK and $\overline{CK}$ inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when $\overline{RESET}$ is driven HIGH.

2 C/A= DAn, DBAn, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$. Inputs DCKEn, DODTn, and $\overline{DCSn}$ are not included in this range. This column represents the sum of the number of C/A signals that are electrically HIGH.

3 PAR_IN arrives one clock cycle after the data to which it applies, $\overline{ERROUT}$ is issued three clock cycles after the failing data.

4 This transition assumes $\overline{ERROUT}$ is high at the crossing of CK going high and $\overline{CK}$ going low. If $\overline{ERROUT}$ is low, it stays latched low for exactly two clock cycles or until $\overline{RESET}$ is driven low.

5 Same three cycle delay for $\overline{ERROUT}$ is valid for the de-select phase (see diagram)

6 The system is not allowed to pull CK and $\overline{CK}$ low while $\overline{ERROUT}$ is asserted.

Parity, Low Power and Standby with QuadCS Mode Enabled

Inputs						Output
$\overline{\text{RESET}}$	DCS[3:0]	CK[1]	$\overline{\text{CK}}$[1]	Σ of A/C[2]	PAR_IN[3]	$\overline{\text{ERROUT}}$[4]
H	LXXX XLXX XXLX XXXL	↑	↓	Even	L	H
H	LXXX XLXX XXLX XXXL	↑	↓	Odd	L	L
H	LXXX XLXX XXLX XXXL	↑	↓	Even	H	L
H	LXXX XLXX XXLX XXXL	↑	↓	Odd	H	H
H	HHHH	↑	↓	X	X	H[5]
H	XXXX	L or H	H or L	X	X	$\overline{\text{ERROUT}}n_0$
H	XXXX	L	L	X	X	H[6]
L	X or floating	X or floating	X or floating	X or floating	X or floating	H

1 It is illegal to hold both the CK and $\overline{\text{CK}}$ inputs at static logic high levels or static complementary logic levels (low and high) when $\overline{\text{RESET}}$ is driven high.

2 A/C = DA0..DA15, DBA0..DBA2, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$. Inputs DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ are not included in this range. This column represents the sum of the number of A/C signals that are electrically high.

3 PAR_IN arrivesone clock cycle afterdata to which it applies, $\overline{\text{ERROUT}}$ is issued three clock cycles after the failing data.

4 This transition assumes $\overline{\text{ERROUT}}$ is high at the crossing of CK going high and $\overline{\text{CK}}$ going low. If $\overline{\text{ERROUT}}$ is low, it stays latched low for exactly two clock cycles or until $\overline{\text{RESET}}$ is driven low.

5 Same three-cycle delay for $\overline{\text{ERROUT}}$ is valid for the de-select phase (see diagram)

6 The system is not allowed to pull CK and $\overline{\text{CK}}$ low while $\overline{\text{ERROUT}}$ is asserted.

PLL Function Table

Inputs					Outputs				PLL
$\overline{\text{RESET}}$	AVDD	OEn[1]	CK[2]	$\overline{\text{CK}}$[2]	Yn	$\overline{\text{Yn}}$	FBOUT	$\overline{\text{FBOUT}}$	
L	X	X	X	X	Float	Float	Float	Float	Off
H	VDD nominal	L	L	H	L	H	L	H	On
H	VDD nominal	L	H	L	H	L	H	L	On
H	VDD nominal	H	L	H	Float	Float	L	H	On
H	VDD nominal	H	H	L	Float	Float	H	L	On
H	VDD nominal	X	L	L	Float	Float	Float	Float	Off
H	GND[3]	L	L	H	L	H	L	H	Bypassed/Off
H	GND[3]	L	H	L	H	L	H	L	Bypassed/Off
H	GND[3]	H	L	H	Float	Float	L	H	Bypassed/Off
H	GND[3]	H	H	L	Float	Float	H	L	Bypassed/Off
H	GND[3]	X	L	L	Float	Float	Float	Float	Bypassed/Off
H	X	X	H	H	Reserved				

1 The Output Enable (OEn) to disable the output buffer is not an input signal to the SSTE32882HLB, but an internal signal from the PLL powerdown control and test logic. It is controlled by setting or clearing the corresponding bit in the Clock Driver mode register.

2 It is illegal to hold both the CK and $\overline{\text{CK}}$ inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when $\overline{\text{RESET}}$ is driven HIGH.

3 This is a device test mode and all register timing parameters are not guaranteed.

Absolute Maximum Ratings

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Symbol	Parameter	Conditions	Min	Max	Unit
AV_{DD}, PV_{DD}, V_{DD}	Supply voltage		–0.4	+1.975	V
V_I	Receiver input voltage[1]		–0.4	V_{DD} + 0.5	V
V_{REF}	Reference voltage		–0.4	V_{DD} + 0.5	V
V_O	Driver output voltage[1]		–0.4	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$		±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$		±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin			±100	mA
T_{STG}	Storage temperature		–65	+150	°C
$R\theta_{JA}$	Package Thermal Impedance, Junction-to-Ambient[2]	0m/s Airflow		43.8	°C/W
		1m/s Airflow		35.5	
$R\theta_{JB}$	Package Thermal Impedance, Junction-to-Board[2]			22	°C/W
$R\theta_{JC}$	Package Thermal Impedance, Junction-to-Case[2]			16.2	°C/W

1 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 1.975 V maximum.

2 The package thermal impedance is calculated in accordance with JESD51-2.

DC and AC Specifications

The SSTE32882HLB parametric values are specified for the device default control word settings, unless otherwise stated. Note that RC10 setting does not affect any of the paramteric values.

DC Specifications - Voltage

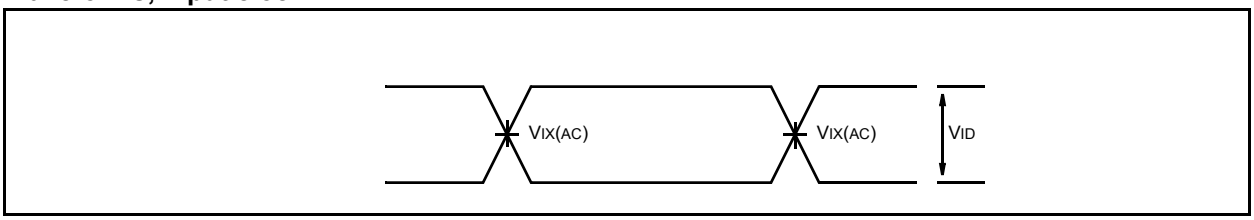
The SSTE32882 parametric values are specified for the device default control word settings, unless otherwise stated. Note that the RC10 setting does not affect any of the parametric values.

Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage (1.5V Operation)		1.425	1.5	1.575	V
	DC Supply voltage (1.35V Operation)		1.282	1.35	1.451	V
V_{REF}	DC Reference voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
V_{TT}	DC Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
$V_{IH(AC)}$	AC HIGH-level input voltage (1.5V Operation, DDR3-800/1066/1333)	Data inputs[1]	V_{REF} + 175 mV	–	V_{DD} + 0.4	V
	AC HIGH-level input voltage (1.5V Operation, DDR3-1600)	Data inputs[1]	V_{REF} + 150 mV	–	V_{DD} + 0.4	V
	AC HIGH-level input voltage (1.35V Operation, DDR3L-800/1066/1333)	Data inputs[1]	V_{REF} + 150 mV	–	V_{DD} + 0.2	V
	AC HIGH-level input voltage (1.35V Operation, DDR3L-1600)	Data inputs[1]	V_{REF} + 135 mV	–	V_{DD} + 0.2	V
$V_{IL(AC)}$	AC LOW-level input voltage (1.5V Operation, DDR3-800/1066/1333)	Data inputs[1]	–0.4	–	V_{REF} – 175 mV	V
	AC LOW-level input voltage (1.5V Operation, DDR3-1600)	Data inputs[1]	–0.4	–	V_{REF} – 150 mV	V
	AC LOW-level input voltage(1.35V Operation, DDR3L-800/1066/1333)	Data inputs[1]	–0.2	–	V_{REF} – 150 mV	V
	AC LOW-level input voltage (1.35V Operation, DDR3L-1600)	Data inputs[1]	–0.2	–	V_{REF} – 135 mV	V
$V_{IH(DC)}$	DC HIGH-level input voltage(1.5V Operation)	Data inputs[1]	V_{REF} + 100 mV	–	V_{DD} + 0.4	V
	DC HIGH-level input voltage(1.35V Operation)	Data inputs[1]	V_{REF} + 90 mV	–	V_{DD} + 0.2	V
$V_{IL(DC)}$	DC LOW-level input voltage(1.5V Operation)	Data inputs[1]	–0.4	–	V_{REF} – 100 mV	V
	DC LOW-level input voltage(1.35V Operation)	Data inputs[1]	–0.2	–	V_{REF} – 90 mV	V
$V_{IH(CMOS)}$	HIGH-level input voltage	CMOS inputs[2]	0.65 x VDD	–	V_{DD}	V
$V_{IL(CMOS)}$	LOW-level input voltage	CMOS inputs[2]	0	–	0.35 x VDD	V
$V_{IL(Static)}$	Static LOW-level input voltage[3]	CK, $\overline{CK}$,	-	–	0.35 x VDD	V
$V_{IX(AC)}$	Differential input crosspoint voltage range(1.5V Operation, DDR3-800/1066/1333/1600)	CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	0.5xV_{DD} - 175 mV	0.5 x V_{DD}	0.5xV_{DD} + 175 mV	V
			0.5xV_{DD} - 200 mV[4]	0.5 x V_{DD}	0.5xV_{DD} + 200 mV[4]	V
	Differential input crosspoint voltage range(1.35V Operation, DDR3L-800/1066/1333/1600)	CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	0.5xV_{DD} - 150 mV	0.5 x V_{DD}	0.5xV_{DD} + 150 mV	V
			0.5xV_{DD} - 180 mV[5]	0.5 x V_{DD}	0.5xV_{DD} + 180 mV[5]	V
$V_{ID(AC)}$	Differential input voltage[6] (1.5V Operation, DDR3-800/1066/1333)	CK, $\overline{CK}$	350	–	V_{DD}	mV
	Differential input voltage[6](1.5V Operation, DDR3-1600)	CK, $\overline{CK}$	300	–	V_{DD}	mV
	Differential input voltage[6](1.35V Operation, DDR3-800/1066/1333)	CK, $\overline{CK}$	300	–	V_{DD}	mV
	Differential input voltage[6] (1.35V Operation, DDR3-1600)	CK, $\overline{CK}$	270	–	V_{DD}	mV
I_{OH}	HIGH-level output current[7]	All outputs except $\overline{ERROUT}$	-11	–	–	mA
I_{OL}	LOW-level output current[7]	All outputs except $\overline{ERROUT}$	11	–	–-	mA

Symbol	Parameter	Signals	Min	Nom	Max	Unit
I_{OL}	LOW-level output current	$\overline{ERROUT}$	25	–	–	mA
V_{OD}	Differential re-driven clock swing (1.5V Operation)	Yn, $\overline{Yn}$	500	–	V_{DD}	mV
	Differential re-driven clock swing (1.35V Operation)	Yn, $\overline{Yn}$	450	–	V_{DD}	mV
V_{OX}	Differential Output Crosspoint Voltage (1.5V Operation)	Yn, $\overline{Yn}$	$0.5xV_{DD}$ – 100 mV	–	$0.5xV_{DD}$ + 100 mV	V
	Differential Output Crosspoint Voltage (1.35V Operation)	Yn, $\overline{Yn}$	$0.5xV_{DD}$ – 90 mV	–	$0.5xV_{DD}$ + 90 mV	V
		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	
T_{case} (max)	Case temperature[8]	109[9]	108[9]	106[9]	103[9]	°C

1 $\overline{DCKE0/1}$, DODT0/1, DA0..DA15, DBA0..DBA2, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$, PAR_IN, $\overline{DCS[1:0]}$ when $\overline{QCSEN}$ = HIGH, $\overline{DCS[3:0]}$ when $\overline{QCSEN}$ = LOW.
2 $\overline{RESET}$, MIRROR
3 This spec applies only when both CK and $\overline{CK}$ are actively driven LOW. It does not apply when $\overline{CK/CK}$ are floating.
4 Extended range for Vix is only allowed for clock (CK and $\overline{CK}$) and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-275 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 4 V/ns.
5 Extended range for Vix is only allowed for clock (CK and $\overline{CK}$) and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3.6 V/ns
6 VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$ See Diagram (Voltage waveforms; input clock)
7 Default settings
8 Measurement procedure JESD51-2
9 This spec is meant to guarantee a Tj of 125C by the SSTE32882 device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a SSTE32882 device shall not be higher than 125 °C.

Voltage waveforms; input clock



$V_{IX(AC)} = 0.5xV_{DD} \pm 175$ mV (1.5V operation) or $0.5xV_{DD} \pm 150$ mV (1.35 V operation)

DC Current Specifications

Operating Electrical Characteristics

Symbol	Parameter[1]	Conditions	Min	Typ[2]	Max	Unit
I_I	Input current	$\overline{RESET}$, MIRROR, $V_I = V_{DD}$ or GND			±5	µA
	$\overline{QCSEN}$ input current	$\overline{QCSEN}$, $V_I = V_{DD}$ or GND	-150		5	
I_{ID}	Input current	Data inputs[3], $V_I = V_{DD}$ or GND			±5	µA
		CK, $\overline{CK}$[4]; $V_I = V_{DD}$ or GND	-5		150	µA
I_{OH}	HIGH-level output current	Qn[5]	-11			mA
		Yn, $\overline{Yn}$, FBOUT, $\overline{FBOUT}$	-11			mA
I_{OL}	LOW-level output current	Qn[5]	11			mA
		Yn, $\overline{Yn}$, FBOUT, $\overline{FBOUT}$	11			mA
		$\overline{ERROUT}$	25			mA
I_{DD}[6]	Static standby current	$\overline{RESET}$ = GND and CK = $\overline{CK}$ = $V_{IL(AC)}$			5	mA
	Low-Power Static Operating	$\overline{RESET}$ = V_{DD} and CK = $\overline{CK}$ = $V_{IL(AC)}$, MIRROR = V_{DD}, $\overline{DCS}$[1:0] = [0,1]			15	mA
I_{CCD}	Dynamic operating -- input clock only; active outputs	$\overline{RESET}$ = V_{DD}, MIRROR = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RC0[DBA0]=0, RC0[DBA1]=0, CK and $\overline{CK}$ switching 50% duty cycle, I_O = 0, $\overline{DCS0}$ = L, $\overline{DCS1}$ = H. $V_{DD} = V_{DDMAX}$		68		µA/MHz
	Dynamic operating -- per each data input	$\overline{RESET}$ = V_{DD}, MIRROR = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at one half clock frequency, 50% duty cycle; RC0[DBA0]=0, RC0[DBA1]=0, I_O = 0, $\overline{DCS0}$ = L, $\overline{DCS1}$ = H. $V_{DD} = V_{DDMAX}$		16		µA/Clock MHz/ D Input

1 The $\overline{RESET}$ and MIRROR inputs of the device must be held at valid voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is LOW.

2 All typical values are at V_{DD} = 1.5V, T_A = 25°C.

3 DCKEn, DODTn, DAn, DBAn, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$, DCSn, PAR_IN are measured while $\overline{RESET}$ is pulled LOW.

4 The CK and $\overline{CK}$ inputs have pull-down resistors in the range of 10KΩ to 100KΩ.

5 Qn = QxAn, $\overline{QxCSn}$, QxCKEn, QxODTn, $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$, and QxBAn.

6 The supply current is measured as the total current consumption on the AV_{DD}, PV_{DD}, and V_{DD} supply current pins. Io = 0.

Capacitance Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input capacitance, Data inputs	see footnote[1]	1.5	-	2.5	pF
	Input capacitance, CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	see footnote[1]	2	-	3	pF
	Input capacitance, CK, $\overline{CK}$, FBIN, $\overline{FBIN}$ (1.35 V operation)	see footnote[1]	1.5	-	2.5	pF
C_O	Output capacitance, Re-driven and Clock Outputs	QxA0..QxA15, QxBA0..QxBA2, $\overline{QxCS0/1}$, QxCKE0/1, QxODT0/1, $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$, Y0, $\overline{Y0}$.. Y3, $\overline{Y3}$	1	-	2	pF
$C_{I\Delta}$	Delta capacitance over all inputs		-	-	0.5	pF
C_{IR}	Input capacitance, $\overline{RESET}$, MIRROR, $\overline{QCSEN}$	$V_I = V_{DD}$ or GND; V_{DD} = 1.5 V	-	-	3	pF

1 This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with VDD, VSS, AVDD, AVSS, PVDD, PVSS, V_{REF} applied and all other pins (except the pin under test) floating. Input capacitance are measured with the device default settings when MIRROR=Low.