



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



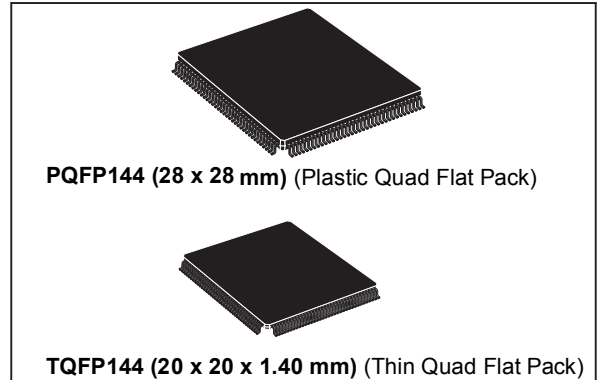


ST10F269Zx

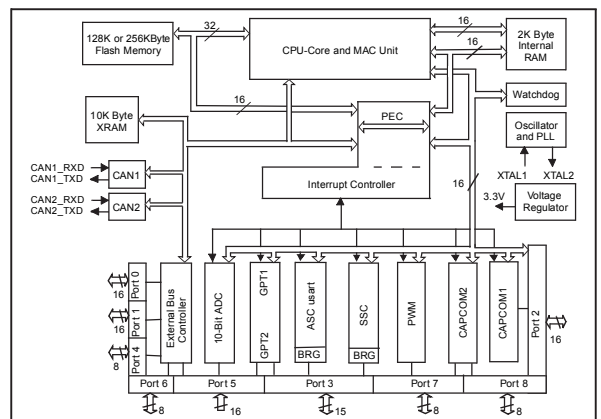
16-BIT MCU WITH MAC UNIT, 128K to 256K BYTE FLASH MEMORY AND 12K BYTE RAM

DATASHEET

- **HIGH PERFORMANCE 32 OR 40 MHZ CPU WITH DSP FUNCTION**
 - 16-bit CPU With 4-stage Pipeline
 - 50ns (or 62.5ns) Instruction Cycle Time at 40MHz (or 32MHz) Max CPU Clock
 - Multiply/accumulate Unit (Mac) 16 X 16-bit Multiplication, 40-bit Accumulator
 - Repeat Unit
 - Enhanced Boolean Bit Manipulation Facilities
 - Additional Instructions to Support HLL and Operating Systems
 - Single-cycle Context Switching Support
- **MEMORY ORGANIZATION**
 - 128K or 256K Byte On-chip Flash Memory Single Voltage With Erase/program Controller
 - Up to 1K Erasing/programming Cycles
 - Up to 16 MByte Linear Address Space For Code And Data (5 MBytes With CAN)
 - 2K Byte On-chip Internal RAM (IRAM)
 - 10K Byte On-chip Extension RAM (XRAM)
- **FAST AND FLEXIBLE BUS**
 - Programmable External Bus Characteristics for Different Address Ranges
 - 8-bit or 16-bit External Data Bus
 - Multiplexed or Demultiplexed External Address/data Buses
 - Five Programmable Chip-select Signals
 - Hold-acknowledge Bus Arbitration Support
- **INTERRUPT**
 - 8-channel Peripheral Event Controller for Single Cycle Interrupt Driven Data Transfer
 - 16-priority-level Interrupt System with 56 Sources, Sampling Rate Down to 25ns at 40MHz (31.25ns at 32MHz)
- **TIMERS**
 - Two Multi-functional General Purpose Timer Units with 5 Timers
- **TWO 16-CHANNEL CAPTURE / COMPARE UNITS**
- **A/D CONVERTER**
 - 16-channel 10-bit
 - 4.85µs Conversion Time at 40MHz CPU Clock (6.06µs at 32MHz)
- **4-CHANNEL PWM UNIT**
- **SERIAL CHANNELS**
 - Synchronous / Asynchronous Serial Channel
 - High-speed Synchronous Channel



- **TWO CAN 2.0B INTERFACES OPERATING ON ONE OR TWO CAN BUSES (30 OR 2x15 MESSAGE OBJECTS)**
- **FAIL-SAFE PROTECTION**
 - Programmable Watchdog Timer
 - Oscillator Watchdog
- **ON-CHIP BOOTSTRAP LOADER**
- **CLOCK GENERATION**
 - On-chip PLL
 - Direct or Prescaled Clock Input
- **REAL TIME CLOCK**
- **UP TO 111 GENERAL PURPOSE I/O LINES**
 - Individually Programmable as Input, Output or Special Function
 - Programmable Threshold (Hysteresis)
- **IDLE AND POWER DOWN MODES**
- **SINGLE VOLTAGE SUPPLY: 5V ±10% (EMBEDDED REGULATOR FOR 2.7 or 3.3 V CORE SUPPLY).**
- **TEMPERATURE RANGES: -40 +125°C / -40 to 85°C**
- **144-PIN PQFP/TQFP PACKAGES**



ST10F269

1 -	Introduction	6
2 -	Pin Data	7
3 -	Functional Description	13
4 -	Memory Organization	14
5 -	Internal Flash Memory	17
5.1 -	OVERVIEW	17
5.2 -	OPERATIONAL OVERVIEW	17
5.3 -	ARCHITECTURAL DESCRIPTION	19
5.3.1 -	Read Mode	19
5.3.2 -	Command Mode	19
5.3.3 -	Ready/Busy Signal	19
5.3.4 -	Flash Status Register	19
5.3.5 -	Flash Protection Register	21
5.3.6 -	Instructions Description	21
5.3.7 -	Reset Processing and Initial State	26
5.4 -	FLASH MEMORY CONFIGURATION	26
5.5 -	APPLICATION EXAMPLES	26
5.5.1 -	Handling of Flash Addresses	26
5.5.2 -	Basic Flash Access Control	27
5.5.3 -	Programming Examples	28
5.6 -	BOOTSTRAP LOADER	31
5.6.1 -	Entering the Bootstrap Loader	31
5.6.2 -	Memory Configuration After Reset	32
5.6.3 -	Loading the Startup Code	33
5.6.4 -	Exiting Bootstrap Loader Mode	33
5.6.5 -	Choosing the Baud Rate for the BSL	34
6 -	Central Processing Unit (CPU)	35
6.1 -	MULTIPLIER-ACCUMULATOR UNIT (MAC)	36
6.1.1 -	Features	37
6.1.1.1 -	Enhanced Addressing Capabilities	37
6.1.1.2 -	Multiply-Accumulate Unit	37
6.1.1.3 -	Program Control	37
6.2 -	INSTRUCTION SET SUMMARY	38
6.3 -	MAC COPROCESSOR SPECIFIC INSTRUCTIONS	39
7 -	External Bus Controller	43
7.1 -	PROGRAMMABLE CHIP SELECT TIMING CONTROL	43
7.2 -	READY PROGRAMMABLE POLARITY	43
8 -	Interrupt System	45
8.1 -	EXTERNAL INTERRUPTS	45
8.2 -	INTERRUPT REGISTERS AND VECTORS LOCATION LIST	46
8.3 -	INTERRUPT CONTROL REGISTERS	47

TABLE OF CONTENTS		PAGE
8.4 -	EXCEPTION AND ERROR TRAPS LIST	48
9 -	Capture/Compare (CAPCOM) Units	49
10 -	General Purpose Timer Unit	52
10.1 -	GPT1	52
10.2 -	GPT2	53
11 -	PWM Module	56
12 -	Parallel Ports	57
12.1 -	INTRODUCTION	57
12.2 -	I/O'S SPECIAL FEATURES	59
12.2.1 -	Open Drain Mode	59
12.2.2 -	Input Threshold Control	59
12.2.3 -	Output Driver Control	60
12.2.4 -	Alternate Port Functions	62
12.3 -	PORT0	63
12.3.1 -	Alternate Functions of PORT0	64
12.4 -	PORT1	66
12.4.1 -	Alternate Functions of PORT1	66
12.5 -	PORT 2	68
12.5.1 -	Alternate Functions of Port 2	68
12.6 -	PORT 3	71
12.6.1 -	Alternate Functions of Port 3	73
12.7 -	PORT 4	76
12.7.1 -	Alternate Functions of Port 4	77
12.8 -	PORT 5	80
12.8.1 -	Alternate Functions of Port 5	81
12.8.2 -	Port 5 Schmitt Trigger Analog Inputs	82
12.9 -	PORT 6	82
12.9.1 -	Alternate Functions of Port 6	83
12.10 -	PORT 7	86
12.10.1 -	Alternate Functions of Port 7	87
12.11 -	PORT 8	90
12.11.1 -	Alternate Functions of Port 8	91
13 -	A/D Converter	93
14 -	Serial Channels	95
14.1 -	ASYNCHRONOUS / SYNCHRONOUS SERIAL INTERFACE (ASCO)	95
14.1.1 -	ASCO in Asynchronous Mode	95
14.1.2 -	ASCO in Synchronous Mode	98
14.2 -	HIGH SPEED SYNCHRONOUS SERIAL CHANNEL (SSC)	101
15 -	CAN Modules	103
15.1 -	CAN MODULES MEMORY MAPPING	103
15.1.1 -	CAN1	103
15.1.2 -	CAN2	103
15.2 -	CAN BUS CONFIGURATIONS	103

TABLE OF CONTENTS		PAGE
16 -	Real Time Clock	105
16.1 -	RTC REGISTERS	106
16.1.1 -	RTCCON: RTC Control Register	106
16.1.2 -	RTCPH & RTCPL: RTC PRESCALER Registers	108
16.1.3 -	RTCDH & RTCDL: RTC DIVIDER Counters	108
16.1.4 -	RTCH & RTCL: RTC Programmable COUNTER Registers	109
16.1.5 -	RTCAH & RTCAL: RTC ALARM Registers	110
16.2 -	PROGRAMMING THE RTC	110
17 -	Watchdog Timer	112
18 -	System Reset	114
18.1 -	LONG HARDWARE RESET	114
18.1.1 -	Asynchronous Reset	114
18.1.2 -	Synchronous Reset (RSTIN pulse > 1040TCL and RPD pin at high level)	115
18.1.3 -	Exit of Long Hardware Reset	116
18.2 -	SHORT HARDWARE RESET	116
18.3 -	SOFTWARE RESET	117
18.4 -	WATCHDOG TIMER RESET	117
18.5 -	RSTOUT, RSTIN, BIDIRECTIONAL RESET	118
18.5.1 -	RSTOUT Pin	118
18.5.2 -	Bidirectional Reset	118
18.5.3 -	RSTIN pin	118
18.6 -	RESET CIRCUITRY	118
19 -	Power Reduction Modes	122
19.1 -	IDLE MODE	122
19.2 -	POWER DOWN MODE	122
19.2.1 -	Protected Power Down Mode	122
19.2.2 -	Interruptible Power Down Mode	122
20 -	Special Function Register Overview	125
20.1 -	IDENTIFICATION REGISTERS	131
20.2 -	SYSTEM CONFIGURATION REGISTERS	132
21 -	Electrical Characteristics	139
21.1 -	ABSOLUTE MAXIMUM RATINGS	139
21.2 -	PARAMETER INTERPRETATION	139
21.3 -	DC CHARACTERISTICS	139
21.3.1 -	A/D Converter Characteristics	144
21.3.2 -	Conversion Timing Control	145
21.4 -	AC CHARACTERISTICS	146
21.4.1 -	Test Waveforms	146
21.4.2 -	Definition of Internal Timing	146
21.4.3 -	Clock Generation Modes	148
21.4.4 -	Prescaler Operation	149
21.4.5 -	Direct Drive	149
21.4.6 -	Oscillator Watchdog (OWD)	149

TABLE OF CONTENTS		PAGE
21.4.7 -	Phase Locked Loop	149
21.4.8 -	External Clock Drive XTAL1	150
21.4.9 -	Memory Cycle Variables	151
21.4.10 -	Multiplexed Bus	152
21.4.11 -	Demultiplexed Bus	160
21.4.12 -	CLKOUT and READY	168
21.4.13 -	External Bus Arbitration	171
21.4.14 -	High-Speed Synchronous Serial Interface (SSC) Timing	174
	21.4.14.1 Master Mode	174
	21.4.14.2 Slave mode	175
22 -	Package Mechanical Data	178
23 -	Ordering Information	180

ERRATA SHEET

1 -	DESCRIPTION	181
2 -	FUNCTIONAL PROBLEMS	181
2.1 -	PWRDN.1 - EXECUTION OF PWRDN INSTRUCTION	181
2.2 -	MAC.9 - COCMP INSTRUCTION INVERTED OPERANDS	182
2.3 -	MAC.10 - E FLAG EVALUATION FOR COSHR AND COASHR INSTRUCTIONS WHEN SATURATION MODE IS ENABLED	182
2.4 -	ST_PORT.3 - BAD BEHAVIOR OF HYSTERESIS FUNCTION ON INPUT FALLING EDGE	183
3 -	DEVIATIONS FROM DC/AC PRELIMINARY SPECIFICATION	183
4 -	ERRATA SHEET VERSION INFORMATION	183

1 - INTRODUCTION

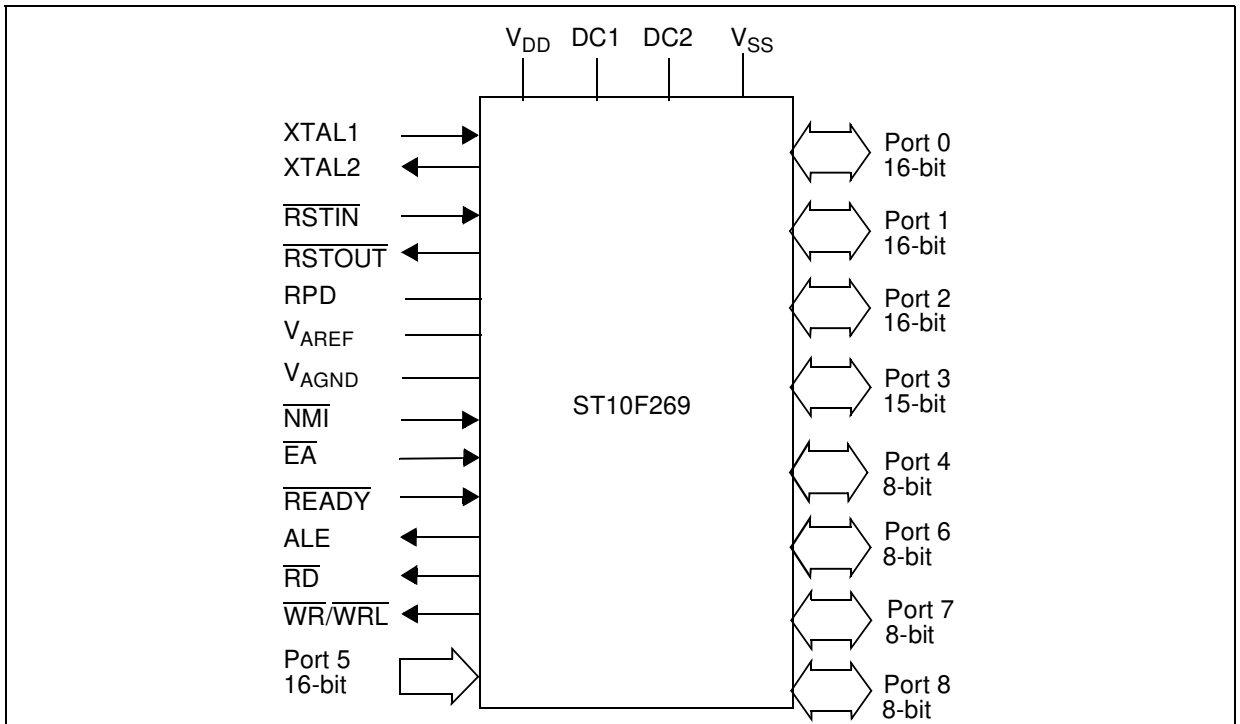
The ST10F269 is a derivative of the STMicroelectronics ST10 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 20 million instructions per second) with high peripheral functionality and enhanced I/O-capabilities. It also provides on-chip high-speed single voltage Flash memory, on-chip high-speed RAM, and clock generation via PLL.

ST10F269 is processed in 0.35 μ m CMOS technology. The MCU core and the logic is supplied with a 5V to 3.3V on chip voltage regulator on PQFP144 devices (or 5V to 2.7V on TQFP144 devices). The part is supplied with a single 5V supply and I/Os work at 5V.

The device is upward compatible with the ST10F168 device, with the following set of differences:

- The Multiply/Accumulate unit is available as standard. This MAC unit adds powerful DSP functions to the ST10 architecture, but maintains full compatibility for existing code.
- Flash control interface is now based on STMicroelectronics third generation of stand-alone Flash memories, with an embedded Erase/Program Controller. This completely frees up the CPU during programming or erasing the Flash.
- 128-KByte Flash Option
- Two dedicated pins (DC1 and DC2) on the 144-pin package are used for decoupling the internally generated 3.3V (or 2.7V on TQFP144 devices) core logic supply. **Do not connect these two pins to 5.0V external supply.** Instead, these pins should be connected to a decoupling capacitor (ceramic type, value ≥ 330 nF).
- The A/D Converter characteristics are different from previous ST10 derivatives ones. Refer to *Section 21.3.1* -.
- The AC and DC parameters are adapted to the 40MHz maximum CPU frequency on PQFP144 devices (32MHz on TQFP144 devices). The characterization is performed with $C_L = 50$ pF max on output pins. Refer to *Section 21.3* -.
- In order to reduce EMC, the rise/fall time and the sink/source capability of the drivers of the I/O pads are programmable. Refer to *Section 12.2* -.
- The Real Time Clock functionality is added.
- The external interrupt sources can be selected with the EXISEL register.
- The reset source is identified by a dedicated status bit in the WDTCN register.

Figure 1 : Logic Symbol



2 - PIN DATA

Figure 2 : Pin Configuration (top view)

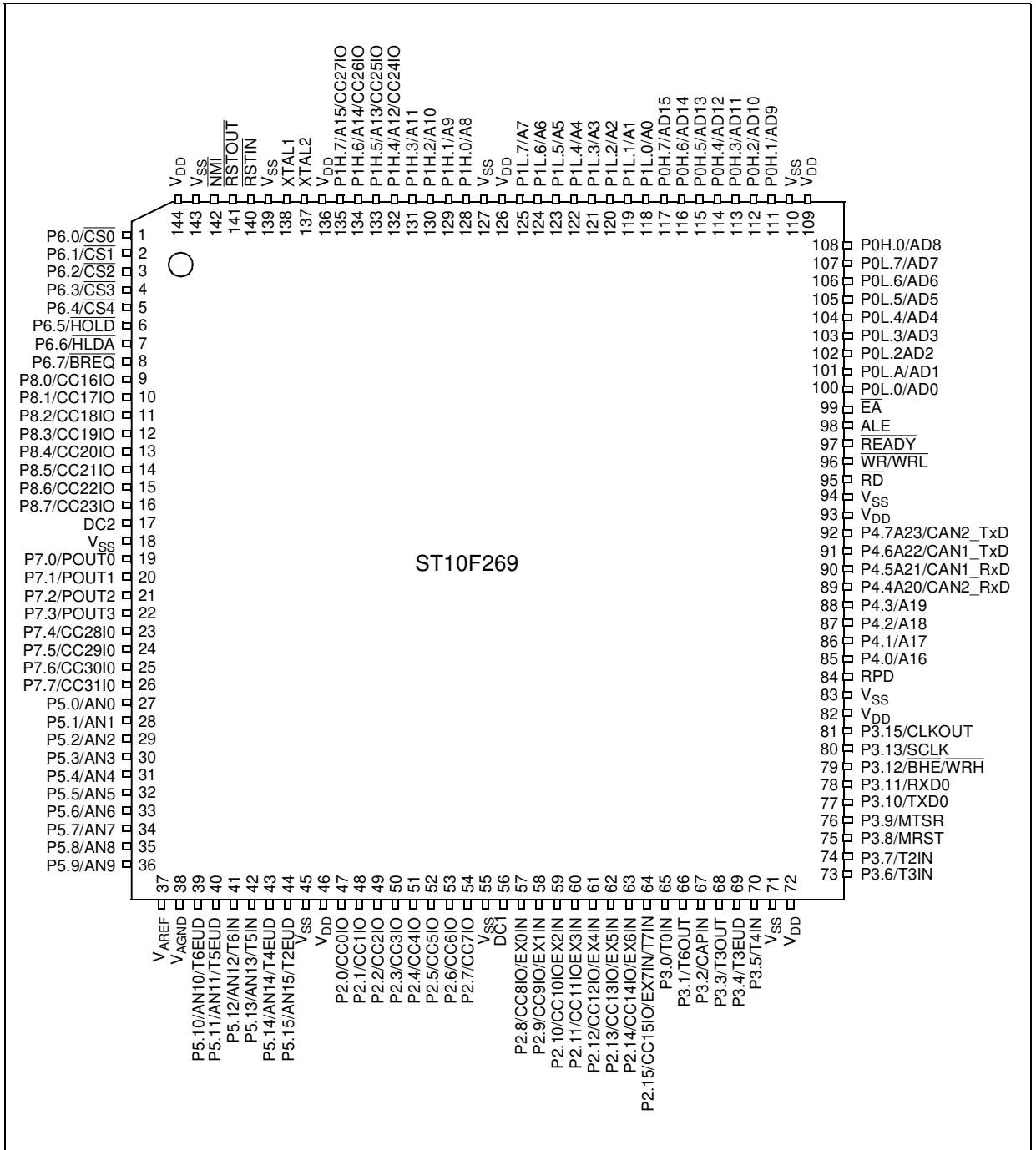


Table 1 : Pin Description

Symbol	Pin	Type	Function
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push-pull or open drain drivers. The following Port 6 pins have alternate functions:
	1	O	P6.0 $\overline{CS0}$ Chip Select 0 Output

	5	O	P6.4 $\overline{CS4}$ Chip Select 4 Output
	6	I	P6.5 \overline{HOLD} External Master Hold Request Input
	7	O	P6.6 \overline{HLDA} Hold Acknowledge Output
	8	O	P6.7 \overline{BREQ} Bus Request Output
P8.0 - P8.7	9-16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins have alternate functions:
	9	I/O	P8.0 CC16IO CAPCOM2: CC16 Capture Input / Compare Output

	16	I/O	P8.7 CC23IO CAPCOM2: CC23 Capture Input / Compare Output
P7.0 - P7.7	19-26	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 7 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins have alternate functions:
	19	O	P7.0 POUT0 PWM Channel 0 Output

	22	O	P7.3 POUT3 PWM Channel 3 Output
	23	I/O	P7.4 CC28IO CAPCOM2: CC28 Capture Input / Compare Output

	26	I/O	P7.7 CC31IO CAPCOM2: CC31 Capture Input / Compare Output
P5.0 - P5.9 P5.10 - P5.15	27-36 39-44	I I	16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 can be the analog input channels (up to 16) for the A/D converter, where P5.x equals ANx (Analog input channel x), or they are timer inputs:
	39	I	P5.10 T6EUD GPT2 Timer T6 External Up / Down Control Input
	40	I	P5.11 T5EUD GPT2 Timer T5 External Up / Down Control Input
	41	I	P5.12 T6IN GPT2 Timer T6 Count Input
	42	I	P5.13 T5IN GPT2 Timer T5 Count Input
	43	I	P5.14 T4EUD GPT1 Timer T4 External Up / Down Control Input
	44	I	P5.15 T2EUD GPT1 Timer T2 External Up / Down Control Input

Symbol	Pin	Type	Function		
P2.0 - P2.7 P2.8 - P2.15	47-54 57-64	I/O	16-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 2 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins have alternate functions:		
	47	I/O	P2.0	CC0IO	CAPCOM: CC0 Capture Input / Compare Output

	54	I/O	P2.7	CC7IO	CAPCOM: CC7 Capture Input / Compare Output
	57	I/O	P2.8	CC8IO	CAPCOM: CC8 Capture Input / Compare Output
		I		EX0IN	Fast External Interrupt 0 Input

	64	I/O	P2.15	CC15IO	CAPCOM: CC15 Capture Input / Compare Output
		I		EX7IN	Fast External Interrupt 7 Input
		I		T7IN	CAPCOM2 Timer T7 Count Input
P3.0 - P3.5 P3.6 - P3.13, P3.15	65-70, 73-80, 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins have alternate functions:		
	65	I	P3.0	T0IN	CAPCOM Timer T0 Count Input
	66	O	P3.1	T6OUT	GPT2 Timer T6 Toggle Latch Output
	67	I	P3.2	CAPIN	GPT2 Register CAPREL Capture Input
	68	O	P3.3	T3OUT	GPT1 Timer T3 Toggle Latch Output
	69	I	P3.4	T3EUD	GPT1 Timer T3 External Up / Down Control Input
	70	I	P3.5	T4IN	GPT1 Timer T4 Input for Count / Gate / Reload / Capture
	73	I	P3.6	T3IN	GPT1 Timer T3 Count / Gate Input
	74	I	P3.7	T2IN	GPT1 Timer T2 Input for Count / Gate / Reload / Capture
	75	I/O	P3.8	MRST	SSC Master-Receiver / Slave-Transmitter I/O
	76	I/O	P3.9	MTSR	SSC Master-Transmitter / Slave-Receiver O/I
	77	O	P3.10	TxD0	ASC0 Clock / Data Output (Asynchronous / Synchronous)
	78	I/O	P3.11	RxD0	ASC0 Data Input (Asynchronous) or I/O (Synchronous)
	79	O	P3.12	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal
				$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
	80	I/O	P3.13	SCLK	SSC Master Clock Output / Slave Clock Input
	81	O	P3.15	CLKOUT	System Clock Output (=CPU Clock)

Symbol	Pin	Type	Function
P4.0 –P4.7	85-92	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold is selectable (TTL or special). Port 4.6 & 4.7 outputs can be configured as push-pull or open drain drivers. In case of an external bus configuration, Port 4 can be used to output the segment address lines:
	85	O	P4.0 A16 Segment Address Line
	86	O	P4.1 A17 Segment Address Line
	87	O	P4.2 A18 Segment Address Line
	88	O	P4.3 A19 Segment Address Line
	89	O	P4.4 A20 Segment Address Line
		I	CAN2_RxD CAN2 Receive Data Input
	90	O	P4.5 A21 Segment Address Line
		I	CAN1_RxD CAN1 Receive Data Input
	91	O	P4.6 A22 Segment Address Line
		O	CAN1_TxD CAN1 Transmit Data Output
	92	O	P4.7 A23 Most Significant Segment Address Line
		O	CAN2_TxD CAN2 Transmit Data Output
\overline{RD}	95	O	External Memory Read Strobe. \overline{RD} is activated for every external instruction or data read access.
$\overline{WR/WRL}$	96	O	External Memory Write Strobe. In \overline{WR} -mode this pin is activated for every external data write access. In \overline{WRL} mode this pin is activated for low Byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection.
READY/ READY	97	I	Ready Input. The active level is programmable. When the Ready function is enabled, the selected inactive level at this pin, during an external memory access, will force the insertion of waitstate cycles until the pin returns to the selected active level.
ALE	98	O	Address Latch Enable Output. In case of use of external addressing or of multiplexed mode, this signal is the latch command of the address lines.
\overline{EA}	99	I	External Access Enable pin. A low level applied to this pin during and after Reset forces the ST10F269 to start the program from the external memory space. A high level forces the MCU to start in the internal memory space.

Symbol	Pin	Type	Function																				
P0L.0 - P0L.7, P0H.0 P0H.1 - P0H.7	100-107, 108, 111-117	I/O	<p>Two 8-bit bidirectional I/O ports P0L and P0H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state.</p> <p>In case of an external bus configuration, PORT0 serves as the address (A) and as the address / data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.</p> <p>Demultiplexed bus modes</p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>D0 – D7</td> <td>D0 - D7</td> </tr> <tr> <td>P0H.0 – P0H.7</td> <td>I/O</td> <td>D8 - D15</td> </tr> </table> <p>Multiplexed bus modes</p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>AD0 – AD7</td> <td>AD0 - AD7</td> </tr> <tr> <td>P0H.0 – P0H.7</td> <td>A8 – A15</td> <td>AD8 - AD15</td> </tr> </table>	Data Path Width:	8-bit	16-bit	P0L.0 – P0L.7:	D0 – D7	D0 - D7	P0H.0 – P0H.7	I/O	D8 - D15	Data Path Width:	8-bit	16-bit	P0L.0 – P0L.7:	AD0 – AD7	AD0 - AD7	P0H.0 – P0H.7	A8 – A15	AD8 - AD15		
Data Path Width:	8-bit	16-bit																					
P0L.0 – P0L.7:	D0 – D7	D0 - D7																					
P0H.0 – P0H.7	I/O	D8 - D15																					
Data Path Width:	8-bit	16-bit																					
P0L.0 – P0L.7:	AD0 – AD7	AD0 - AD7																					
P0H.0 – P0H.7	A8 – A15	AD8 - AD15																					
P1L.0 - P1L.7 P1H.0 - P1H.7	118-125 128-135	I/O	<p>Two 8-bit bidirectional I/O ports P1L and P1H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.</p> <p>The following PORT1 pins have alternate functions:</p> <table> <tr> <td>132</td> <td>I</td> <td>P1H.4</td> <td>CC24IO</td> <td>CAPCOM2: CC24 Capture Input</td> </tr> <tr> <td>133</td> <td>I</td> <td>P1H.5</td> <td>CC25IO</td> <td>CAPCOM2: CC25 Capture Input</td> </tr> <tr> <td>134</td> <td>I</td> <td>P1H.6</td> <td>CC26IO</td> <td>CAPCOM2: CC26 Capture Input</td> </tr> <tr> <td>135</td> <td>I</td> <td>P1H.7</td> <td>CC27IO</td> <td>CAPCOM2: CC27 Capture Input</td> </tr> </table>	132	I	P1H.4	CC24IO	CAPCOM2: CC24 Capture Input	133	I	P1H.5	CC25IO	CAPCOM2: CC25 Capture Input	134	I	P1H.6	CC26IO	CAPCOM2: CC26 Capture Input	135	I	P1H.7	CC27IO	CAPCOM2: CC27 Capture Input
132	I	P1H.4	CC24IO	CAPCOM2: CC24 Capture Input																			
133	I	P1H.5	CC25IO	CAPCOM2: CC25 Capture Input																			
134	I	P1H.6	CC26IO	CAPCOM2: CC26 Capture Input																			
135	I	P1H.7	CC27IO	CAPCOM2: CC27 Capture Input																			
XTAL1 XTAL2	138 137	I O	<p>XTAL1 Oscillator amplifier and/or external clock input.</p> <p>XTAL2 Oscillator amplifier circuit output.</p> <p>To clock the device from an external source, drive XTAL1 while leaving XTAL2 unconnected. Minimum and maximum high / low and rise / fall times specified in the AC Characteristics must be observed.</p>																				
RSTIN	140	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10F269. An internal pull-up resistor permits power-on reset using only a capacitor connected to V _{SS} . In bidirectional reset mode (enabled by setting bit BDRSTEN in SYSCON register), the RSTIN line is pulled low for the duration of the internal reset sequence.																				
RSTOUT	141	O	Internal Reset Indication Output. This pin is driven to a low level during hardware, software or watchdog timer reset. RSTOUT remains low until the EINIT (end of initialization) instruction is executed.																				
NMI	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the ST10F269 to go into power down mode. If NMI is high and PWDCFG = '0', when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.																				
V _{AREF}	37	-	A/D converter reference voltage.																				
V _{AGND}	38	-	A/D converter reference ground.																				
RPD	84	-	Timing pin for the return from interruptible powerdown mode and synchronous / asynchronous reset selection.																				

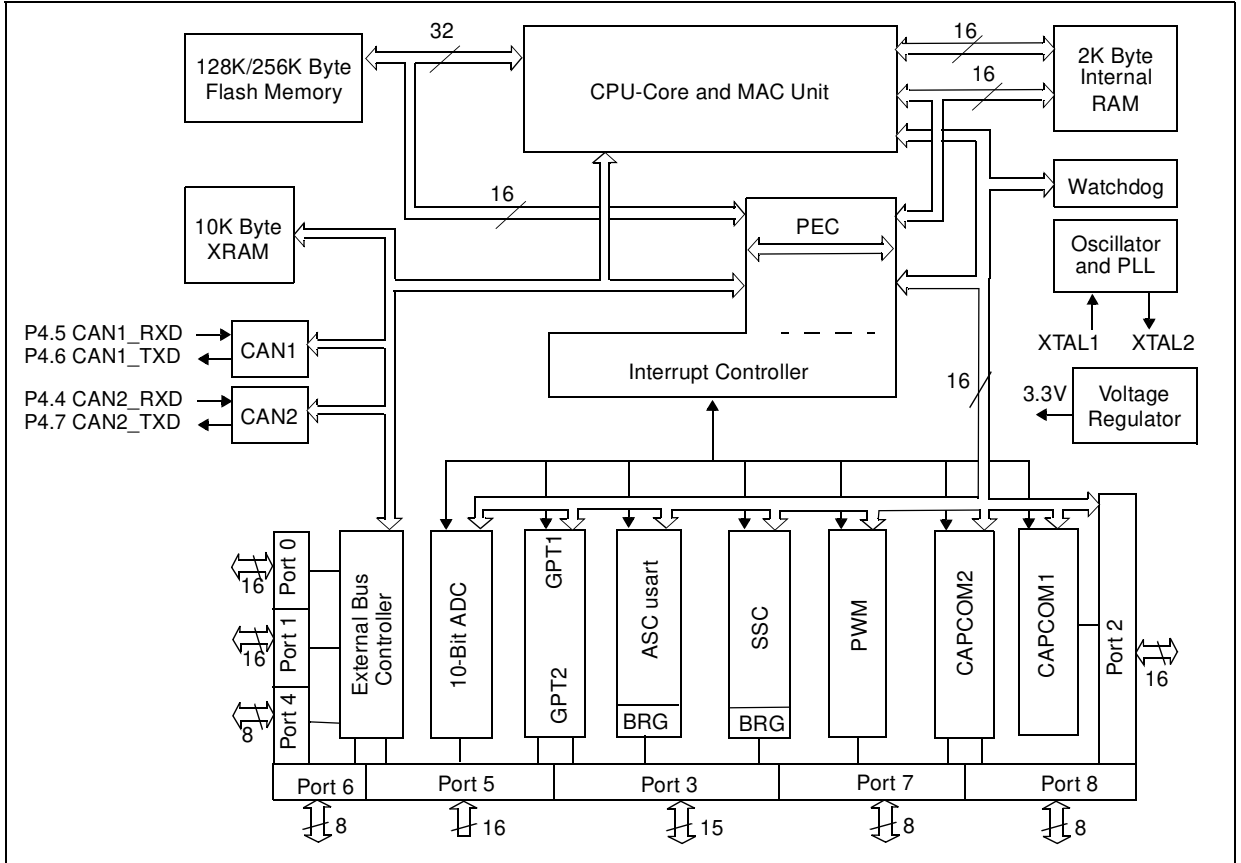
Symbol	Pin	Type	Function
V _{DD}	46, 72, 82,93, 109, 126, 136, 144	-	Digital Supply Voltage: = + 5V during normal operation and idle mode.
V _{SS}	18,45, 55,71, 83,94, 110, 127, 139, 143	-	Digital Ground.
DC1 DC2	56 17	- -	3.3V Decoupling pin (2.7V on TQFP144 devices): a decoupling capacitor of ≥ 330 nF must be connected between this pin and nearest V _{SS} pin.

3 - FUNCTIONAL DESCRIPTION

The architecture of the ST10F269 combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The

block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F269.

Figure 3 : Block Diagram



4 - MEMORY ORGANIZATION

The memory space of the ST10F269 is configured in a unified memory architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16M Bytes. The entire memory space can be accessed Byte wise or Word wise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

Flash: 128K or 256K Bytes of on-chip Flash memory.

IRAM: 2K Bytes of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. A register bank is 16 Wordwide (R0 to R15) and / or Byte-wide (RL0, RH0, ..., RL7, RH7) general purpose registers.

XRAM: 10K Bytes of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.

The XRAM is divided into 2 areas, the first 2K Bytes named XRAM1 and the second 8K Bytes named XRAM2, connected to the internal XBUS and are accessed like an external memory in 16-bit demultiplexed bus-mode without wait state or read/write delay (50ns access at 40MHz CPU clock on PQFP144 devices and 62.5ns access at 32MHz CPU clock on TQFP144 devices). Byte and Word accesses are allowed.

The XRAM1 address range is 00'E000h - 00'E7FFh if XPEN (bit 2 of SYSCON register), and XRAM1EN (bit 2 of XPERCON register) are set. If XRAM1EN or XPEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register

The XRAM2 address range is 00'C000h - 00'DFFFh if XPEN (bit 2 of SYSCON register), and XRAM2 (bit 3 of XPERCON register) are set). If bit XRAM2EN or XPEN is cleared, then any access in the address range 00'C000h - 00'DFFFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

As the XRAM appears like external memory, it cannot be used as system stack or as register banks. The XRAM is not provided for single bit storage and therefore is not bit addressable.

SFR/ESFR: 1024 Bytes (2 x 512 Bytes) of address space is reserved for the special function register areas. SFRs are Wordwide registers

which are used to control and to monitor the function of the different on-chip units.

CAN1: Address range 00'EF00h - 00'EFFFh is reserved for the CAN1 Module access. The CAN1 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN1EN bit 0 of the new XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (Byte accesses are possible). Two wait states give an access time of 100ns at 40MHz CPU clock on PQFP144 devices (or 125ns at 32MHz CPU clock on TQFP144 devices). No tri-state wait states are used.

CAN2: Address range 00'EE00h - 00'EEFFh is reserved for the CAN2 Module access. The CAN2 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN2EN bit 1 of the new XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (Byte accesses are possible). Two wait states give an access time of 100ns at 40MHz CPU clock on PQFP144 devices (or 125ns at 32MHz CPU clock on TQFP144 devices). No tri-state wait states are used.

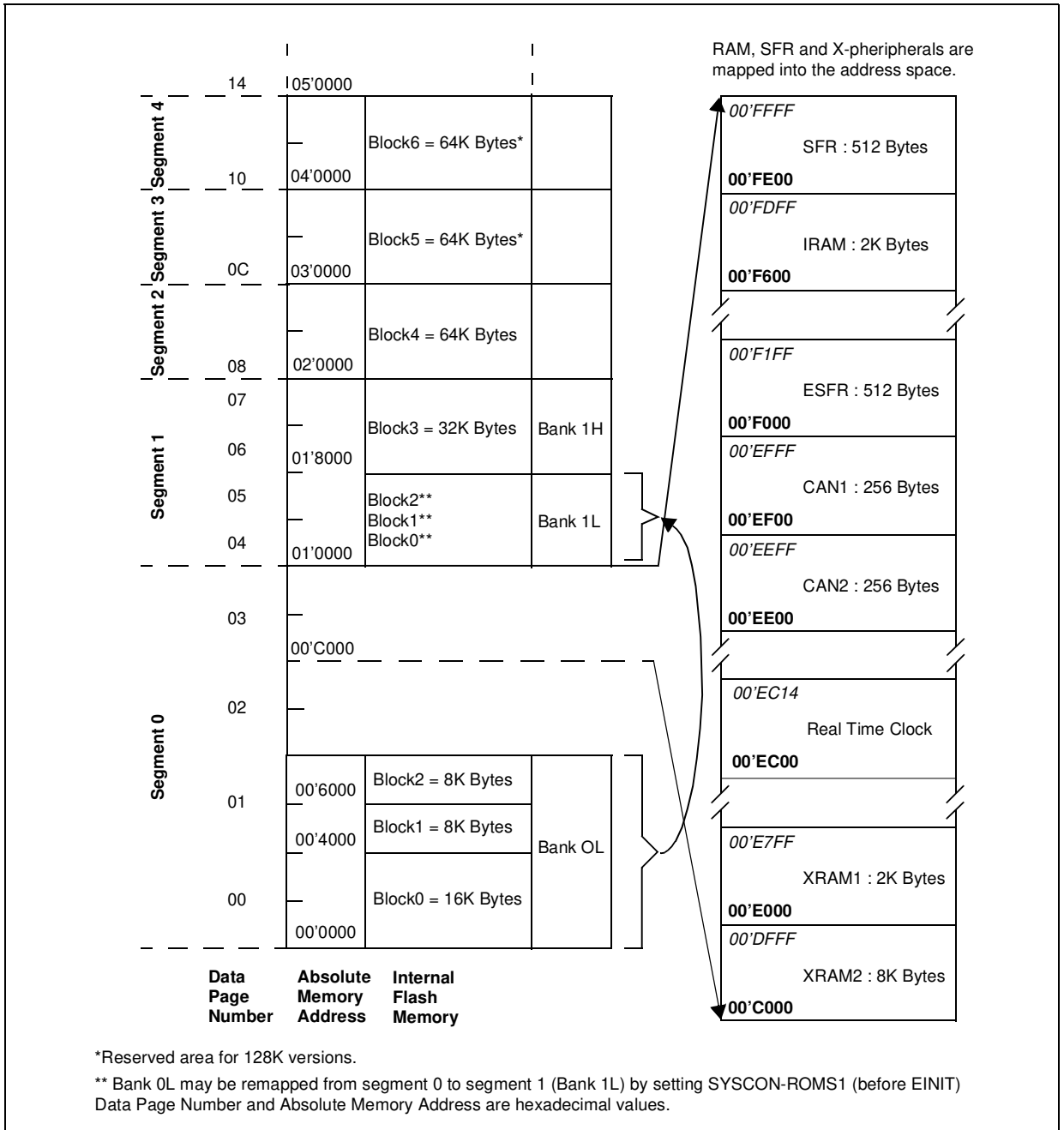
In order to meet the needs of designs where more memory is required than is provided on chip, up to 16M Bytes of external RAM and/or ROM can be connected to the microcontroller.

Note If one or the two CAN modules are used, Port 4 cannot be programmed to output all 8 segment address lines. Thus, only 4 segment address lines can be used, reducing the external memory space to 5M Bytes (1M Byte per \overline{CS} line).

Visibility of XBUS Peripherals

In order to keep the ST10F269 compatible with the ST10C167 and with the ST10F167, the XBUS peripherals can be selected to be visible and / or accessible on the external address / data bus. CAN1EN and CAN2EN bits of XPERCON register must be set. If these bits are cleared before the global enabling with XPEN-bit in SYSCON register, the corresponding address space, port pins and interrupts are not occupied by the peripheral, thus the peripheral is not visible and not available. Refer to Chapter : *Special Function Register Overview* on page 125.

Figure 4 : ST10F269 On-chip Memory Mapping



XPERCON (F024h / 12h)											ESFR					Reset Value: - - 05h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	-	-	-	-	RTCEN	XRAM2EN	XRAM1EN	CAN2EN	CAN1EN	
											RW	RW	RW	RW	RW	

CAN1EN	<p>CAN1 Enable Bit</p> <p>'0': Accesses to the on-chip CAN1 XPeripheral and its functions are disabled. P4.5 and P4.6 pins can be used as general purpose I/Os. Address range 00'EF00h-00'EFFh is only directed to external memory if CAN2EN is also '0'.</p> <p>'1': The on-chip CAN1 XPeripheral is enabled and can be accessed.</p>
CAN2EN	<p>CAN2 Enable Bit</p> <p>'0': Accesses to the on-chip CAN2 XPeripheral and its functions are disabled. P4.4 and P4.7 pins can be used as general purpose I/Os. Address range 00'EE00h-00'EEFFh is only directed to external memory if CAN1EN is also '0'.</p> <p>'1': The on-chip CAN2 XPeripheral is enabled and can be accessed.</p>
XRAM1EN	<p>XRAM1 Enable Bit</p> <p>'0': Accesses to external memory within space 00'E000h to 00'E7FFh. The 2K Bytes of internal XRAM1 are disabled.</p> <p>'1': Accesses to the internal 2K Bytes of XRAM1.</p>
XRAM2EN	<p>XRAM2 Enable Bit</p> <p>'0': Accesses to the external memory within space 00'C000h to 00'DFFFh. The 8K Bytes of internal XRAM2 are disabled.</p> <p>'1': Accesses to the internal 8K Bytes of XRAM2.</p>
RTCEN	<p>RTC Enable Bit</p> <p>'0': Accesses to the on-chip Real Time Clock are disabled, external access is performed. Address range 00'EC00h-00'ECFFh is only directed to external memory if CAN1EN and CAN2EN are '0' also</p> <p>'1': The on-chip Real Time Clock is enabled and can be accessed.</p>

Note: - When both CAN are disabled via XPERCON setting, then any access in the address range 00'EE00h - 00'EFFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register. P4.4 and P4.7 can be used as General Purpose I/O when CAN2 is disabled, and P4.5 and P4.6 can be used as General Purpose I/O when CAN1 is disabled.

- The default XPER selection after Reset is identical to XBUS configuration of ST10C167: XCAN1 is enabled, XCAN2 is disabled, XRAM1 (2K Byte compatible XRAM) is enabled, XRAM2 (new 8K Byte XRAM) is disabled.

- Register XPERCON cannot be changed after the global enabling of XPeripherals, i.e. after the setting of bit XPEN in the SYSCON register.

- In EMUlation mode, all the XPERipherals are enabled (XPERCON bit are all set).

The access to external memory and/or XBus is controlled by the bondout chip.

- When the Real Time Clock is disabled (RTCEN = 0), the clock oscillator is switch-off if the ST10 enters in power-down mode. Otherwise, when the Real Time Clock is enabled, the bit RTCOFF of the RTCCON register allows to choose the power-down mode of the clock oscillator (See Chapter : *Real Time Clock* on page 105).

5 - INTERNAL FLASH MEMORY

5.1 - Overview

- 128K or 256K Byte on-chip Flash memory
- Two possibilities of Flash mapping into the CPU address space
- Flash memory can be used for code and data storage
- 32-bit, zero waitstate read access (50ns cycle time at $f_{CPU} = 40\text{MHz}$ on PQFP144 devices and 62.5ns cycle time at $f_{CPU} = 32\text{MHz}$ on TQFP144 devices)
- Erase-Program Controller (EPC) similar to M29F400B STM's stand-alone Flash memory
 - Word-by-Word Programmable (16 μs typical)
 - Data polling and Toggle Protocol for EPC Status
 - Ready/Busy signal connected on XP2INT interrupt line
 - Internal Power-On detection circuit
- Memory Erase in blocks
 - One 16K Byte, two 8K Byte, one 32K Byte, one to three 64K Byte blocks
 - Each block can be erased separately (1.5 second typical)
 - Chip erase (8.5 second typical)
 - Each block can be separately protected against programming and erasing
 - Each protected block can be temporary unprotected
 - When enabled, the read protection prevents access to data in Flash memory using a program running out of the Flash memory space.

Access to data of internal Flash can only be performed with an inner protected program

- Erase Suspend and Resume Modes
 - Read and Program another Block during erase suspend
- Single Voltage operation, no need of dedicated supply pin
- Low Power Consumption:
 - 45mA max. Read current
 - 60mA max. Program or Erase current
 - Automatic Stand-by-mode (50 μA maximum)
- 1000 Erase-Program Cycles per block, 20 years of data retention time
- Operating temperature: -40 to +125 $^{\circ}\text{C}$ / -40 to +125 $^{\circ}\text{C}$

5.2 - Operational Overview

Read Mode

In standard mode (the normal operating mode) the Flash appears like an on-chip ROM with the same timing and functionality. The Flash module offers a fast access time, allowing zero waitstate access with CPU frequency up to 40MHz on PQFP144 devices and up to 32MHz on TQFP144 devices. Instruction fetches and data operand reads are performed with all addressing modes of the ST10F269 instruction set.

In order to optimize the programming time of the internal Flash, blocks of 8K Bytes, 16K Bytes, 32K Bytes, 64K Bytes can be used. But the size of the blocks does not apply to the whole memory space, see details in Table 2.

Table 2 : 128K or 256K Byte Flash Memory Block Organization

Block	Addresses (Segment 0)	Addresses (Segment 1)	Size (byte)
0	00'0000h to 00'3FFFh	01'0000h to 01'3FFFh	16K
1	00'4000h to 00'5FFFh	01'4000h to 01'5FFFh	8K
2	00'6000h to 00'7FFFh	01'6000h to 01'7FFFh	8K
3	01'8000h to 01'FFFFh	01'8000h to 01'FFFFh	32K
4	02'0000h to 02'FFFFh	02'0000h to 02'FFFFh	64K
5*	03'0000h to 03'FFFFh*	03'0000h to 03'FFFFh*	64K*
6*	04'0000h to 04'FFFFh*	04'0000h to 04'FFFFh*	64K*

*Not available on 128K versions (reserved areas).

Instructions and Commands

All operations besides normal read operations are initiated and controlled by command sequences written to the Flash Command Interface (CI). The Command Interface (CI) interprets words written to the Flash memory and enables one of the following operations:

- Read memory array
- Program Word
- Block Erase
- Chip Erase
- Erase Suspend
- Erase Resume
- Block Protection
- Block Temporary Unprotection
- Code Protection

Commands are composed of several write cycles at specific addresses of the Flash memory. The different write cycles of such command sequences offer a fail-safe feature to protect against an inadvertent write.

A command only starts when the Command Interface has decoded the last write cycle of an operation. Until that last write is performed, Flash memory remains in Read Mode

Notes: 1. As it is not possible to perform write operations in the Flash while fetching code from Flash, the Flash commands must be written by instructions executed from internal RAM or external memory.

2. Command write cycles do not need to be consecutively received, pauses are allowed, save for Block Erase command. During this operation all Erase Confirm commands must be sent to complete any block erase operation before time-out period expires (typically 96 μ s). Command sequencing must be followed exactly. Any invalid combination of commands will reset the Command Interface to Read Mode.

Status Register

This register is used to flag the status of the memory and the result of an operation. This register can be accessed by read cycles during the Erase-Program Controller (EPC) operation.

Erase Operation

This Flash memory features a block erase architecture with a chip erase capability too. Erase is accomplished by executing the six cycle erase command sequence. Additional command write

cycles can then be performed to erase more than one block in parallel. When a time-out period elapses (96 μ s) after the last cycle, the Erase-Program Controller (EPC) automatically starts and times the erase pulse and executes the erase operation. There is no need to program the block to be erased with '0000h' before an erase operation. Termination of operation is indicated in the Flash status register. After erase operation, the Flash memory locations are read as 'FFFFh' value.

Erase Suspend

A block erase operation is typically executed within 1.5 second for a 64K Byte block. Erasure of a memory block may be suspended, in order to read data from another block or to program data in another block, and then resumed.

In-System Programming

In-system programming is fully supported. No special programming voltage is required. Because of the automatic execution of erase and programming algorithms, write operations are reduced to transferring commands and data to the Flash and reading the status. Any code that programs or erases Flash memory locations (that writes data to the Flash) must be executed from memory outside the on-chip Flash memory itself (on-chip RAM or external memory).

A boot mechanism is provided to support in-system programming. It works using serial link via USART interface and a PC compatible or other programming host.

Read/Write Protection

The Flash module supports read and write protection in a very comfortable and advanced protection functionality. If Read Protection is installed, the whole Flash memory is protected against any "external" read access; read accesses are only possible with instructions fetched directly from program Flash memory. For update of the Flash memory a temporary disable of Flash Read Protection is supported.

The device also features a block write protection. Software locking of selectable memory blocks is provided to protect code and data. This feature will disable both program and erase operations in the selected block(s) of the memory. Block Protection is accomplished by block specific lock-bit which are programmed by executing a four cycle command sequence. The locked state of blocks is indicated by specific flags in the according block status registers. A block may only

be temporarily unlocked for update (write) operations.

With the two possibilities for write protection - whole memory or block specific - a flexible installation of write protection is supported to protect the Flash memory or parts of it from unauthorized programming or erase accesses and to provide virus-proof protection for all system code blocks. All write protection also is enabled during boot operation.

Power Supply, Reset

The Flash module uses a single power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations from 5V supply. Once a program or erase cycle has been completed, the device resets to the standard read mode. At power-on, the Flash memory has a setup phase of some microseconds (dependent on the power supply ramp-up). During this phase, Flash can not be read. Thus, if EA pin is high (execution will start from Flash memory), the CPU will remain in reset state until the Flash can be accessed.

5.3 - Architectural Description

The Flash module distinguishes two basic operating modes, the standard read mode and the command mode. The initial state after power-on and after reset is the standard read mode.

5.3.1 - Read Mode

The Flash module enters the standard operating mode, the read mode:

- After Reset command
- After every completed erase operation
- After every completed programming operation
- After every other completed command execution
- Few microseconds after a CPU-reset has started
- After incorrect address and data values of command sequences or writing them in an improper sequence
- After incorrect write access to a read protected Flash memory

The read mode remains active until the last command of a command sequence is decoded which starts directly a Flash array operation, such as:

- erase one or several blocks
- program a word into Flash array
- protect / temporary unprotect a block.

In the standard read mode read accesses are directly controlled by the Flash memory array, delivering a 32-bit double Word from the addressed position. Read accesses are always aligned to double Word boundaries. Thus, both low order address bit A1 and A0 are not used in the Flash array for read accesses. The high order address bit A17/A16 define the physical 64K Byte segment being accessed within the Flash array.

5.3.2 - Command Mode

Every operation besides standard read operations is initiated by commands written to the Flash command register. The addresses used for command cycles define in conjunction with the actual state the specific step within command sequences. With the last command of a command sequence, the Erase-Program Controller (EPC) starts the execution of the command. The EPC status is indicated during command execution by:

- The Status Register,
- The Ready/Busy signal.

5.3.3 - Ready/Busy Signal

The Ready/Busy (\bar{R}/B) signal is connected to the XPER2 interrupt node (XP2IC). When \bar{R}/B is high, the Flash is busy with a Program or Erase operation and will not accept any additional program or erase instruction. When \bar{R}/B is Low, the Flash is ready for any Read/Write or Erase operation. The \bar{R}/B will also be low when the memory is put in Erase Suspend mode.

This signal can be polled by reading XP2IC register, or can be used to trigger an interrupt when the Flash goes from Busy to Ready.

5.3.4 - Flash Status Register

The Flash Status register is used to flag the status of the Flash memory and the result of an operation. This register can be accessed by Read cycles during the program-Erase Controller operations. The program or erase operation can be controlled by data polling on bit FSB.7 of Status Register, detection of Toggle on FSB.6 and FSB.2, or Error on FSB.5 and Erase Time-out on FSB.3 bit. Any read attempt in Flash during EPC operation will automatically output these five bits. The EPC sets bit FSB.2, FSB.3, FSB.5, FSB.6 and FSB.7. Other bits are reserved for future use and should be masked.

Flash Status (see note for address)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	FSB.7	FSB.6	FSB.5	-	FSB.3	FSB.2	-	-
								R	R	R		R	R		

FSB.7	<p>Flash Status bit 7: Data Polling Bit</p> <p>Programming Operation: this bit outputs the complement of the bit 7 of the word being programmed, and after completion, will output the bit 7 of the word programmed.</p> <p>Erasing Operation: outputs a '0' during erasing, and '1' after erasing completion.</p> <p>If the block selected for erasure is (are) protected, FSB.7 will be set to '0' for about 100 μs, and then return to the previous addressed memory data value.</p> <p>FSB.7 will also flag the Erase Suspend Mode by switching from '0' to '1' at the start of the Erase Suspend.</p> <p>During Program operation in Erase Suspend Mode, FSB.7 will have the same behaviour as in normal Program execution outside the Suspend mode.</p>
FSB.6	<p>Flash Status bit 6: Toggle Bit</p> <p>Programming or Erasing Operations: successive read operations of Flash Status register will deliver complementary values. FSB.6 will toggle each time the Flash Status register is read. The Program operation is completed when two successive reads yield the same value. The next read will output the bit last programmed, or a '1' after Erase operation</p> <p>FSB.6 will be set to '1' if a read operation is attempted on an Erase Suspended block. In addition, an Erase Suspend/Resume command will cause FSB.6 to toggle.</p>
FSB.5	<p>Flash Status bit 5: Error Bit</p> <p>This bit is set to '1' when there is a failure of Program, block or chip erase operations. This bit will also be set if a user tries to program a bit to '1' to a Flash location that is currently programmed with '0'.</p> <p>The error bit resets after Read/Reset instruction.</p> <p>In case of success, the Error bit will be set to '0' during Program or Erase and then will output the bit last programmed or a '1' after erasing</p>
FSB.3	<p>Flash Status bit 3: Erase Time-out Bit</p> <p>This bit is cleared by the EPC when the last Block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the time-out period is finished, after 96 μs, FSB.3 returns back to '1'.</p>
FSB.2	<p>Flash Status bit 2: Toggle Bit</p> <p>This toggle bit, together with FSB.6, can be used to determine the chip status during the Erase Mode or Erase Suspend Mode. It can be used also to identify the block being Erased Suspended. A Read operation will cause FSB.2 to Toggle during the Erase Mode. If the Flash is in Erase Suspend Mode, a Read operation from the Erase suspended block or a Program operation into the Erase suspended block will cause FSB.2 to toggle.</p> <p>When the Flash is in Program Mode during Erase Suspend, FSB.2 will be read as '1' if address used is the address of the word being programmed.</p> <p>After Erase completion with an Error status, FSB.2 will toggle when reading the faulty sector.</p>

Note: The Address of Flash Status Register is the address of the word being programmed when Programming operation is in progress, or an address within block being erased when Erasing operation is in progress.

5.3.5 - Flash Protection Register

The Flash Protection register is a non-volatile register that contains the protection status. This register can be read by using the Read Protection Status (RP) command, and programmed by using the dedicated Set Protection command.

Flash Protection Register (PR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP	-	-	-	-	-	-	-	-	BP6*	BP5*	BP4	BP3	BP2	BP1	BP0

*Not available for 128K versions (reserved areas)

BPx	<p>Block x Protection Bit (x = 0...6)</p> <p>'0': the Block Protection is enabled for block x. Programming or erasing the block is not possible, unless a Block Temporary Unprotection command is issued.</p> <p>'1': the Block Protection is disabled for block x.</p> <p>Bit is '1' by default, and can be programmed permanently to '0' using the Set Protection command but then cannot be set to '1' again. It is therefore possible to temporarily disable the Block Protection using the Block Temporary Unprotection instruction.</p>
CP	<p>Code Protection Bit</p> <p>'0': the Flash Code Protection is enabled. Read accesses to the Flash for execution not performed in the Flash itself are not allowed, the returned value will be 009Bh, whatever the content of the Flash is.</p> <p>'1': the Flash Code Protection is disabled: read accesses to the Flash from external or internal RAM are allowed</p> <p>Bit is '1' by default, and can be programmed permanently to '0' using the Set Protection command but then cannot be set to '1' again. It is therefore possible to temporarily disable the Code Protection using the Code Temporary Unprotection instruction.</p>

5.3.6 - Instructions Description

Twelve instructions dedicated to Flash memory accesses are defined as follow:

Read/Reset (RD). The Read/Reset instruction consist of one write cycle with data XXF0h. it can be optionally preceded by two CI enable coded cycles (data xxA8h at address 1554h + data xx54h at address 2AA8h). Any successive read cycle following a Read/Reset instruction will read the memory array. A Wait cycle of 10µs is necessary after a Read/Reset command if the memory was in program or Erase mode.

Program Word (PW). This instruction uses four write cycles. After the two CI enable coded cycles, the Program Word command xxA0h is written at address 1554h. The following write cycle will latch the address and data of the word to be programmed. Memory programming can be done only by writing 0's instead of 1's, otherwise an error occurs. During programming, the Flash

Status is checked by reading the Flash Status bit FSB.2, FSB.5, FSB.6 and FSB.7 which show the status of the EPC. FSB.2, FSB.6 and FSB.7 determine if programming is on going or has completed, and FSB.5 allows a check to be made for any possible error.

Block Erase (BE). This instruction uses a minimum of six command cycles. The erase enable command xx80h is written at address 1554h after the two-cycle CI enable sequence.

The erase confirm code xx30h must be written at an address related to the block to be erased preceded by the execution of a second CI enable sequence. Additional erase confirm codes must be given to erase more than one block in parallel. Additional erase confirm commands must be written within a defined time-out period. The input of a new Block Erase command will restart the time-out period.

When this time-out period has elapsed, the erase starts. The status of the internal timer can be monitored through the level of FSB.3, if FSB.3 is '0', the Block Erase command has been given and

the time-out is running; if FSB.3 is '1', the time-out has expired and the EPC is erasing the block(s).

If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts, and the device is reset to Read Mode. It is not necessary to program the block with 0000h as the EPC will do this automatically before the erasing to FFFFh. Read operations after the EPC has started, output the Flash Status Register.

During the execution of the erase by the EPC, the device accepts only the Erase Suspend and Read/Reset instructions. Data Polling bit FSB.7 returns '0' while the erasure is in progress, and '1' when it has completed. The Toggle bit FSB.2 and FSB.6 toggle during the erase operation. They stop when erase is completed. After completion, the Error bit FSB.5 returns '1' if there has been an erase failure because erasure has not completed even after the maximum number of erase cycles have been executed by the EPC, in this case, it will be necessary to input a Read/Reset to the Command Interface in order to reset the EPC.

Chip Erase (CE). This instruction uses six write cycles. The Erase Enable command xx80h, must be written at address 1554h after CI-Enable cycles. The Chip Erase command xx10h must be given on the sixth cycle after a second CI-Enable sequence. An error in command sequence will reset the CI to Read mode. It is NOT necessary to program the block with 0000h as the EPC will do this automatically before the erasing to FFFFh. Read operations after the EPC has started output the Flash Status Register. During the execution of the erase by the EPC, Data Polling bit FSB.7 returns '0' while the erasure is in progress, and '1' when it has completed. The FSB.2 and FSB.6 bit toggle during the erase operation. They stop when erase is finished. The FSB.5 error bit returns "1" in case of failure of the erase operation. The error flag is set after the maximum number of erase cycles have been executed by the EPC. In this case, it will be necessary to input a Read/Reset to the Command Interface in order to reset the EPC.

Erase Suspend (ES). This instruction can be used to suspend a Block Erase operation by giving the command xxB0h without any specific address. No CI-Enable cycles is required. Erase Suspend operation allows reading of data from another block and/or the programming in another block while erase is in progress. If this command is given during the time-out period, it will terminate the time-out period in addition to erase Suspend. The Toggle bit FSB.6, when monitored at an address that belongs to the block being erased, stops toggling when Erase Suspend Command is effective, It happens between 0.1µs and 15µs

after the Erase Suspend Command has been written. The Flash will then go in normal Read Mode, and read from blocks not being erased is valid, while read from block being erased will output FSB.2 toggling. During a Suspend phase the only instructions valid are Erase Resume and Program Word. A Read / Reset instruction during Erase suspend will definitely abort the Erase and result in invalid data in the block being erased.

Erase Resume (ER). This instruction can be given when the memory is in Erase Suspend State. Erase can be resumed by writing the command xx30h at any address without any CI-enable sequence.

Program during Erase Suspend. The Program Word instruction during Erase Suspend is allowed only on blocks that are not Erase-suspended. This instruction is the same than the Program Word instruction.

Set Protection (SP). This instruction can be used to enable both Block Protection (to protect each block independently from accidental Erasing-Programming Operation) and Code Protection (to avoid code dump). The Set Protection Command must be given after a special CI-Protection Enable cycles (see instruction table). The following Write cycle, will program the Protection Register. To protect the block x (x = 0 to 6), the data bit x must be at '0'. To protect the code, bit 15 of the data must be '0'. Enabling Block or Code Protection is **permanent** and can be cleared only by STM. Block Temporary Unprotection and Code Temporary Unprotection instructions are available to allow the customer to update the code.

Notes: 1. The new value programmed in protection register will only become active after a reset.

2. Bit that are already at '0' in protection register must be confirmed at '0' also in data latched during the 4th cycle of set protection command, otherwise an error may occur.

Read Protection Status (RP). This instruction is used to read the Block Protection status and the Code Protection status. To read the protection register (see Table 3), the CI-Protection Enable cycles must be executed followed by the command xx90h at address x2A54h. The following Read Cycles at any odd word address will output the Block Protection Status. The Read/Reset command xxF0h must be written to reset the protection interface.

Note: After a modification of protection register (using Set Protection command), the Read

Protection Status will return the new PR value only after a reset.

Block Temporary Unprotection (BTU). This Instruction can be used to temporary unprotect all the blocks from Program / Erase protection. The Unprotection is disabled after a Reset cycle. The Block Temporary Unprotection command `xxC1h` must be given to enable Block Temporary Unprotection. The Command must be preceded by the CI-Protection Enable cycles and followed by the Read/Reset command `xxF0h`.

Set Code Protection (SCP). This kind of protection allows the customer to protect the proprietary code written in Flash. If installed and active, Flash Code Protection prevents data operand accesses and program branches into the on-chip Flash area from any location outside the Flash memory itself. Data operand accesses and branches to Flash locations are only and exclusively allowed for instructions executed from the Flash memory itself. Every read or jump to Flash performed from another memory (like internal RAM, external memory) while Code Protection is enabled, will give the opcode `009Bh` related to TRAP #00 illegal instruction. The CI-Protection Enable cycles must be sent to set the Code Protection. By writing data `7FFFh` at any odd word address, the Code Protected status is stored in the Flash Protection Register (PR). Protection is permanent and cannot be cleared by the user. It is possible to temporarily disable the Code Protection using Code Temporary Unprotection instruction.

Note: Bits that are already at '0' in protection register must be confirmed at '0' also in data latched during the 4th cycle of set protection command, otherwise an error may occur.

Code Temporary Unprotection (CTU). This instruction must be used to temporary disable Code Protection. This instruction is effective only if executed from Flash memory space. To restore the protection status, without using a reset, it is necessary to use a Code Temporary Protection instruction. System reset will reset also the Code Temporary Unprotected status. The Code Temporary Unprotection command consists of the following write cycle:

```
MOV  MEM, Rn      ; This instruction MUST be executed from Flash memory space
```

Where MEM is an absolute address inside memory space, Rn is a register loaded with data `0FFFFh`.

Code Temporary Protection (CTP). This instruction allows to restore Code Protection. This operation is effective only if executed from Flash memory and is necessary to restore the protection status after the use of a Code Temporary Unprotection instruction.

The Code Temporary Protection command consists of the following write cycle:

```
MOV  MEM, Rn      ; This instruction MUST be executed from Flash memory space
```

Where MEM is an absolute address inside memory space, Rn is a register loaded with data `0FFFBh`.

Note that Code Temporary Unprotection instruction must be used when it is necessary to modify the Flash with protected code (SCP), since the write/erase routines must be executed from a memory external to Flash space. Usually, the write/erase routines, executed in RAM, ends with a return to Flash space where a CTP instruction restore the protection.

Table 3 : Instructions

Instruction	Mne	Cycle		1 st Cycle	2 nd Cycle	3 rd Cycle	4 th Cycle	5 th Cycle	6 th Cycle	7 th Cycle
Read/Reset	RD	1+	Addr. ¹	X ²	Read Memory Array until a new write cycle is initiated					
			Data	xxF0h						
Read/Reset	RD	3+	Addr. ¹	x1554h	x2AA8h	xxxxxh	Read Memory Array until a new write cycle is initiated			
			Data	xxA8h	xx54h	xxF0h				
Program Word	PW	4	Addr. ¹	x1554h	x2AA8h	x1554h	WA ³	Read Data Polling or Toggle bit until Program completes.		
			Data	xxA8h	xx54h	xxA0h	WD ⁴			
Block Erase	BE	6	Addr. ¹	x1554h	x2AA8h	x1554h	x1554h	x2AA8h	BA	BA' ⁵
			Data	xxA8h	xx54h	xx80h	xxA8h	xx54h	xx30h	xx30h
Chip Erase	CE	6	Addr. ¹	x1554h	x2AA8h	x1554h	x1554h	x2AA8h	x1554h	Note ⁶
			Data	xxA8h	xx54h	xx80h	xxA8h	xx54h	xx10h	
Erase Suspend	ES	1	Addr. ¹	X ²	Read until Toggle stops, then read or program all data needed from block(s) not being erased then Resume Erase.					
			Data	xxB0h						
Erase Resume	ER	1	Addr. ¹	X ²	Read Data Polling or Toggle bit until Erase completes or Erase is suspended another time.					
			Data	xx30h						
Set Block/Code Protection	SP	4	Addr. ¹	x2A54h	x15A8h	x2A54h	Any odd word address ⁹			
			Data	xxA8h	xx54h	xxC0h	WPR ⁷			
Read Protection Status	RP	4	Addr. ¹	x2A54h	x15A8h	x2A54h	Any odd word address ⁹	Read Protection Register until a new write cycle is initiated.		
			Data	xxA8h	xx54h	xx90h	Read PR			
Block Temporary Unprotection	BTU	4	Addr. ¹	x2A54h	x15A8h	x2A54h	X ²			
			Data	xxA8h	xx54h	xxC1h	xxF0h			
Code Temporary Unprotection	CTU	1	Addr. ¹	MEM ⁸	Write cycles must be executed from Flash.					
			Data	FFFFh						
Code Temporary Protection	CTP	1	Addr. ¹	MEM ⁸	Write cycles must be executed from Flash.					
			Data	FFFBh						

Notes 1. Address bit A14, A15 and above are don't care for coded address inputs.

2. X = Don't Care.

3. WA = Write Address: address of memory location to be programmed.

4. WD = Write Data: 16-bit data to be programmed

5. Optional, additional blocks addresses must be entered within a time-out delay (96 μs) after last write entry, time-out status can be verified through FSB.3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended.

6. Read Data Polling or Toggle bit until Erase completes.

7. WPR = Write protection register. To protect code, bit 15 of WPR must be '0'. To protect block N (N=0,1,...), bit N of WPR must be '0'. Bit that are already at '0' in protection register must also be '0' in WPR, else a writing error will occurs (it is not possible to write a '1' in a bit already programmed at '0').