Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

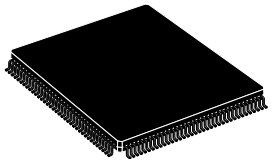
ST10F273M

16-bit MCU with 512 Kbyte Flash memory and 36 Kbyte RAM

Datasheet – production data

Features

- High performance 16-bit CPU with DSP functions
  - 50ns instruction cycle time at 40 MHz max CPU clock
  - Multiply/accumulate unit (MAC) 16 x 16-bit multiplication, 40-bit accumulator
  - Enhanced boolean bit manipulations
  - Single-cycle context switching support
- Memory organization
  - 512 Kbyte on-chip Flash memory single voltage with erase/program controller (full performance, 32-bit fetch)
  - 100 K erasing/programming cycles
  - Up to 16 Mbyte linear address space for code and data (5 Mbytes with CAN or I^2C)
  - 2 Kbyte on-chip internal RAM (IRAM)
  - 34 Kbyte on-chip extension RAM (XRAM)
  - Programmable external bus configuration and characteristics for different address ranges
  - 5 programmable chip-select signals
  - Hold-acknowledge bus arbitration support
- Interrupt
  - 8-channel peripheral event controller for single cycle interrupt driven data transfer
  - 16-priority-level interrupt system with 56 sources, sampling rate down to 25ns
- Timers
  - 2 multifunctional general purpose timer units with 5 timers
- Two 16-channel capture / compare units
- 4-channel PWM unit + 4-channel XPWM



PQFP144 (28 x 28 x 3.4mm) (Plastic Quad Flat Package)
LQFP144 (20 x 20 x 1.4mm) (Low Profile Quad Flat Package)

- 24-channel A/D converter
  - 16-channel 10-bit, accuracy +/-2 LSB
  - 8-channel 10-bit, accuracy +/-5 LSB
  - 4.85µs Minimum conversion time
- Serial channels
  - 2 synch. / asynch. serial channels
  - 2 high-speed synchronous channels
  - I^2C standard interface
- 2 CAN 2.0B interfaces operating on 1 or 2 CAN buses (64 or 2x32 messages, C-CAN version)
- Fail-safe protection
  - Programmable watchdog timer
  - Oscillator watchdog
- On-chip bootstrap loader
- Clock generation
  - On-chip PLL and 4 to 12 MHz oscillator
  - Direct or prescaled clock input
- Real time clock and 32 kHz on-chip oscillator
- Up to 111 general purpose I/O lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Idle, power down and standby modes
- Single voltage supply: 5 V ±10% (embedded regulator for 1.8 V core supply)
- Temperature range: -40°C to 125°C

Contents

List of tables

List of figures

1 Introduction

1.1 Description

The ST10F273M device is a new derivative of the STMicroelectronics® ST10 family of 16-bit single-chip CMOS microcontrollers.

The ST10F273M combines high CPU performance (up to 20 million instructions per second) with high peripheral functionality and enhanced I/O capabilities. It also provides on-chip high-speed single voltage Flash memory, on-chip high-speed RAM, and clock generation via PLL.

The ST10F273M is processed in 0.18mm CMOS technology. The MCU core and the logic is supplied with a 5V to 1.8V on-chip voltage regulator. The part is supplied with a single 5V supply and I/Os work at 5V.

The ST10F273M is an optimized version of the ST10F273E, upward compatible with the following set of differences:

- Maximum CPU frequency is 40 MHz
- A single bank of IFlash has been implemented but the programming interface has been kept compatible with the ST10F273E
- Identification registers: the IDMEM register reflects the Flash type difference and allows to differentiate the two devices by software
- Improved EMC behavior thanks to the introduction of an internal RC filter on the 5V for the ballast transistors
- The clock to the X-Peripherals is gated: X-Peripheral not used will not get the clock in order to reduce the power consumption.

1.2 Special characteristics

1.2.1 X-Peripheral clock gating

This new feature have been implemented on the ST10F273M: once the EINIT instruction has been executed, only the X-Peripherals enabled in the XPERCON register will be clocked.

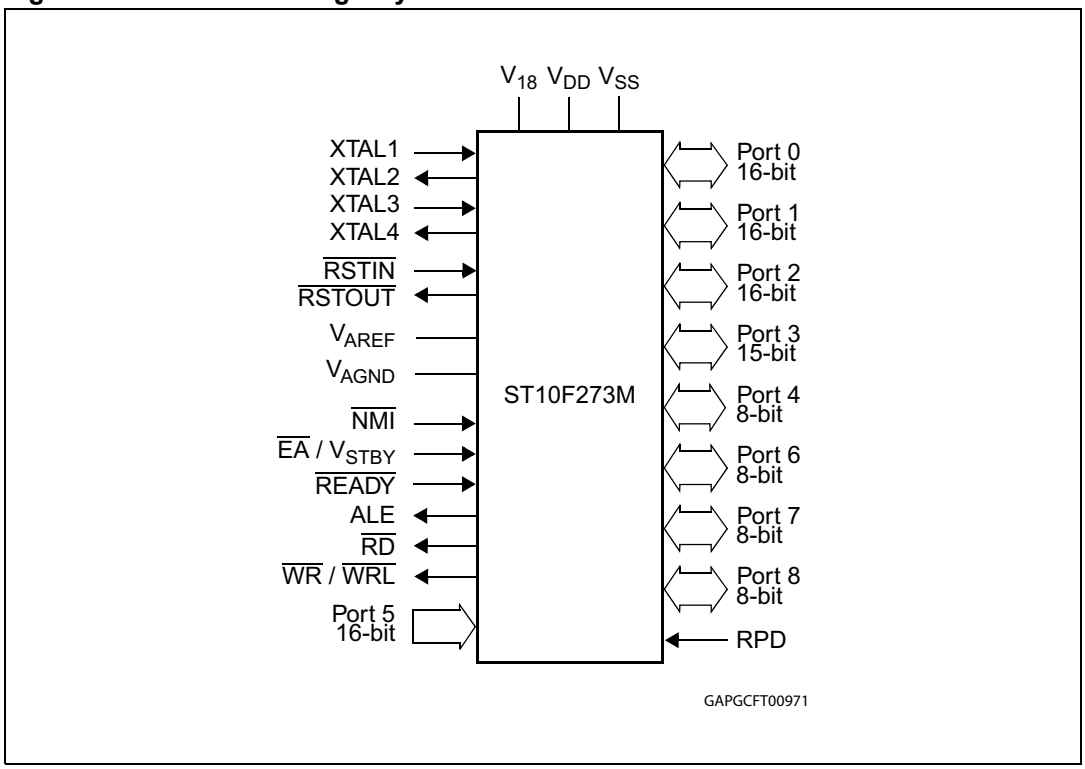
The new feature allows to reduce the power consumption and also should improve the emissions as it avoids to propagate useless clock signals across the device.

1.2.2 Improved supply ring

An RC filter has been introduced in the 5V power supply ring of the ballast transistor. In addition, the supply rings for the internal voltage regulators and the IOs have been split.

These two modifications should improve the behavior of the device regarding conducted emissions.

Figure 1. ST10F273M logic symbol



2 Pin data

Figure 2. Pin configuration (top view)

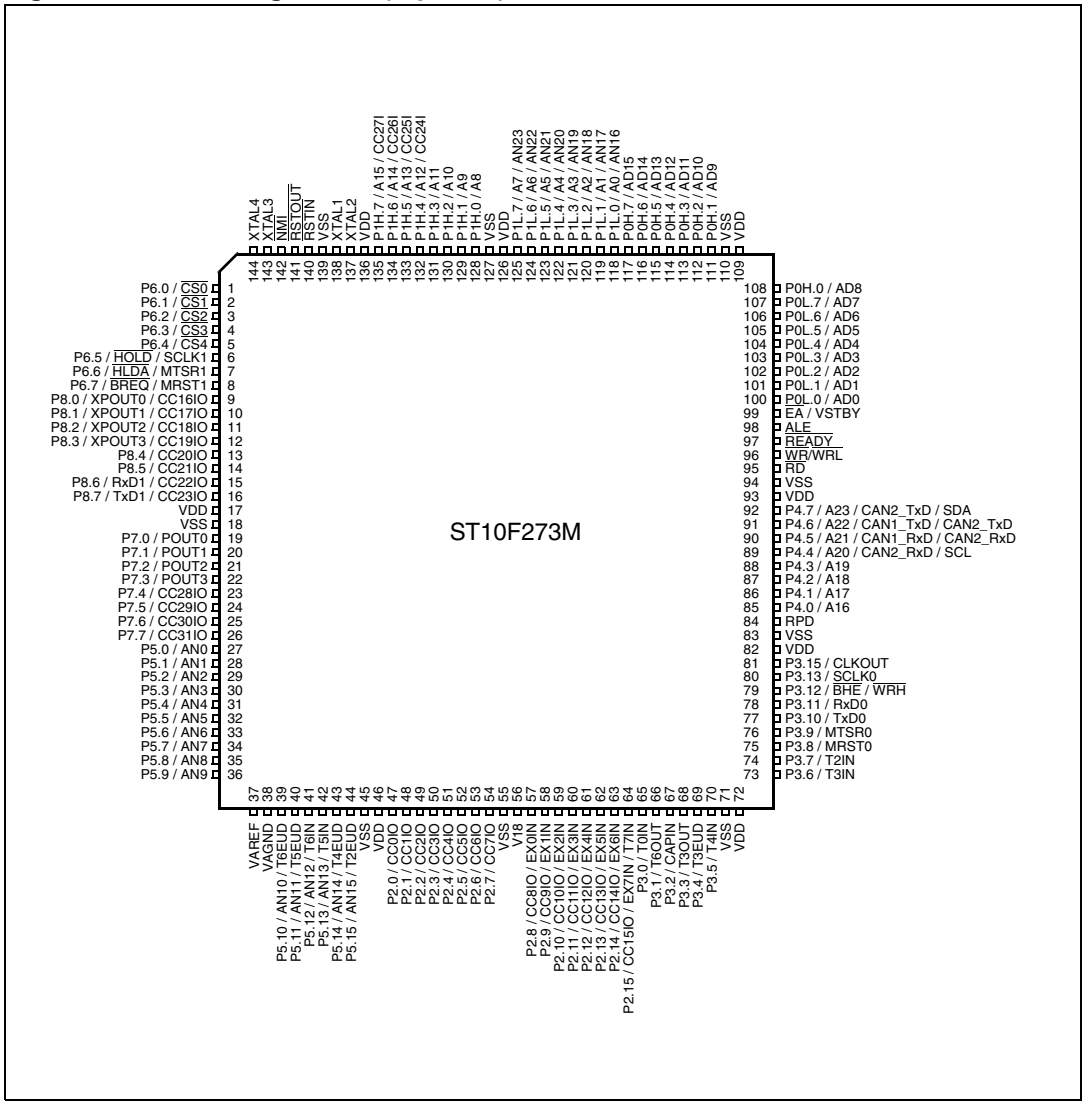


Table 1. Pin description

Symbol	Pin	Type	Function		
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or CMOS). The following Port 6 pins have alternate functions:		
	1	O	P6.0	$\overline{CS0}$	Chip select 0 output
	...	...	...	...	...
	5	O	P6.4	$\overline{CS4}$	Chip select 4 output
	6	I	P6.5	$\overline{HOLD}$	External master hold request input
		I/O		SCLK1	SSC1: master clock output / slave clock input
	7	O	P6.6	$\overline{HLDA}$	Hold acknowledge output
		I/O		MTSR1	SSC1: master-transmitter / slave-receiver O/I
	8	O	P6.7	$\overline{BREQ}$	Bus request output
		I/O		MRST1	SSC1: master-receiver / slave-transmitter I/O
P8.0 - P8.7	9-16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or CMOS). The following Port 8 pins have alternate functions:		
	9	I/O	P8.0	CC16IO	CAPCOM2: CC16 capture input / compare output
		O		XPWM0	PWM1: channel 0 output
	...	...	...	...	...
	12	I/O	P8.3	CC19IO	CAPCOM2: CC19 capture input / compare output
		O		XPWM0	PWM1: channel 3 output
	13	I/O	P8.4	CC20IO	CAPCOM2: CC20 capture input / compare output
	14	I/O	P8.5	CC21IO	CAPCOM2: CC21 capture input / compare output
	15	I/O	P8.6	CC22IO	CAPCOM2: CC22 capture input / compare output
		I/O		RxD1	ASC1: Data input (Asynchronous) or I/O (Synchronous)
	16	I/O	P8.7	CC23IO	CAPCOM2: CC23 capture input / compare output
		O		TxD1	ASC1: Clock / Data output (Asynchronous/Synchronous)

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P7.0 - P7.7	19-26	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 7 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or CMOS). The following Port 7 pins have alternate functions:		
	19	O	P7.0	POUT0	PWM0: channel 0 output
	...	...	...	...	...
	22	O	P7.3	POUT3	PWM0: channel 3 output
	23	I/O	P7.4	CC28IO	CAPCOM2: CC28 capture input / compare output
	...	...	...	...	...
	26	I/O	P7.7	CC31IO	CAPCOM2: CC31 capture input / compare output
P5.0 - P5.9 P5.10 - P5.15	27-36 39-44	I I	16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 can be the analog input channels (up to 16) for the A/D converter, where P5.x equals ANx (Analog input channel x), or they are timer inputs. The input threshold of Port 5 is selectable (TTL or CMOS). The following Port 5 pins have alternate functions:		
	39	I	P5.10	T6EUD	GPT2: timer T6 external up/down control input
	40	I	P5.11	T5EUD	GPT2: timer T5 external up/down control input
	41	I	P5.12	T6IN	GPT2: timer T6 count input
	42	I	P5.13	T5IN	GPT2: timer T5 count input
	43	I	P5.14	T4EUD	GPT1: timer T4 external up/down control input
	44	I	P5.15	T2EUD	GPT1: timer T2 external up/down control input
P2.0 - P2.7 P2.8 - P2.15	47-54 57-64	I/O	16-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 2 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or CMOS). The following Port 2 pins have alternate functions:		
	47	I/O	P2.0	CC0IO	CAPCOM: CC0 capture input/compare output
	...	...	...	...	...
	54	I/O	P2.7	CC7IO	CAPCOM: CC7 capture input/compare output
	57	I/O	P2.8	CC8IO	CAPCOM: CC8 capture input/compare output
		I		EX0IN	Fast external interrupt 0 input
	...	...	...	...	...
	64	I/O	P2.15	CC15IO	CAPCOM: CC15 capture input/compare output
		I		EX7IN	Fast external interrupt 7 input
		I		T7IN	CAPCOM2: timer T7 count input

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P3.0 - P3.5 P3.6 - P3.13, P3.15	65-70, 73-80, 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or CMOS). The following Port 3 pins have alternate functions:		
	65	I	P3.0	T0IN	CAPCOM1: timer T0 count input
	66	O	P3.1	T6OUT	GPT2: timer T6 toggle latch output
	67	I	P3.2	CAPIN	GPT2: register CAPREL capture input
	68	O	P3.3	T3OUT	GPT1: timer T3 toggle latch output
	69	I	P3.4	T3EUD	GPT1: timer T3 external up/down control input
	70	I	P3.5	T4IN	GPT1; timer T4 input for count/gate/reload/capture
	73	I	P3.6	T3IN	GPT1: timer T3 count/gate input
	74	I	P3.7	T2IN	GPT1: timer T2 input for count/gate/reload / capture
	75	I/O	P3.8	MRST0	SSC0: master-receiver/slave-transmitter I/O
	76	I/O	P3.9	MTSR0	SSC0: master-transmitter/slave-receiver O/I
	77	O	P3.10	TxD0	ASC0: clock / data output (asynchronous/synchronous)
	78	I/O	P3.11	RxD0	ASC0: data input (asynchronous) or I/O (synchronous)
	79	O	P3.12	$\overline{BHE}$	External memory high byte enable signal
				$\overline{WRH}$	External memory high byte write strobe
	80	I/O	P3.13	SCLK0	SSC0: master clock output / slave clock input
	81	O	P3.15	CLKOUT	System clock output (programmable divider on CPU clock)

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P4.0 –P4.7	85-92	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold is selectable (TTL or CMOS). Port 4.4, 4.5, 4.6 and 4.7 outputs can be configured as push-pull or open drain drivers. In case of an external bus configuration, Port 4 can be used to output the segment address lines:		
	85	O	P4.0	A16	Segment address line
	86	O	P4.1	A17	Segment address line
	87	O	P4.2	A18	Segment address line
	88	O	P4.3	A19	Segment address line
	89	O	P4.4	A20	Segment address line
		I		CAN2_RxD	CAN2: receive data input
		I/O		SCL	I^2C Interface: serial clock
	90	O	P4.5	A21	Segment address line
		I		CAN1_RxD	CAN1: receive data input
		I		CAN2_RxD	CAN2: receive data input
	91	O	P4.6	A22	Segment address line
		O		CAN1_TxD	CAN1: transmit data output
		O		CAN2_TxD	CAN2: transmit data output
	92	O	P4.7	A23	Most significant segment address line
		O		CAN2_TxD	CAN2: transmit data output
		I/O		SDA	I^2C Interface: serial data
$\overline{RD}$	95	O	External memory read strobe. $\overline{RD}$ is activated for every external instruction or data read access.		
$\overline{WR}/\overline{WRL}$	96	O	External memory write strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$ mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection.		
READY/ $\overline{READY}$	97	I	Ready input. The active level is programmable. When the ready function is enabled, the selected inactive level at this pin, during an external memory access, will force the insertion of waitstate cycles until the pin returns to the selected active level.		
ALE	98	O	Address latch enable output. In case of use of external addressing or of multiplexed mode, this signal is the latch command of the address lines.		

Table 1. Pin description (continued)

Symbol	Pin	Type	Function
$\overline{EA}$ / V_{STBY}	99	I	External access enable pin. A low level applied to this pin during and after Reset forces the ST10F273M to start the program from the external memory space. A high level forces ST10F273M to start in the internal memory space. This pin is also used (when Standby mode is entered, that is ST10F273M under reset and main V_{DD} turned off) to bias the 32 kHz oscillator amplifier circuit and to provide a reference voltage for the low-power embedded voltage regulator which generates the internal 1.8V supply for the RTC module (when not disabled) and to retain data inside the Standby portion of the XRAM (16 Kbyte). It can range from 4.5 to 5.5V (6V for a reduced amount of time during the device life, 4.0V when RTC and 32 kHz on-chip oscillator amplifier are turned off). In running mode, this pin can be tied low during reset without affecting 32 kHz oscillator, RTC and XRAM activities, since the presence of a stable V_{DD} guarantees the proper biasing of all those modules.
P0L.0 -P0L.7, P0H.0 P0H.1 - P0H.7	100-107, 108, 111-117	I/O	Two 8-bit bidirectional I/O ports P0L and P0H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold of Port 0 is selectable (TTL or CMOS). In case of an external bus configuration, PORT0 serves as the address (A) and as the address / data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. Demultiplexed bus modes Data path width: 8-bit / 16-bit P0L.0 – P0L.7: D0 – D7 / D0 - D7 P0H.0 – P0H.7: I/O / D8 - D15 Multiplexed bus modes Data path width: 8-bit / 16-bit P0L.0 – P0L.7: AD0 – AD7 / AD0 - AD7 P0H.0 – P0H.7: A8 – A15 / AD8 - AD15
P1L.0 - P1L.7 P1H.0 - P1H.7	118-125 128-135	I/O	Two 8-bit bidirectional I/O ports P1L and P1H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes: if at least BUSCONx is configured such the demultiplexed mode is selected, the pis of PORT1 are not available for general purpose I/O function. The input threshold of Port 1 is selectable (TTL or CMOS). The pins of P1L also serve as the additional (up to 8) analog input channels for the A/D converter, where P1L.x equals ANy (Analog input channel y, where y = x + 16). This additional function have higher priority on demultiplexed bus function. The following PORT1 pins have alternate functions:
	132	I	P1H.4 / CC24IO / CAPCOM2: CC24 capture input
	133	I	P1H.5 / CC25IO / CAPCOM2: CC25 capture input
	134	I	P1H.6 / CC26IO / CAPCOM2: CC26 capture input
	135	I	P1H.7 / CC27IO / CAPCOM2: CC27 capture input

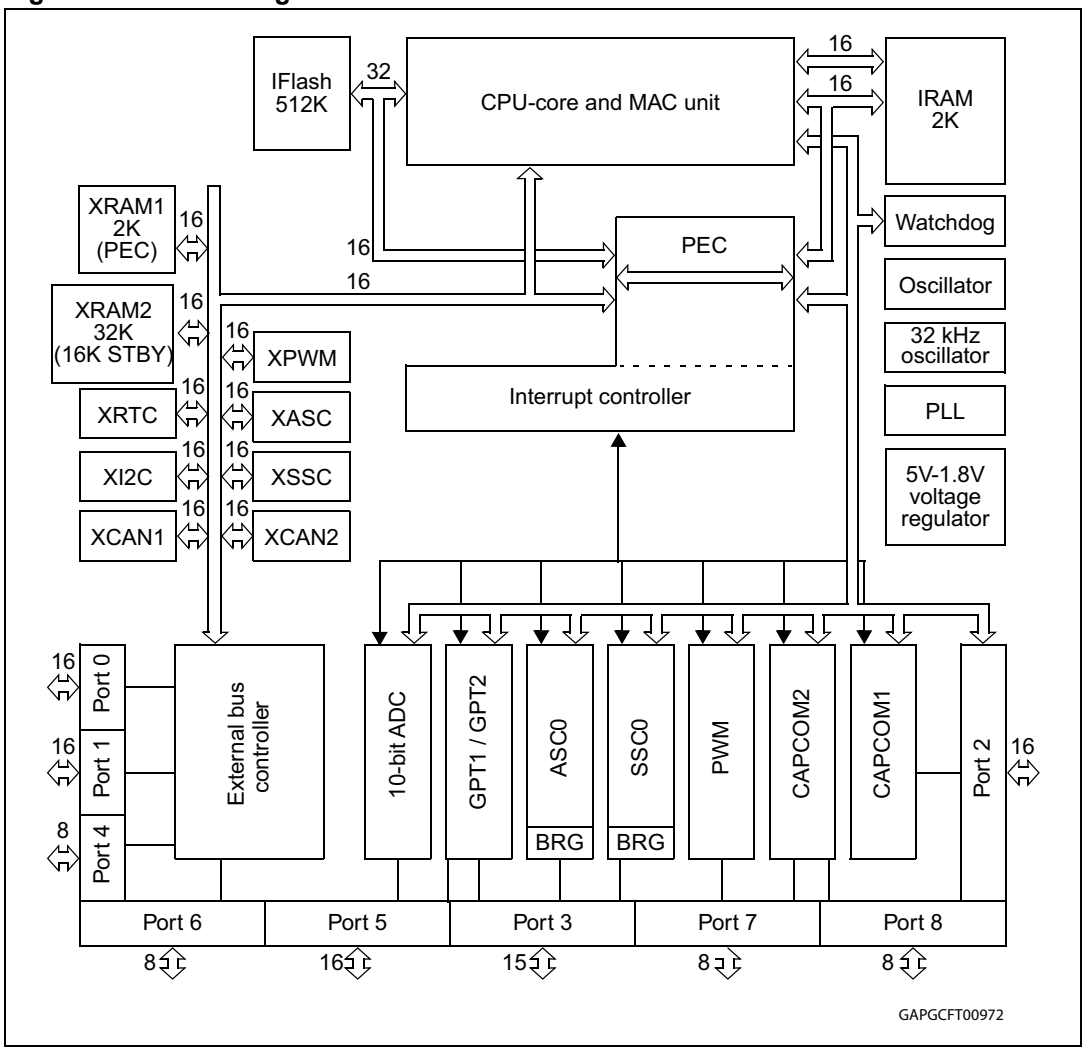
Table 1. Pin description (continued)

Symbol	Pin	Type	Function	
XTAL1	138	I	XTAL1	Main oscillator amplifier circuit and/or external clock input.
XTAL2	137	O	XTAL2	Main oscillator amplifier circuit output.
			To clock the device from an external source, drive XTAL1 while leaving XTAL2 unconnected. Minimum and maximum high / low and rise / fall times specified in the AC Characteristics must be observed.	
XTAL3	143	I	XTAL3	32 kHz oscillator amplifier circuit input
XTAL4	144	O	XTAL4	32 kHz oscillator amplifier circuit output
			When 32 kHz oscillator amplifier is not used, to avoid spurious consumption, XTAL3 shall be tied to ground while XTAL4 shall be left open. Besides, bit OFF32 in RTCCON register shall be set. 32 kHz oscillator can only be driven by an external crystal, and not by a different clock source.	
$\overline{\text{RSTIN}}$	140	I	Reset Input with CMOS Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10F273M. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. In bidirectional reset mode (enabled by setting bit BDRSTEN in SYSCON register), the $\overline{\text{RSTIN}}$ line is pulled low for the duration of the internal reset sequence.	
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is driven to a low level during hardware, software or watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.	
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10F273M to go into power down mode. If $\overline{\text{NMI}}$ is high and PWDCFG = '0', when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.	
V_{AREF}	37	-	A/D converter reference voltage and analog supply	
V_{AGND}	38	-	A/D converter reference and analog ground	
RPD	84	-	Timing pin for the return from interruptible power down mode and synchronous / asynchronous reset selection.	
V_{DD}	17, 46, 72,82,93, 109, 126, 136	-	Digital supply voltage = + 5V during normal operation, idle and power down modes. It can be turned off when Standby RAM mode is selected.	
V_{SS}	18,45, 55,71, 83,94, 110, 127, 139	-	Digital ground	
V_{18}	56	-	1.8V decoupling pin: a decoupling capacitor (typical value of 10nF, max 100nF) must be connected between this pin and nearest V_{SS} pin.	

3 Functional description

The architecture of the ST10F273M combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F273M.

Figure 3. Block diagram



4 Memory organization

The memory space of the ST10F273M is configured in a unified memory architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16 Mbytes. The entire memory space can be accessed Bytewise or Wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

IFlash: 512 Kbytes of on-chip Flash memory implemented as a unique Bank (Bank0). Bank0 is divided in 12 blocks (B0F0...B0F11).

Note: Read-while-write operations are not allowed: Write commands must be executed from a non IFlash memory area (on-chip RAM or external memory).

When Bootstrap mode is selected, the Test-Flash Block B0TF (4 Kbytes) appears at address 00'0000h: Refer to the device User Manual for more details on the memory mapping in Bootstrap mode. The summary of address range for IFlash is the following:

Table 2. Summary of IFlash address range

Blocks	User mode	Size (bytes)
B0TF	Not visible	4 K
B0F0	00'0000h - 00'1FFFh	8 K
B0F1	00'2000h - 00'3FFFh	8 K
B0F2	00'4000h - 00'5FFFh	8 K
B0F3	00'6000h - 00'7FFFh	8 K
B0F4	01'8000h - 01'FFFFh	32 K
B0F5	02'0000h - 02'FFFFh	64 K
B0F6	03'0000h - 03'FFFFh	64 K
B0F7	04'0000h - 04'FFFFh	64 K
B0F8	05'0000h - 05'FFFFh	64 K
B0F9	06'0000h - 06'FFFFh	64 K
B1F0 / B0F10 (1)	07'0000h - 07'FFFFh	64 K
B1F1 / B0F11 (1)	08'0000h - 08'FFFFh	64 K

Note: A single Flash bank is implemented on the ST10F273M compared to the ST10F273E. The last two sectors (B0F10 and B0F11) can be seen as the Bank1 of the ST10F273E in order to maintain the compatibility with the existing Flash programming drivers. For this, the control and status bit of the blocks B0F10 and B0F11 have been duplicated to be usable as blocks B1F0 and B1F1 of the ST10F273E.

XFLASH / Flash Control Registers: Address range 0E'0000h-0E'FFFFh is reserved for the Flash Control Register and other internal service memory space used by the Flash Program/Erase Controller. XFLASHEN bit in XPERCON register must be set to access the Flash Control Register. Note that when Flash Control Registers are not accessible, no program/erase operations are possible. The Flash Control Registers are accessed in 16-bit demultiplexed bus-mode without read/write delay. Byte and word accesses are allowed.

IRAM: 2 Kbytes of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. A register bank is 16 Wordwide (R0 to R15) and / or Bytewide (RL0, RH0, …, RL7, RH7) general purpose registers group.

XRAM: 34 Kbytes of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.
The XRAM is divided into two areas, the first 2 Kbytes named XRAM1 and the second 32 Kbytes named XRAM2, connected to the internal XBUS and are accessed like an external memory in 16-bit demultiplexed bus-mode without wait state or read/write delay (50ns access at 40 MHz CPU clock). Byte and Word accesses are allowed.

The XRAM1 address range is 00'E000h - 00'E7FFh if XPEN (bit 2 of SYSCON register), and XRAM1EN (bit 2 of XPERCON register) are set.
If XRAM1EN or XPEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

The XRAM2 address range is F'0000h - F'7FFFFh if XPEN (bit 2 of SYSCON register), and XRAM2EN (bit 3 of XPERCON register) are set.
If bit XPEN is cleared, then any access in the address range programmed for XRAM2 will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

The 16 kbytes lower portion of the XRAM2 (address range F'0000h - F'3FFFFh) represents also the Standby RAM, which can be maintained biased through $\overline{EA}$ / V_{STBY} pin when the main supply V_{DD} is turned off.
As the XRAM appears like external memory, it cannot be used as system stack or as register banks. The XRAM is not provided for single bit storage and therefore is not bit addressable.

SFR/ESFR: 1024 bytes (2 x 512 bytes) of address space is reserved for the special function register (SFR) areas. SFRs are Wordwide registers which are used to control and to monitor the function of the different on-chip units.

CAN1: Address range 00'EF00h - 00'EFFFh is reserved for the CAN1 Module access. The CAN1 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN1EN bit 0 of the XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two wait states give an access time of 100ns at 40 MHz CPU clock. No tri-state wait states are used.

CAN2: Address range 00'EE00h - 00'EEFFh is reserved for the CAN2 Module access. The CAN2 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN2EN bit 1 of the new XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two wait states give an access time of 100ns at 40 MHz CPU clock. No tri-state wait states are used.

Note: If one or the two CAN modules are used, Port 4 cannot be programmed to output all eight segment address lines. Thus, only four segment address lines can be used, reducing the external memory space to 5 Mbytes (1 Mbyte per CS line).

RTC: Address range 00'ED00h - 00'EDFFh is reserved for the RTC Module access. The RTC is enabled by setting XPEN bit 2 of the SYSCON register and bit 4 of the XPERCON register. Accesses to the RTC Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

PWM1: Address range 00'EC00h - 00'ECFFh is reserved for the PWM1 Module access. The PWM1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 6 of the XPERCON register. Accesses to the PWM1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used. Only word access is allowed.

ASC1: Address range 00'E900h - 00'E9FFh is reserved for the ASC1 Module access. The ASC1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 7 of the XPERCON register. Accesses to the ASC1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

SSC1: Address range 00'E800h - 00'E8FFh is reserved for the SSC1 Module access. The SSC1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 8 of the XPERCON register. Accesses to the SSC1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

I2C: Address range 00'EA00h - 00'EAFFh is reserved for the I2C Module access. The I2C is enabled by setting XPEN bit 2 of the SYSCON register and bit 9 of the XPERCON register. Accesses to the I2C Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

X-Miscellaneous: Address range 00'EB00h - 00'EBFFh is reserved for the access to a set of XBUS additional features. They are enabled by setting XPEN bit 2 of the SYSCON register and bit 10 of the XPERCON register. Accesses to this additional features use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used. The following set of features are provided:

- CLKOUT programmable divider
- XBUS interrupt management registers
- ADC multiplexing on P1L register
- Port1L digital disable register for extra ADC channels
- CAN2 multiplexing on P4.5/P4.6
- CAN1-2 main clock prescaler
- Main Voltage Regulator disable for power-down mode
- TTL / CMOS threshold selection for Port0, Port1 and Port5

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 Mbytes of external memory can be connected to the microcontroller.

Visibility of XBUS peripherals

In order to keep the ST10F273M compatible with the ST10F168 / ST10F269, the XBUS peripherals can be selected to be visible on the external address / data bus. Different bits for X-Peripheral enabling in XPERCON register must be set. If these bits are cleared before the global enabling with XPEN bit in SYSCON register, the corresponding address space, port pins and interrupts are not occupied by the peripherals, thus the peripheral is not visible and not available. Refer to *Chapter 23: Register set on page 115*.

XPERCON and X-Peripheral clock gating

As already mentioned, the XPERCON register must be programmed to enable the single XBus modules separately. The XPERCON is a read/write ESFR register.

The new feature of Clock Gating has been implemented by means of this register: Once the EINIT instruction has been executed, all the peripherals (except RAMs and XMISC) not enabled in the XPERCON register are not be clocked. The clock gating can reduce power consumption and improve EMI when the user does not use all X-Peripherals.

Note: When the clock has been gated in the disabled peripherals, no Reset will be raised once the EINIT instruction has been executed.

Figure 4. ST10F273M memory mapping (XADRS3 = 800Bh - reset value)