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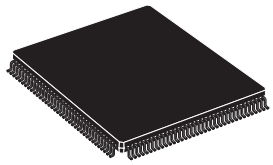
ST10F276E

16-bit MCU with MAC unit
832 Kbyte Flash memory and 68 Kbyte RAM

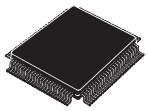
Datasheet – production data

Features

- Highly performance 16-bit CPU with DSP functions
  - 31.25ns instruction cycle time at 64MHz max CPU clock
  - Multiply/accumulate unit (MAC) 16 x 16-bit multiplication, 40-bit accumulator
  - Enhanced boolean bit manipulations
  - Single-cycle context switching support
- On-chip memories
  - 512 Kbyte Flash memory (32-bit fetch)
  - 320 Kbyte extension Flash memory (16-bit fetch)
  - Single voltage Flash memories with erase/program controller and 100K erasing/programming cycles
  - Up to 16 Mbyte linear address space for code and data (5 Mbytes with CAN or I^2C)
  - 2 Kbyte internal RAM (IRAM)
  - 66 Kbyte extension RAM (XRAM)
- External bus
  - Programmable external bus configuration & characteristics for different address ranges
  - 5 programmable chip-select signals
  - Hold-acknowledge bus arbitration support
- Interrupt
  - 8-channel peripheral event controller for single cycle interrupt driven data transfer
  - 16-priority-level interrupt system with 56 sources, sampling rate down to 15.6ns
- Timers
  - 2 multi-functional general purpose timer units with 5 timers
- Two 16-channel capture / compare units



PQFP144 (28 x 28 x 3.4mm)
(Plastic quad flat package)



LQFP144 (20 x 20 x 1.4mm)
(Low profile plastic quad flat package)

- 4-channel PWM unit + 4-channel XPWM
- A/D converter
  - 24-channel 10-bit
  - 3 µs minimum conversion time
- Serial channels
  - 2 synch. / asynch. serial channels
  - 2 high-speed synchronous channels
  - 1 I^2C standard interface
- 2 CAN 2.0B interfaces operating on 1 or 2 CAN busses (64 or 2x32 message, C-CAN version)
- Fail-safe protection
  - Programmable watchdog timer
  - Oscillator watchdog
- On-chip bootstrap loader
- Clock generation
  - On-chip PLL with 4 to 12 MHz oscillator
  - Direct or prescaled clock input
- Real-time clock and 32 kHz on-chip oscillator
- Up to 111 general purpose I/O lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Idle, power down and stand-by modes
- Single voltage supply: 5V ±10% (embedded regulator for 1.8 V core supply)

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1 Introduction

The ST10F276E is a derivative of the STMicroelectronics® ST10 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 32 million instructions per second) with high peripheral functionality and enhanced I/O-capabilities. It also provides on-chip high-speed single voltage Flash memory, on-chip high-speed RAM, and clock generation via PLL.

ST10F276E is processed in 0.18 µm CMOS technology. The MCU core and the logic is supplied with a 5V to 1.8V on-chip voltage regulator. The part is supplied with a single 5V supply and I/Os work at 5V.

The device is upward compatible with the ST10F269 device, with the following set of differences:

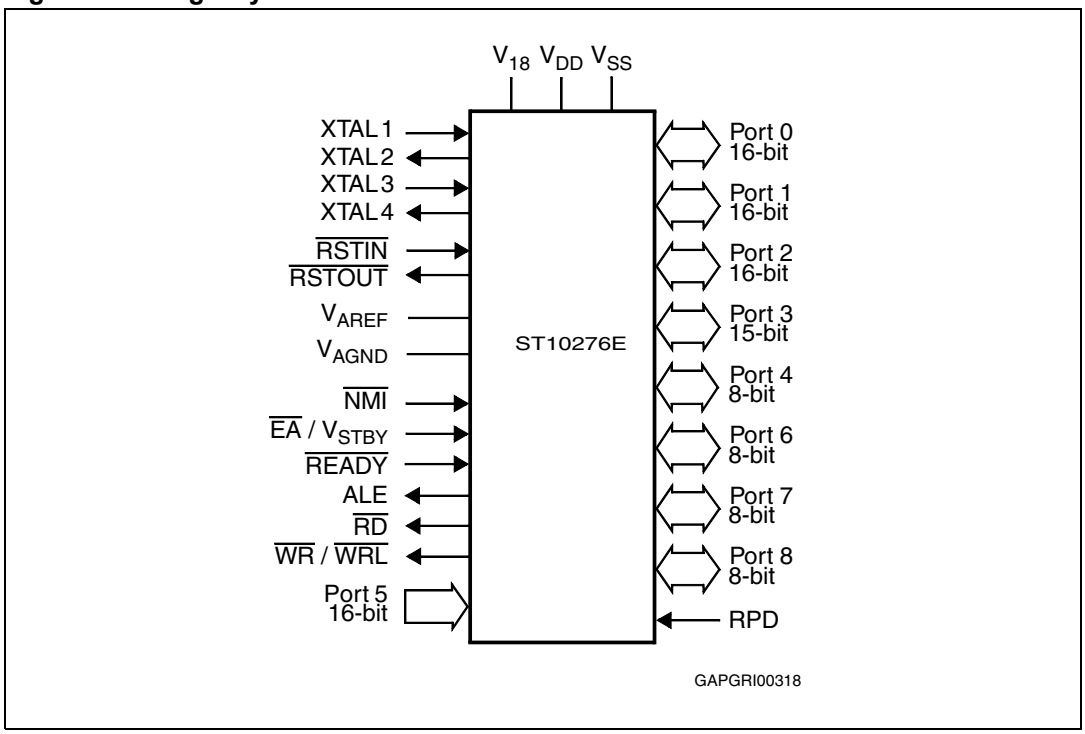
- Flash control interface is now based on STMicroelectronics third generation of stand-alone Flash memories (M29F400 series), with an embedded Program/Erase Controller. This completely frees up the CPU during programming or erasing the Flash.
- Only one supply pin (ex DC1 in ST10F269, renamed into V_{18}) on the QFP144 package is used for decoupling the internally generated 1.8V core logic supply. Do not connect this pin to 5.0V external supply. Instead, this pin should be connected to a decoupling capacitor (ceramic type, typical value 10nF, maximum value 100nF).
- The AC and DC parameters are modified due to a difference in the maximum CPU frequency.
- A new V_{DD} pin replaces DC2 of ST10F269.
- $\overline{EA}$ pin assumes a new alternate functionality: it is also used to provide a dedicated power supply (see V_{STBY}) to maintain biased a portion of the XRAM (16 Kbytes) when the main Power Supply of the device (V_{DD} and consequently the internally generated V_{18}) is turned off for low power mode, allowing data retention. V_{STBY} voltage shall be in the range 4.5-5.5 Volt, and a dedicated embedded low power voltage regulator is in charge to provide the 1.8V for the RAM, the low-voltage section of the 32 kHz oscillator and the Real-Time Clock module when not disabled. It is allowed to exceed the upper limit up to 6V for a very short period of time during the global life of the device, and exceed the lower limit down to 4V when RTC and 32kHz on-chip oscillator are not used.
- A second SSC mapped on the XBUS is added (SSC of ST10F269 becomes here SSC0, while the new one is referred as XSSC or simply SSC1). Note that some restrictions and functional differences due to the XBUS peculiarities are present between the classic SSC, and the new XSSC.
- A second ASC mapped on the XBUS is added (ASC0 of ST10F269 remains ASC0, while the new one is referred as XASC or simply as ASC1). Note that some restrictions and functional differences due to the XBUS peculiarities are present between the classic ASC, and the new XASC.
- A second PWM mapped on the XBUS is added (PWM of ST10F269 becomes here PWM0, while the new one is referred as XPWM or simply as PWM1). Note that some restrictions and functional differences due to the XBUS peculiarities are present between the classic PWM, and the new XPWM.
- An I^2C interface on the XBUS is added (see X-I^2C or simply I^2C interface).
- CLKOUT function can output either the CPU clock (like in ST10F269) or a software programmable prescaled value of the CPU clock.

- Embedded memory size has been significantly increased (both Flash and RAM).
- PLL multiplication factors have been adapted to new frequency range.

  A/D Converter is not fully compatible versus ST10F269 (timing and programming model). Formula for the conversion time is still valid, while the sampling phase programming model is different.

  Besides, additional 8 channels are available on P1L pins as alternate function: the accuracy reachable with these extra channels is reduced with respect to the standard Port5 channels.
- External Memory bus potential limitations on maximum speed and maximum capacitance load could be introduced (under evaluation): ST10F276E will probably not be able to address an external memory at 64MHz with 0 wait states (under evaluation).
- XPERCON register bit mapping modified according to new peripherals implementation (not fully compatible with ST10F269).
- Bondout chip for emulation (ST10R201) cannot achieve more than 50MHz at room temperature (so no real-time emulation possible at maximum speed).
- Input section characteristics are different. The threshold programmability is extended to all port pins (additional XPICON register); it is possible to select standard TTL (with up to 500mV of hysteresis) and standard CMOS (with up to 800mV of hysteresis).
- Output transition is not programmable.
- CAN module is enhanced: ST10F276E implements two C-CAN modules, so the programming model is slightly different. Besides, the possibility to map in parallel the two CAN modules is added (on P4.5/P4.6).
- On-chip main oscillator input frequency range has been reshaped, reducing it from 1-25MHz down to 4-12MHz. This is a high performance oscillator amplifier, providing a very high negative resistance and wide oscillation amplitude: when this on-chip amplifier is used as reference for Real-Time Clock module, the Power-down consumption is dominated by the consumption of the oscillator amplifier itself. A metal option is added to offer a low power oscillator amplifier working in the range of 4-8MHz: this will allow a power consumption reduction when Real-Time Clock is running in Power Down mode using as reference the on-chip main oscillator clock.
- A second on-chip oscillator amplifier circuit (32kHz) is implemented for low power modes: it can be used to provide the reference to the Real-Time Clock counter (either in Power Down or Stand-by mode). Pin XTAL3 and XTAL4 replace a couple of V_{DD}/V_{SS} pins of ST10F269.
- Possibility to re-program internal XBUS chip select window characteristics (XRAM2 and XFLASH address window) is added.

Figure 1. Logic symbol



2 Pin data

Figure 2. Pin configuration (top view)

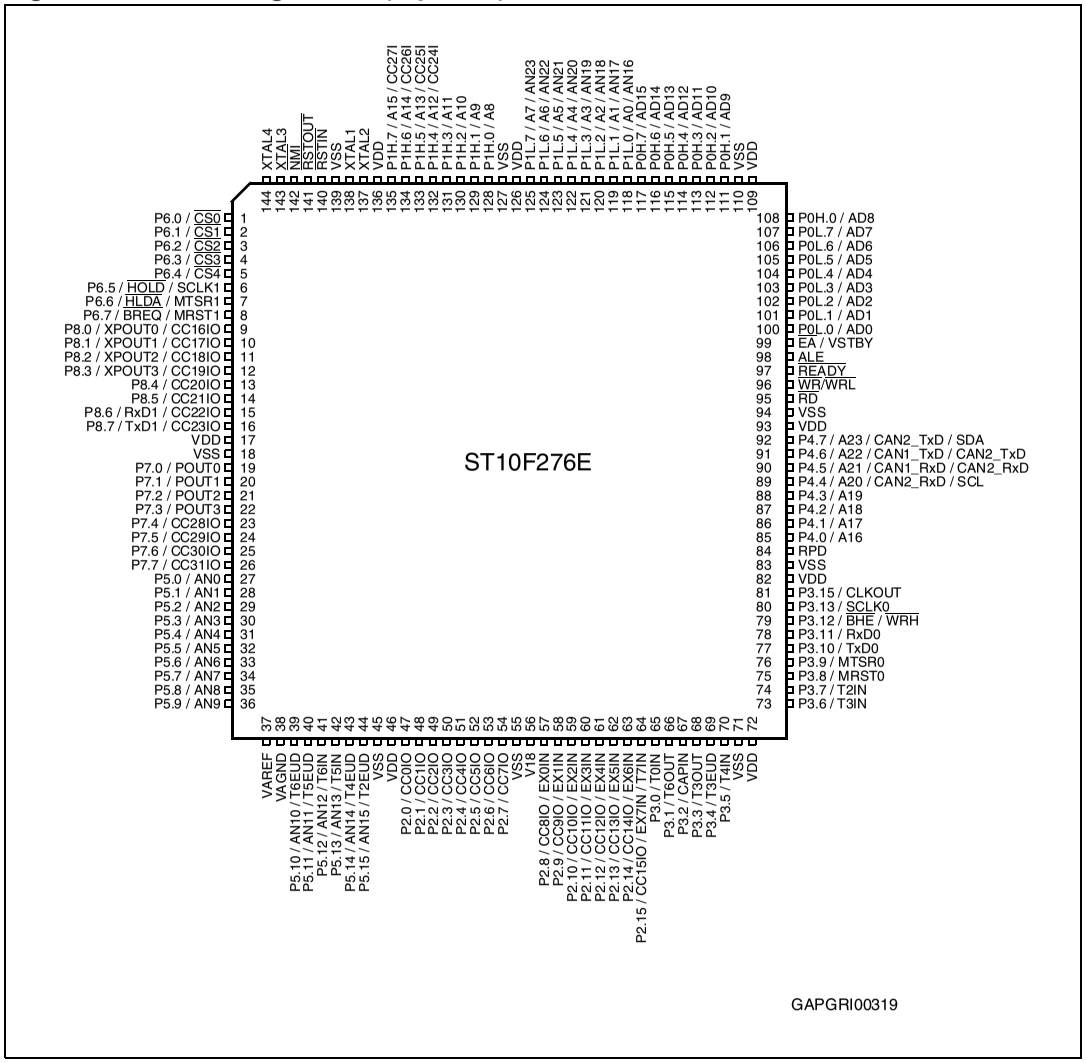


Table 1. Pin description

Symbol	Pin	Type	Function		
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or CMOS). The following Port 6 pins have alternate functions:		
	1	O	P6.0	$\overline{CS0}$	Chip select 0 output
	...	...	...	...	...
	5	O	P6.4	$\overline{CS4}$	Chip select 4 output
	6	I	P6.5	$\overline{HOLD}$	External master hold request input
		I/O		SCLK1	SSC1: master clock output / slave clock input
	7	O	P6.6	$\overline{HLDA}$	Hold acknowledge output
		I/O		MTSR1	SSC1: master-transmitter / slave-receiver O/I
	8	O	P6.7	$\overline{BREQ}$	Bus request output
		I/O		MRST1	SSC1: master-receiver / slave-transmitter I/O
P8.0 - P8.7	9-16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or CMOS). The following Port 8 pins have alternate functions:		
	9	I/O	P8.0	CC16IO	CAPCOM2: CC16 capture input / compare output
		O		XPWM0	PWM1: channel 0 output
	...	...	...	...	...
	12	I/O	P8.3	CC19IO	CAPCOM2: CC19 capture input / compare output
		O		XPWM0	PWM1: channel 3 output
	13	I/O	P8.4	CC20IO	CAPCOM2: CC20 capture input / compare output
	14	I/O	P8.5	CC21IO	CAPCOM2: CC21 capture input / compare output
	15	I/O	P8.6	CC22IO	CAPCOM2: CC22 capture input / compare output
		I/O		RxD1	ASC1: Data input (Asynchronous) or I/O (Synchronous)
	16	I/O	P8.7	CC23IO	CAPCOM2: CC23 capture input / compare output
		O		TxD1	ASC1: Clock / Data output (Asynchronous/Synchronous)

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P7.0 - P7.7	19-26	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 7 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or CMOS). The following Port 7 pins have alternate functions:		
	19	O	P7.0	POUT0	PWM0: channel 0 output
	...	...	...	...	...
	22	O	P7.3	POUT3	PWM0: channel 3 output
	23	I/O	P7.4	CC28IO	CAPCOM2: CC28 capture input / compare output
	...	...	...	...	...
	26	I/O	P7.7	CC31IO	CAPCOM2: CC31 capture input / compare output
P5.0 - P5.9 P5.10 - P5.15	27-36 39-44	I I	16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 can be the analog input channels (up to 16) for the A/D converter, where P5.x equals ANx (Analog input channel x), or they are timer inputs. The input threshold of Port 5 is selectable (TTL or CMOS). The following Port 5 pins have alternate functions:		
	39	I	P5.10	T6EUD	GPT2: timer T6 external up/down control input
	40	I	P5.11	T5EUD	GPT2: timer T5 external up/down control input
	41	I	P5.12	T6IN	GPT2: timer T6 count input
	42	I	P5.13	T5IN	GPT2: timer T5 count input
	43	I	P5.14	T4EUD	GPT1: timer T4 external up/down control input
	44	I	P5.15	T2EUD	GPT1: timer T2 external up/down control input
P2.0 - P2.7 P2.8 - P2.15	47-54 57-64	I/O	16-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 2 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or CMOS). The following Port 2 pins have alternate functions:		
	47	I/O	P2.0	CC0IO	CAPCOM: CC0 capture input/compare output
	...	...	...	...	...
	54	I/O	P2.7	CC7IO	CAPCOM: CC7 capture input/compare output
	57	I/O	P2.8	CC8IO	CAPCOM: CC8 capture input/compare output
		I		EX0IN	Fast external interrupt 0 input
	...	...	...	...	...
	64	I/O	P2.15	CC15IO	CAPCOM: CC15 capture input/compare output
		I		EX7IN	Fast external interrupt 7 input
		I		T7IN	CAPCOM2: timer T7 count input

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P3.0 - P3.5 P3.6 - P3.13, P3.15	65-70, 73-80, 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or CMOS). The following Port 3 pins have alternate functions:		
	65	I	P3.0	T0IN	CAPCOM1: timer T0 count input
	66	O	P3.1	T6OUT	GPT2: timer T6 toggle latch output
	67	I	P3.2	CAPIN	GPT2: register CAPREL capture input
	68	O	P3.3	T3OUT	GPT1: timer T3 toggle latch output
	69	I	P3.4	T3EUD	GPT1: timer T3 external up/down control input
	70	I	P3.5	T4IN	GPT1; timer T4 input for count/gate/reload/capture
	73	I	P3.6	T3IN	GPT1: timer T3 count/gate input
	74	I	P3.7	T2IN	GPT1: timer T2 input for count/gate/reload / capture
	75	I/O	P3.8	MRST0	SSC0: master-receiver/slave-transmitter I/O
	76	I/O	P3.9	MTSR0	SSC0: master-transmitter/slave-receiver O/I
	77	O	P3.10	TxD0	ASC0: clock / data output (asynchronous/synchronous)
	78	I/O	P3.11	RxD0	ASC0: data input (asynchronous) or I/O (synchronous)
	79	O	P3.12	$\overline{\text{BHE}}$	External memory high byte enable signal
				$\overline{\text{WRH}}$	External memory high byte write strobe
	80	I/O	P3.13	SCLK0	SSC0: master clock output / slave clock input
	81	O	P3.15	CLKOUT	System clock output (programmable divider on CPU clock)

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P4.0 –P4.7	85-92	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold is selectable (TTL or CMOS). Port 4.4, 4.5, 4.6 and 4.7 outputs can be configured as push-pull or open drain drivers. In case of an external bus configuration, Port 4 can be used to output the segment address lines:		
	85	O	P4.0	A16	Segment address line
	86	O	P4.1	A17	Segment address line
	87	O	P4.2	A18	Segment address line
	88	O	P4.3	A19	Segment address line
	89	O	P4.4	A20	Segment address line
		I		CAN2_RxD	CAN2: receive data input
		I/O		SCL	I^2C Interface: serial clock
	90	O	P4.5	A21	Segment address line
		I		CAN1_RxD	CAN1: receive data input
		I		CAN2_RxD	CAN2: receive data input
	91	O	P4.6	A22	Segment address line
		O		CAN1_TxD	CAN1: transmit data output
		O		CAN2_TxD	CAN2: transmit data output
	92	O	P4.7	A23	Most significant segment address line
		O		CAN2_TxD	CAN2: transmit data output
		I/O		SDA	I^2C Interface: serial data
$\overline{RD}$	95	O	External memory read strobe. $\overline{RD}$ is activated for every external instruction or data read access.		
$\overline{WR}/\overline{WRL}$	96	O	External memory write strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$ mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection.		
READY/ $\overline{READY}$	97	I	Ready input. The active level is programmable. When the ready function is enabled, the selected inactive level at this pin, during an external memory access, will force the insertion of waitstate cycles until the pin returns to the selected active level.		
ALE	98	O	Address latch enable output. In case of use of external addressing or of multiplexed mode, this signal is the latch command of the address lines.		

Table 1. Pin description (continued)

Symbol	Pin	Type	Function
$\overline{EA}$ / V_{STBY}	99	I	External access enable pin. A low level applied to this pin during and after Reset forces the ST10F276E to start the program from the external memory space. A high level forces ST10F276E to start in the internal memory space. This pin is also used (when Stand-by mode is entered, that is ST10F276E under reset and main V_{DD} turned off) to bias the 32 kHz oscillator amplifier circuit and to provide a reference voltage for the low-power embedded voltage regulator which generates the internal 1.8V supply for the RTC module (when not disabled) and to retain data inside the Stand-by portion of the XRAM (16 Kbyte). It can range from 4.5 to 5.5V (6V for a reduced amount of time during the device life, 4.0V when RTC and 32 kHz on-chip oscillator amplifier are turned off). In running mode, this pin can be tied low during reset without affecting 32 kHz oscillator, RTC and XRAM activities, since the presence of a stable V_{DD} guarantees the proper biasing of all those modules.
P0L.0 -P0L.7, P0H.0 P0H.1 - P0H.7	100-107, 108, 111-117	I/O	Two 8-bit bidirectional I/O ports P0L and P0H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold of Port 0 is selectable (TTL or CMOS). In case of an external bus configuration, PORT0 serves as the address (A) and as the address / data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. Demultiplexed bus modes Data path width: 8-bit / 16-bi P0L.0 – P0L.7: D0 – D7 / D0 - D7 P0H.0 – P0H.7: I/O / D8 - D15 Multiplexed bus modes Data path width: 8-bit / 16-bi P0L.0 – P0L.7: AD0 – AD7 / AD0 - AD7 P0H.0 – P0H.7: A8 – A15 / AD8 - AD15
P1L.0 - P1L.7 P1H.0 - P1H.7	118-125 128-135	I/O	Two 8-bit bidirectional I/O ports P1L and P1H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes: if at least BUSCONx is configured such the demultiplexed mode is selected, the pis of PORT1 are not available for general purpose I/O function. The input threshold of Port 1 is selectable (TTL or CMOS). The pins of P1L also serve as the additional (up to 8) analog input channels for the A/D converter, where P1L.x equals ANy (Analog input channel y, where y = x + 16). This additional function have higher priority on demultiplexed bus function. The following PORT1 pins have alternate functions:
	132	I	P1H.4 / CC24IO / CAPCOM2: CC24 capture input
	133	I	P1H.5 / CC25IO / CAPCOM2: CC25 capture input
	134	I	P1H.6 / CC26IO / CAPCOM2: CC26 capture input
	135	I	P1H.7 / CC27IO / CAPCOM2: CC27 capture input

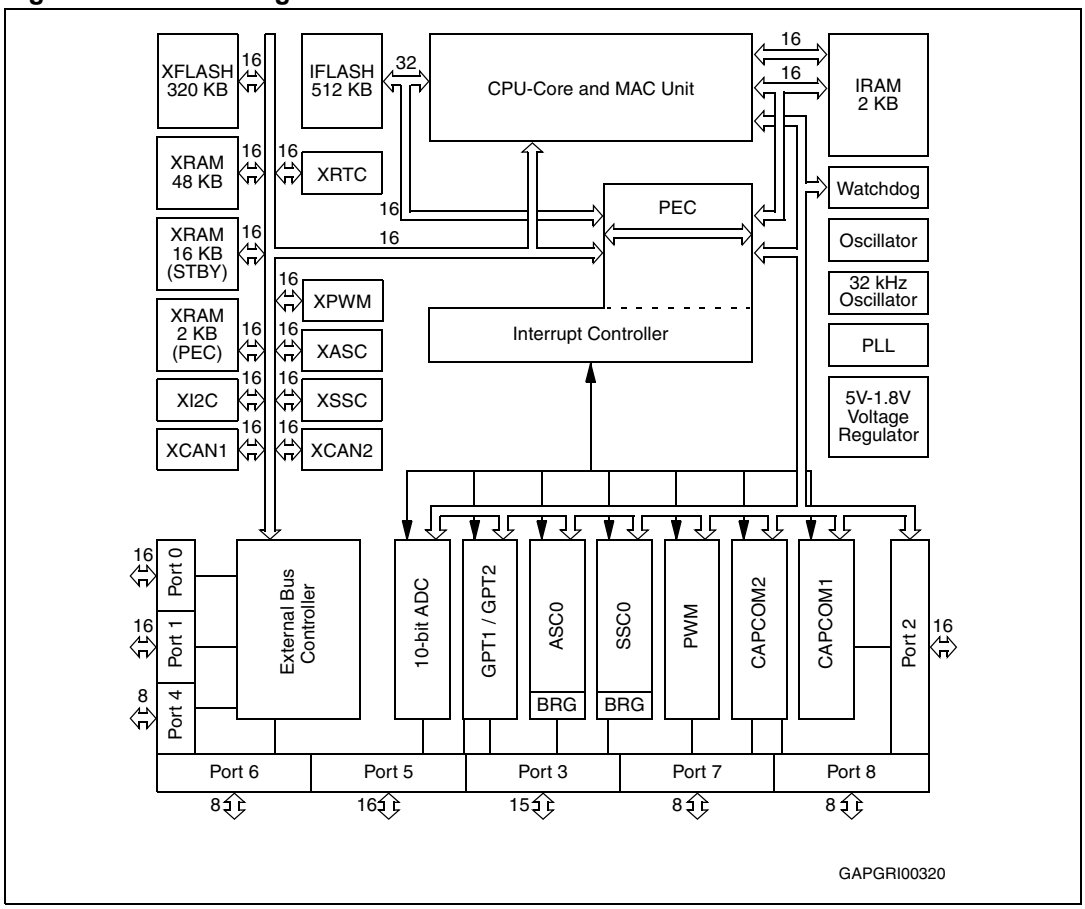
Table 1. Pin description (continued)

Symbol	Pin	Type	Function	
XTAL1	138	I	XTAL1	Main oscillator amplifier circuit and/or external clock input.
XTAL2	137	O	XTAL2	Main oscillator amplifier circuit output.
			To clock the device from an external source, drive XTAL1 while leaving XTAL2 unconnected. Minimum and maximum high / low and rise / fall times specified in the AC Characteristics must be observed.	
XTAL3	143	I	XTAL3	32 kHz oscillator amplifier circuit input
XTAL4	144	O	XTAL4	32 kHz oscillator amplifier circuit output
			When 32 kHz oscillator amplifier is not used, to avoid spurious consumption, XTAL3 shall be tied to ground while XTAL4 shall be left open. Besides, bit OFF32 in RTCCON register shall be set. 32 kHz oscillator can only be driven by an external crystal, and not by a different clock source.	
$\overline{\text{RSTIN}}$	140	I	Reset Input with CMOS Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10F276E. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. In bidirectional reset mode (enabled by setting bit BDRSTEN in SYSCON register), the $\overline{\text{RSTIN}}$ line is pulled low for the duration of the internal reset sequence.	
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is driven to a low level during hardware, software or watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.	
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10F276E to go into power down mode. If $\overline{\text{NMI}}$ is high and PWDCFG = '0', when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.	
V_{AREF}	37	-	A/D converter reference voltage and analog supply	
V_{AGND}	38	-	A/D converter reference and analog ground	
RPD	84	-	Timing pin for the return from interruptible power down mode and synchronous / asynchronous reset selection.	
V_{DD}	17, 46, 72,82,93, 109, 126, 136	-	Digital supply voltage = + 5V during normal operation, idle and power down modes. It can be turned off when Stand-by RAM mode is selected.	
V_{SS}	18,45, 55,71, 83,94, 110, 127, 139	-	Digital ground	
V_{18}	56	-	1.8V decoupling pin: a decoupling capacitor (typical value of 10nF, max 100nF) must be connected between this pin and nearest V_{SS} pin.	

3 Functional description

The architecture of the ST10F276E combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F276E.

Figure 3. Block diagram

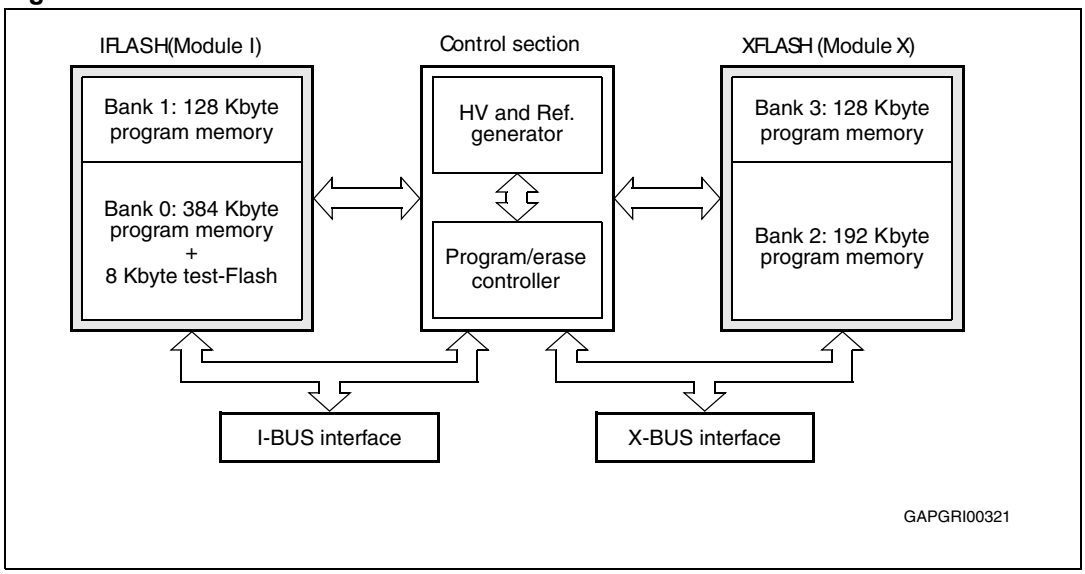


4 Internal Flash memory

4.1 Overview

The on-chip Flash is composed of two matrix modules, each one containing one array divided in two banks that can be read and modified independently of one another: one bank can be read while another bank is under modification.

Figure 4. Flash modules structure



The write operations of the four banks are managed by an embedded Flash program/erase controller (FPEC). The high voltages needed for program/erase operations are internally generated.

The data bus is 32-bit wide. Due to ST10 core architecture limitation, only the first 512 Kbytes are accessed at 32-bit (internal Flash bus, see I-BUS), while the remaining 320 Kbytes are accessed at 16-bit (see X-BUS).

4.2 Functional description

4.2.1 Structure

Table 2 shows the address space reserved to the Flash module.

Table 2. Flash modules absolute mapping

Description	Addresses	Size
IFLASH sectors	0x00 0000 to 0x08 FFFF	512 Kbyte
XFLASH sectors	0x09 0000 to 0x0D FFFF	320 Kbyte
Registers and Flash internal reserved area	0x0E 0000 to 0x0E FFFF	64 Kbyte

4.2.2 Modules structure

The IFLASH module is composed of two banks. Bank 0 contains 384 Kbyte of program memory divided in 10 sectors. Bank 0 contains also a reserved sector named test-Flash. Bank 1 contains 128 Kbyte of program memory or parameter divided in two sectors (64 Kbyte each).

The XFLASH module is composed of two banks as well. Bank 2 contains 192 Kbyte of program memory divided in three sectors. Bank 3 contains 128 Kbyte of program memory or parameter divided in two sectors (64 Kbyte each).

Addresses from 0x0E 0000 to 0x0E FFFF are reserved for the control register interface and other internal service memory space used by the Flash program/erase controller.

The following tables show the memory mapping of the Flash when it is accessed in read mode (*Table 3*), and when accessed in write or erase mode (*Table 2*): note that with this second mapping, the first three banks are remapped into code segment 1 (same as obtained when setting bit ROMS1 in SYSCON register).

Table 3. Flash modules sectorization (read operations)

Bank	Description	Addresses	Size	ST10 bus size
B0	Bank 0 Flash 0 (B0F0)	0x0000 0000 - 0x0000 1FFF	8 KB	32-bit (I-BUS)
	Bank 0 Flash 1 (B0F1)	0x0000 2000 - 0x0000 3FFF	8 KB	
	Bank 0 Flash 2 (B0F2)	0x0000 4000 - 0x0000 5FFF	8 KB	
	Bank 0 Flash 3 (B0F3)	0x0000 6000 - 0x0000 7FFF	8 KB	
	Bank 0 Flash 4 (B0F4)	0x0001 8000 - 0x0001 FFFF	32 KB	
	Bank 0 Flash 5 (B0F5)	0x0002 0000 - 0x0002 FFFF	64 KB	
	Bank 0 Flash 6 (B0F6)	0x0003 0000 - 0x0003 FFFF	64 KB	
	Bank 0 Flash 7 (B0F7)	0x0004 0000 - 0x0004 FFFF	64 KB	
	Bank 0 Flash 8 (B0F8)	0x0005 0000 - 0x0005 FFFF	64 KB	
	Bank 0 Flash 9 (B0F9)	0x0006 0000 - 0x0006 FFFF	64 KB	
B1	Bank 1 Flash 0 (B1F0)	0x0007 0000 - 0x0007 FFFF	64 KB	
	Bank 1 Flash 1 (B1F1)	0x0008 0000 - 0x0008 FFFF	64 KB	
B2	Bank 2 Flash 0 (B2F0)	0x0009 0000 - 0x0009 FFFF	64 KB	16-bit (X-BUS)
	Bank 2 Flash 1 (B2F1)	0x000A 0000 - 0x000A FFFF	64 KB	
	Bank 2 Flash 2 (B2F2)	0x000B 0000 - 0x000B FFFF	64 KB	
B3	Bank 3 Flash 0 (B3F0)	0x000C 0000 - 0x000C FFFF	64 KB	
	Bank 3 Flash 1 (B3F1)	0x000D 0000 - 0x000D FFFF	64 KB	