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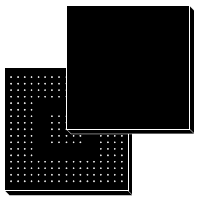
ST10F280

16-bit MCU with MAC unit, 512 Kbyte Flash memory and 18 Kbyte RAM

Datasheet – production data

Features

- High performance cpu with dsp functions
  - 16-bit CPU with 4-stage pipeline.
  - 50ns Instruction cycle time at 40MHz CPU clock
  - Multiply/accumulate unit (MAC) 16 x 16-bit multiplication, 40-bit accumulator
  - Repeat unit
  - Enhanced boolean bit manipulation facilities
  - Additional instructions to support hll and operating systems
  - Single-cycle context switching support
- Memory organization
  - 512KB on-chip Flash memory single voltage with erase/program controller
  - 100K erasing/programming cycles
  - 20 year data retention time
  - Up to 16MB linear address space for code and data (5MB with CAN)
  - 2KB on-chip internal ram (IRAM)
  - 16KB extension RAM (XRAM)
- Fast and flexible bus
  - Programmable external bus characteristics for different address ranges
  - 8-bit or 16-bit external data bus
  - Multiplexed or demultiplexed external address/data buses
  - Five programmable chip-select signals
  - Hold-acknowledge bus arbitration support
- Interrupt
  - 8-channel peripheral event controller for single cycle, interrupt driven data transfer
  - 16-priority-level interrupt system with 56 sources, sample-rate down to 25ns
- Two multi-functional general purpose timer units with 5 timers
- Two 16-channel capture/compare units



PBGA208 (23 x 23 x 1.96 - Pitch 1.27 mm)
(Plastic Bold Grid Array)

ORDER CODE: ST10F280-JT3

- A/D converter
  - 2X16-channel 10-bit
  - 4.85µs conversion time
  - One timer for adc channel injection
- 8-channel PWM unit
- Serial channels
  - Synchronous/async serial channel
  - High-speed synchronous channel
- Fail-safe protection
  - Programmable watchdog timer
  - Oscillator watchdog
- Two CAN 2.0b interfaces operating on one or two can busses (30 or 2x15 message objects)
- On-chip bootstrap loader
- Clock generation
  - On-chip PLL
  - Direct or prescaled clock input
- Up to 143 general purpose i/o lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Idle and power down modes
- Maximum cpu frequency 40MHz
- Package PBGA 208 balls (23 x 23 x 1.96 mm - pitch 1.27 mm)
- Single voltage supply: 5 V ±10% (embedded regulator for 3.3 V core supply)
- Temperature range: -40°C to 125°C

Contents

List of tables

List of figures

1 Description

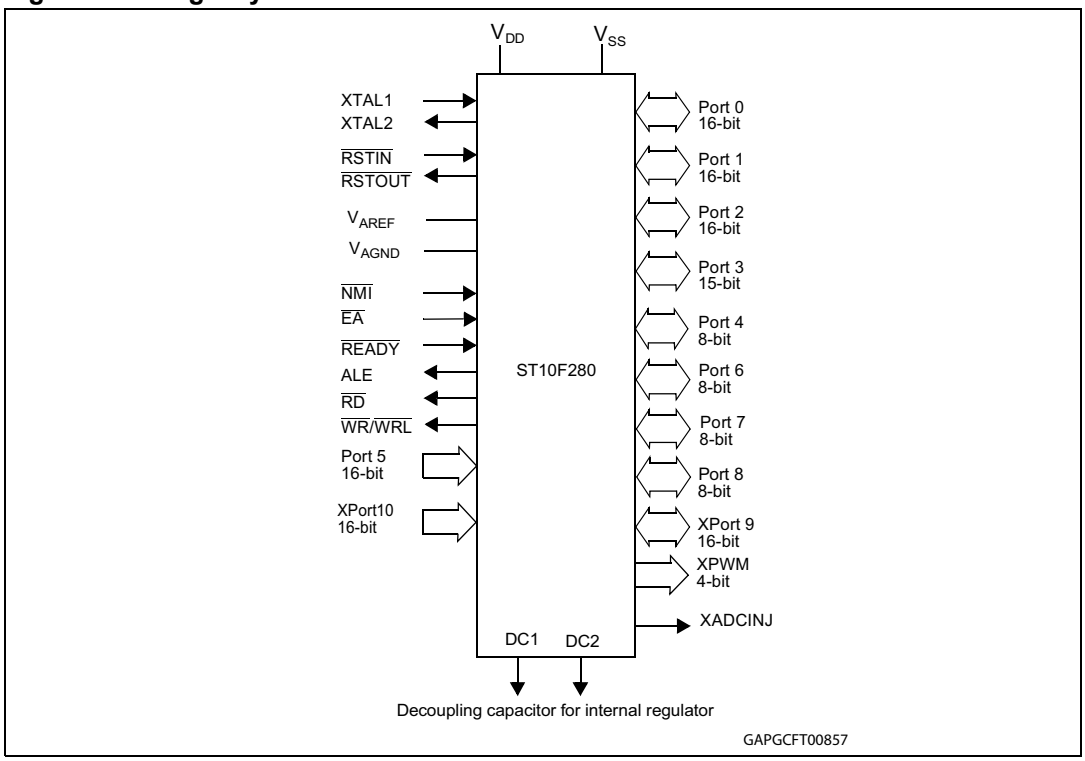
The ST10F280 is a new derivative of the STMicroelectronics® ST10 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 20 million instructions per second) with high peripheral functionality and enhanced I/O-capabilities. It also provides on-chip high-speed single voltage FLASH memory, on-chip high-speed RAM, and clock generation via PLL.

ST10F280 is processed in 0.35µm CMOS technology. The MCU core and the logic is supplied with a 5V to 3.3V on chip voltage regulator. The part is supplied with a single 5V supply and I/Os work at 5V.

The device is upward compatible with the ST10F269 device, with the following set of differences:

- Two supply pins (DC1,DC2) on the PBGA-208 package are used for decoupling the internally generated 3.3V core logic supply. Do not connect these two pins to 5.0V external supply. Instead, these pins should be connected to a decoupling capacitor (ceramic type, value ≥ 330nF).
- The A/D Converter characteristics stay identical but 16 new input channel are added. A bit in a new register (XADCMUX) control the multiplexage between the first block of 16 channel (on Port5) and the second block (on XPort10). The conversion result registers stay identical and the software management can determine the block in use. A new dedicated timer controls now the ADC channel injection mode on the input CC31 (P7.7). The output of this timer is visible on a dedicated pin (XADCINJ) to emulate this new functionality.
- A second XPWM peripheral (4 new channels) is added. Four dedicated pins are reserved for the outputs (XPWM[0:3])
- A new general purpose I/O port named XPORT9 (16 bits) is added. Due to the bit addressing management, it will be different from other standard general purpose I/O ports.

Figure 1. Logic symbol



2 Ball data

The ST10F280 package is a PBGA of 23 x 23 x 1.96 mm. The pitch of the balls is 1.27 mm. The signal assignment of the 208 balls is described in *Figure 2* for the configuration and in *Table 1* for the ball signal assignment. This package has 25 additional thermal balls.

Figure 2. Ball Configuration (bottom view)

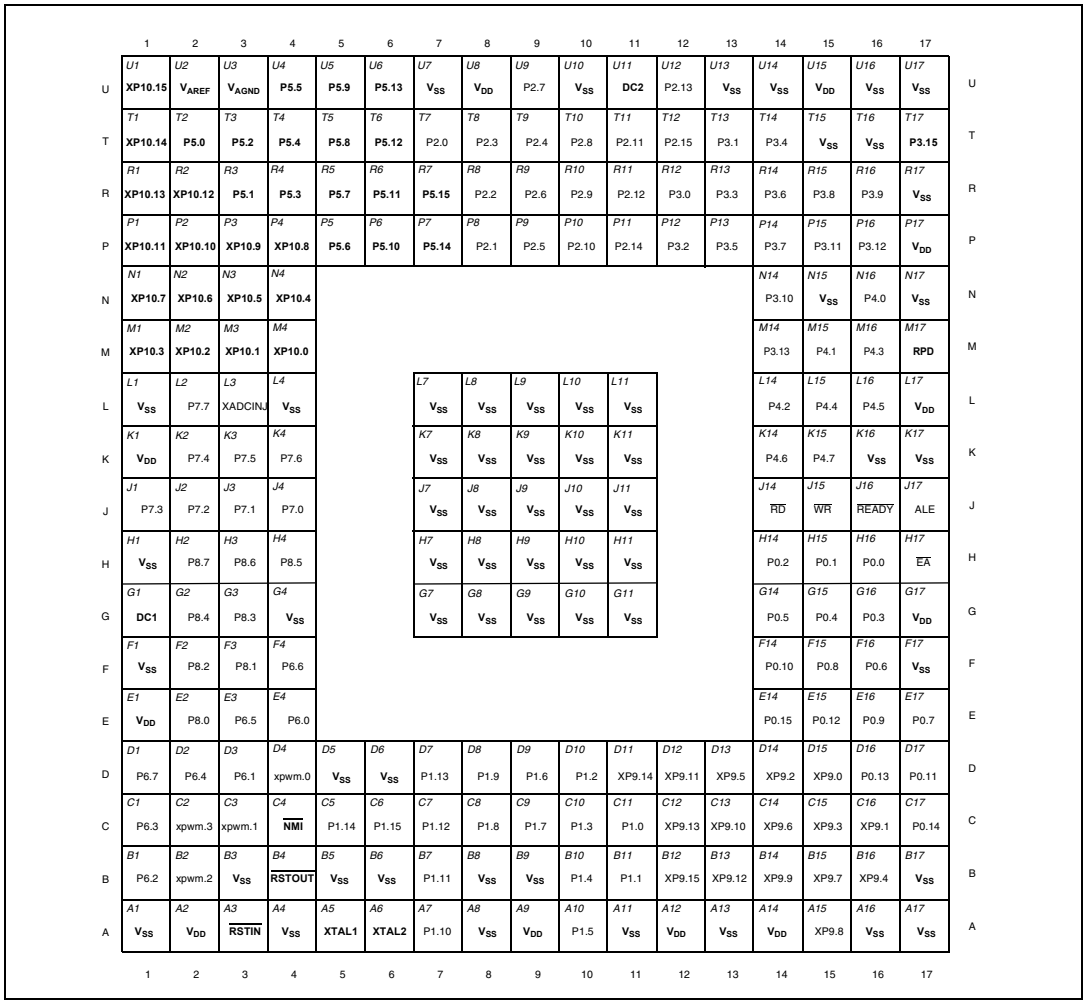


Table 1. Ball description

Symbol	Ball number	Type	Function
P6.0 – P6.7		I/O	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins also serve for alternate functions:
	E4	O	P6.0 $\overline{CS0}$ Chip Select 0 Output
	D3	O	P6.1 $\overline{CS1}$ Chip Select 1 Output
	B1	O	P6.2 $\overline{CS2}$ Chip Select 2 Output
	C1	O	P6.3 $\overline{CS3}$ Chip Select 3 Output
	D2	O	P6.4 $\overline{CS4}$ Chip Select 4 Output
	E3	I	P6.5 $\overline{HOLD}$ External Master Hold Request Input
	F4	O	P6.6 $\overline{HLDA}$ Hold Acknowledge Output
	D1	O	P6.7 $\overline{BREQ}$ Bus Request Output
P8.0 – P8.7		I/O	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
	E2	I/O	P8.0 CC16IO CAPCOM2: CC16 Capture Input / Compare Output
	F3	I/O	P8.1 CC17IO CAPCOM2: CC17 Capture Input / Compare Output
	F2	I/O	P8.2 CC18IO CAPCOM2: CC18 Capture Input / Compare Output
	G3	I/O	P8.3 CC19IO CAPCOM2: CC19 Capture Input / Compare Output
	G2	I/O	P8.4 CC20IO CAPCOM2: CC20 Capture Input / Compare Output
	H4	I/O	P8.5 CC21IO CAPCOM2: CC21 Capture Input / Compare Output
	H3	I/O	P8.6 CC22IO CAPCOM2: CC22 Capture Input / Compare Output
	H2	I/O	P8.7 CC23IO CAPCOM2: CC23 Capture Input / Compare Output

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P7.0 – P7.7		I/O	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
	J4	O	P7.0 POUT0 PWM Channel 0 Output
	J3	O	P7.1 POUT1 PWM Channel 1 Output
	J2	O	P7.2 POUT2 PWM Channel 2 Output
	J1	O	P7.3 POUT3 PWM Channel 3 Output
	K2	I/O	P7.4 CC28IO CAPCOM2: CC28 Capture Input / Compare Output
	K3	I/O	P7.5 CC29IO CAPCOM2: CC29 Capture Input / Compare Output
	K4	I/O	P7.6 CC30IO CAPCOM2: CC30 Capture Input / Compare Output
	L2	I/O	P7.7 CC31IO CAPCOM2: CC31 Capture Input / Compare Output
XP10.0 – XP10.15		I	XPort 10 is a 16-bit input-only port with Schmitt-Trigger characteristics. The pins of XPort10 also serve as the analog input channels (up to 16) for the A/D converter, where XP10.X equals ANx (Analog input channel x).
	M4	I	XP10.0
	M3	I	XP10.1
	M2	I	XP10.2
	M1	I	XP10.3
	N4	I	XP10.4
	N3	I	XP10.5
	N2	I	XP10.6
	N1	I	XP10.7
	P4	I	XP10.8
	P3	I	XP10.9
	P2	I	XP10.10
	P1	I	XP10.11
	R2	I	XP10.12
	R1	I	XP10.13
	T1	I	XP10.14
	U1	I	XP10.15

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P5.0 – P5.15		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as the analog input channels (up to 16) for the A/D converter, where P5.x equals ANx (Analog input channel x), or they serve as timer inputs:
	T2	I	P5.0
	R3	I	P5.1
	T3	I	P5.2
	R4	I	P5.3
	T4	I	P5.4
	U4	I	P5.5
	P5	I	P5.6
	R5	I	P5.7
	T5	I	P5.8
	U5	I	P5.9
	P6	I	P5.10 T6EUD GPT2 Timer T6 External Up / Down Control Input
	R6	I	P5.11 T5EUD GPT2 Timer T5 External Up / Down Control Input
	T6	I	P5.12 T6IN GPT2 Timer T6 Count Input
	U6	I	P5.13 T5IN GPT2 Timer T5 Count Input
	P7	I	P5.14 T4EUD GPT1 Timer T4 External Up / Down Control Input
	R7	I	P5.15 T2EUD GPT1 Timer T2 External Up / Down Control Input

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P2.0 – P2.15		I/O	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:
	T7	I/O	P2.0 CC0IO CAPCOM: CC0 Capture Input / Compare Output
	P8	I/O	P2.1 CC1IO CAPCOM: CC1 Capture Input / Compare Output
	R8	I/O	P2.2 CC2IO CAPCOM: CC2 Capture Input / Compare Output
	T8	I/O	P2.3 CC3IO CAPCOM: CC3 Capture Input / Compare Output
	T9	I/O	P2.4 CC4IO CAPCOM: CC4 Capture Input / Compare Output
	P9	I/O	P2.5 CC5IO CAPCOM: CC5 Capture Input / Compare Output
	R9	I/O	P2.6 CC6IO CAPCOM: CC6 Capture Input / Compare Output
	U9	I/O	P2.7 CC7IO CAPCOM: CC7 Capture Input / Compare Output
	T10	I/O I	P2.8 CC8IO CAPCOM: CC8 Capture Input / Compare Output, EX0IN Fast External Interrupt 0 Input
	R10	I/O I	P2.9 CC9IO CAPCOM: CC9 Capture Input / Compare Output, EX1IN Fast External Interrupt 1 Input
	P10	I/O I	P2.10 CC10IO CAPCOM: CC10 Capture Input / Compare Output, EX2IN Fast External Interrupt 2 Input
	T11	I/O I	P2.11 CC11IO CAPCOM: CC11 Capture Input / Compare Output, EX3IN Fast External Interrupt 3 Input
	R11	I/O I	P2.12 CC12IO CAPCOM: CC12 Capture Input / Compare Output, EX4IN Fast External Interrupt 4 Input
	U12	I/O I	P2.13 CC13IO CAPCOM: CC13 Capture Input / Compare Output, EX5IN Fast External Interrupt 5 Input
	P11	I/O I	P2.14 CC14IO CAPCOM: CC14 Capture Input / Compare Output, EX6IN Fast External Interrupt 6 Input
	T12	I/O I I	P2.15 CC15IO CAPCOM: CC15 Capture Input / Compare Output, EX7IN Fast External Interrupt 7 Input T7IN CAPCOM2 Timer T7 Count Input

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P3.0 - P3.13, P3.15		I/O	Port 3 is a 15-bit (P3.14 is missing) bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:
	R12	I	P3.0 T0IN CAPCOM Timer T0 Count Input
	T13	O	P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output
	P12	I	P3.2 CAPIN GPT2 Register CAPREL Capture Input
	R13	O	P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output
	T14	I	P3.4 T3EUD GPT1 Timer T3 External Up / Down Control Input
	P13	I	P3.5 T4IN GPT1 Timer T4 Input for Count / Gate / Reload / Capture
	R14	I	P3.6 T3IN GPT1 Timer T3 Count / Gate Input
	P14	I	P3.7 T2IN GPT1 Timer T2 Input for Count / Gate / Reload / Capture
	R15	I/O	P3.8 MRST SSC Master-Receive / Slave-Transmit I/O
	R16	I/O	P3.9 MTSR SSC Master-Transmit / Slave-Receive O/I
	N14	I/O	P3.10 TxD0 ASC0 Clock / Data Output (Asynchronous / Synchronous)
	P15	O	P3.11 RxD0 ASC0 Data Input (Asynchronous) or I/O (Synchronous)
	P16	O	P3.12 $\overline{BHE}$ External Memory High Byte Enable Signal, $\overline{WRH}$ External Memory High Byte Write Strobe
	M14	I/O	P3.13 SCLK SSC Master Clock Output / Slave Clock Input
	T17	O	P3.15 CLKOUT System Clock Output (= CPU Clock)

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P4.0 – P4.7		I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The input threshold is selectable (TTL or special). P4.6 & P4.7 outputs can be configured as push-pull or open-drain drivers. In case of an external bus configuration, Port 4 can be used to output the segment address lines:
	N16	O	P4.0 A16 Least Significant Segment Address Line
	M15	O	P4.1 A17 Segment Address Line
	L14	O	P4.2 A18 Segment Address Line
	M16	O	P4.3 A19 Segment Address Line
	L15	O I	P4.4 A20 Segment Address Line CAN2_RxD CAN2 Receive Data Input
	L16	O I	P4.5 A21 Segment Address Line CAN1_RxD CAN1 Receive Data Input
	K14	O O	P4.6 A22 Segment Address Line, CAN_TxD CAN1_TxD CAN1 Transmit Data Output
	K15	O O	P4.7 A23 Most Significant Segment Address Line CAN2_TxD CAN2 Transmit Data Output
RD	J14	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}/\overline{WRL}$	J15	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
READY/ $\overline{READY}$	J16	I	Ready Input. The active level is programmable. When the Ready function is enabled, the selected inactive level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to the selected active level.
ALE	J17	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
EA	H17	I	External Access Enable pin. A low level at this pin during and after Reset forces the ST10F280 to begin instruction execution out of external memory. A high level forces execution out of the internal Flash Memory.

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
PORT0: P0L.0 - P0L.7, P0H.0 - P0H.7		I/O	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. Demultiplexed bus modes: Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 - D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 Multiplexed bus modes: Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 - AD7 AD0 - AD7 P0H.0 – P0H.7: A8 - A15 AD8 - AD15
	H16	I/O	P0L.0
	H15	I/O	P0L.1
	H14	I/O	P0L.2
	G16	I/O	P0L.3
	G15	I/O	P0L.4
	G14	I/O	P0L.5
	F16	I/O	P0L.6
	E17	I/O	P0L.7
	F15	I/O	P0H.0
	E16	I/O	P0H.1
	F14	I/O	P0H.2
	D17	I/O	P0H.3
	E15	I/O	P0H.4
	D16	I/O	P0H.5
	C17	I/O	P0H.6
	E14	I/O	P0H.7

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
XPORT9.0 - XPORT9.15		I/O	XPort 9 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. XPort 9 outputs can be configured as push/pull or open drain drivers.
	D15	I/O	XPORT9.0
	C16	I/O	XPORT9.1
	D14	I/O	XPORT9.2
	C15	I/O	XPORT9.3
	B16	I/O	XPORT9.4
	D13	I/O	XPORT9.5
	C14	I/O	XPORT9.6
	B15	I/O	XPORT9.7
	A15	I/O	XPORT9.8
	B14	I/O	XPORT9.9
	C13	I/O	XPORT9.10
	D12	I/O	XPORT9.11
	B13	I/O	XPORT9.12
	C12	I/O	XPORT9.13
	D11	I/O	XPORT9.14
	B12	I/O	XPORT9.15

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
PORT1: P1L.0 - P1L.7, P1H.0 - P1H.7		I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions:
	C11	I/O	P1L.0
	B11	I/O	P1L.1
	D10	I/O	P1L.2
	C10	I/O	P1L.3
	B10	I/O	P1L.4
	A10	I/O	P1L.5
	D9	I/O	P1L.6
	C9	I/O	P1L.7
	C8	I/O	P1H.0
	D8	I/O	P1H.1
	A7	I/O	P1H.2
	B7	I/O	P1H.3
	C7	I	P1H.4 CC24IO CAPCOM2: CC24 Capture Input
	D7	I	P1H.5 CC25IO CAPCOM2: CC25 Capture Input
	C5	I	P1H.6 CC26IO CAPCOM2: CC26 Capture Input
	C6	I	P1H.7 CC27IO CAPCOM2: CC27 Capture Input
XTAL1	A5	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	A6	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
RSTIN	A3	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10F280. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. In bidirectional reset mode (enabled by setting bit BDRSTEN in SYSCON register), the $\overline{\text{RSTIN}}$ line is pulled low for the duration of the internal reset sequence.
RSTOUT	B4	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware, a software or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
NMI	C4	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the $\overline{NMI}$ pin must be low in order to force the ST10F280 to go into power down mode. If $\overline{NMI}$ is high and PWDCFG ='0', when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{NMI}$ should be pulled high externally.
XPWM.0	D4	O	XPWM Channel 0 Output
XPWM.1	C3	O	XPWM Channel 1 Output
XPWM.2	B2	O	XPWM Channel 2 Output
XPWM.3	C2	O	XPWM Channel 3 Output
XADCINJ	L3	O	Output trigger for ADC channel injection
V_{AREF}	U2	-	Reference voltage for the A/D converter.
V_{AGND}	U3	-	Reference ground for the A/D converter.
RPD	M17	I/O	Timing pin for the return from powerdown circuit and synchronous/asynchronous reset selection.
DC1	G1	O	3.3V Decoupling pin: a decoupling capacitor of ~330 nF must be connected between this pin and nearest V_{SS} pin.
DC2	U11	O	3.3V Decoupling pin: a decoupling capacitor of ~330 nF must be connected between this pin and V_{SS} nearest pin.
V_{DD}	A2 A9 A12 A14 E1 K1 U8 U15 P17 L17 G17	-	Digital Supply Voltage: + 5 V during normal operation, idle mode and power down mode

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
V_{SS}	A1 A4 A8 A11 A13 A16 A17 B3 B5 B6 B8 B9 B17 D5 D6 F1 F17 G4 H1 K16 K17 L1 L4 N15 N17 R17 T15 T16 U7 U10 U13 U14 U16 U17	-	Digital ground.