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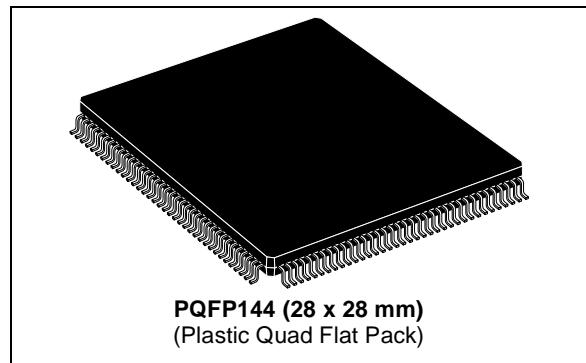
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16-BIT ROMLESS MCU

- HIGH PERFORMANCE CPU
 - 16-BIT CPU WITH 4-STAGE PIPELINE
 - 80ns INSTRUCTION CYCLE TIME @ 25MHz CLK
 - 400ns 16 X 16-BIT MULTIPLICATION
 - 800ns 32 / 16-BIT DIVISION
 - ENHANCED BOOLEAN BIT MANIPULATION FACILITIES
 - ADDITIONAL INSTRUCTIONS TO SUPPORT HLL AND OPERATING SYSTEMS
 - SINGLE-CYCLE CONTEXT SWITCHING SUPPORT
- MEMORY ORGANIZATION
 - UP TO 16M BYTE LINEAR ADDRESS SPACE FOR CODE AND DATA (5M BYTE WITH CAN)
 - 2K BYTE ON-CHIP INTERNAL RAM (IRAM)
 - 2K BYTE ON-CHIP EXTENSION RAM (XRAM)
- FAST AND FLEXIBLE BUS
 - PROGRAMMABLE EXTERNAL BUS CHARACTERISTICS FOR DIFFERENT ADDRESS RANGES
 - 8-BIT OR 16-BIT EXTERNAL DATA BUS
 - MULTIPLEXED OR DEMULTIPLEXED EXTERNAL ADDRESS/DATA BUSES
 - FIVE PROGRAMMABLE CHIP-SELECT SIGNALS
 - HOLD-ACKNOWLEDGE BUS ARBITRATION SUPPORT
- INTERRUPT
 - 8-CHANNEL PERIPHERAL EVENT CONTROLLER FOR SINGLE CYCLE, INTERRUPT DRIVEN DATA TRANSFER
 - 16-PRIORITY-LEVEL INTERRUPT SYSTEM WITH 56 SOURCES, SAMPLE-RATE DOWN TO 40ns
- TIMERS
 - TWO MULTI-FUNCTIONAL GENERAL PURPOSE TIMER UNITS WITH 5 TIMERS
 - TWO 16-CHANNEL CAPTURE/COMPARE UNITS
- A/D CONVERTER
 - 16-CHANNEL 10-BIT
 - 7.76µs CONVERSION TIME
- FAIL-SAFE PROTECTION
 - PROGRAMMABLE WATCHDOG TIMER
 - OSCILLATOR WATCHDOG
- ON-CHIP CAN 2.0B INTERFACE
- ON-CHIP BOOTSTRAP LOADER
- CLOCK GENERATION
 - ON-CHIP PLL
 - DIRECT OR PRESCALED CLOCK INPUT



- UP TO 111 GENERAL PURPOSE I/O LINES
 - INDIVIDUALLY PROGRAMMABLE AS INPUT, OUTPUT OR SPECIAL FUNCTION
 - PROGRAMMABLE DRIVE STRENGTH
 - PROGRAMMABLE THRESHOLD (HYSTERESIS)
- IDLE AND POWER DOWN MODES
 - IDLE CURRENT <95mA
 - POWER-DOWN SUPPLY CURRENT <400µA
- 4-CHANNEL PWM UNIT
- SERIAL CHANNELS
 - SYNCHRONOUS/ASYNCHRONOUS SERIAL CHANNEL
 - HIGH-SPEED SYNCHRONOUS CHANNEL
- DEVELOPMENT SUPPORT
 - C-COMPILERS, MACRO-ASSEMBLER PACKAGES, EMULATORS, EVAL BOARDS, HLL-DEBUGGERS, SIMULATORS, LOGIC ANALYZER DISASSEMBLERS, PROGRAMMING BOARDS
- 144-PIN PQFP PACKAGE

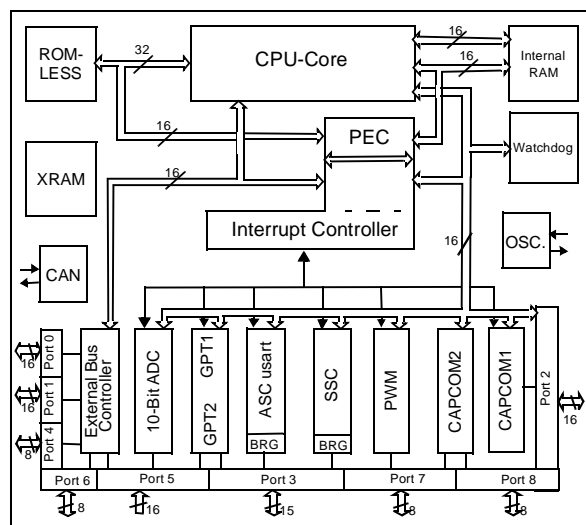


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ST10R167

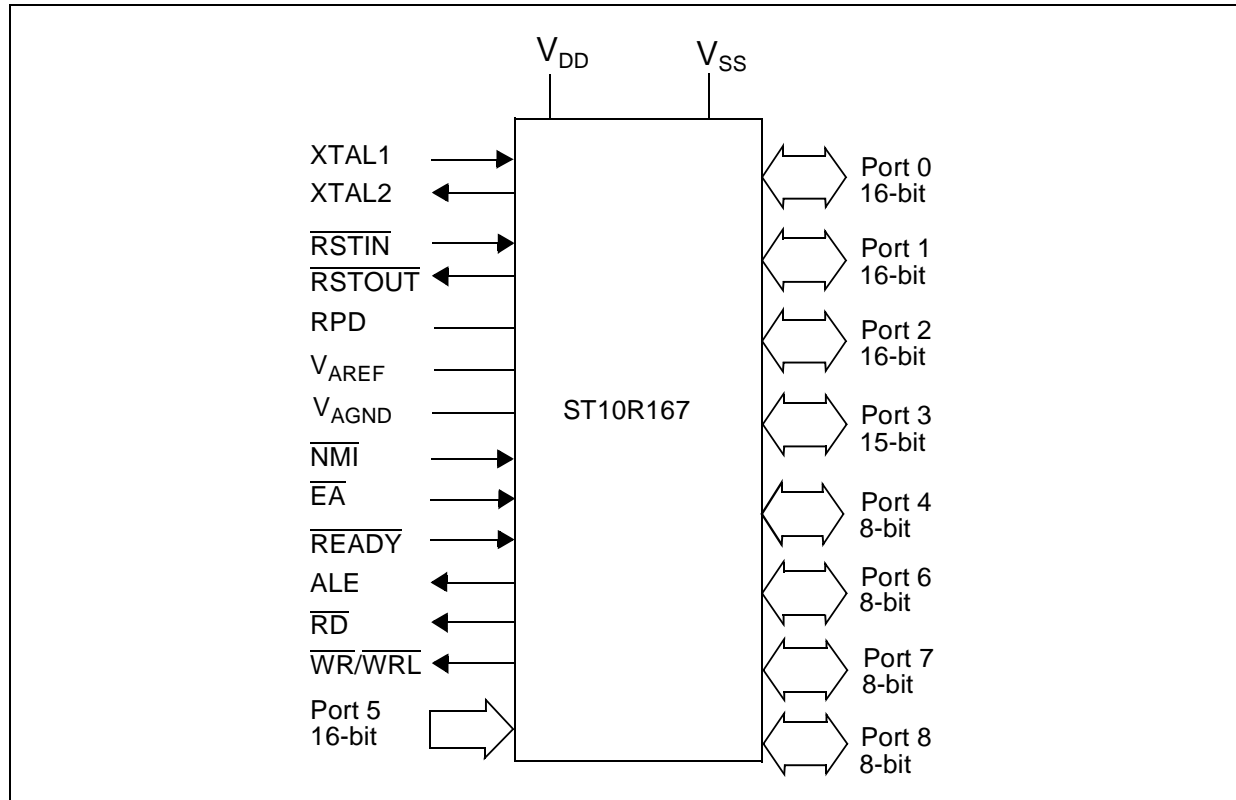
I - INTRODUCTION

The ST10R167 is a derivative of the STMicroelectronics ST10 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million

instructions per second) with high peripheral functionality and enhanced I/O capabilities.

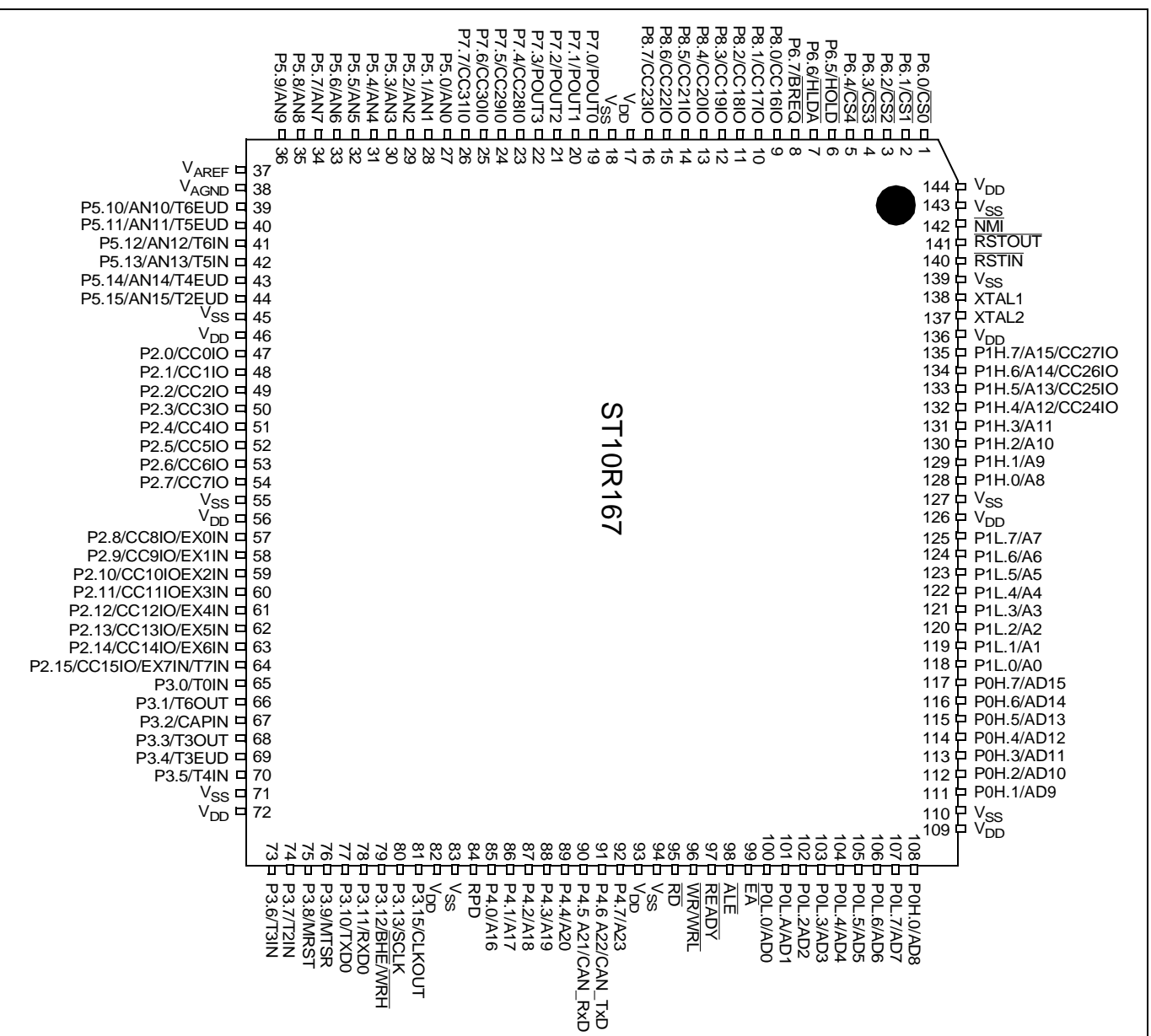
It also provides on-chip high-speed RAM and clock generation via PLL.

Figure 1 : Logic Symbol



II - PIN DATA

Figure 2 : Pin Configuration (top view)



II - PIN DATA (continued)

Table 1 : Pin list

Symbol	Pin	Type	Function
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins have alternate functions:
	1	O	P6.0 $\overline{CS0}$ Chip Select 0 Output

	5	O	P6.4 $\overline{CS4}$ Chip Select 4 Output
	6	I	P6.5 \overline{HOLD} External Master Hold Request Input
	7	O	P6.6 \overline{HLDA} Hold Acknowledge Output
	8	O	P6.7 \overline{BREQ} Bus Request Output
P8.0 - P8.7	9 - 16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins have alternate functions:
	9	I/O	P8.0 CC16IO CAPCOM2: CC16 Capture Input/Compare Output

	16	I/O	P8.7 CC23IO CAPCOM2: CC23 Capture Input/Compare Output
P7.0 - P7.7	19 - 26	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins have alternate functions:
	19	O	P7.0 POUT0 PWM Channel 0 Output

	22	O	P7.3 POUT3 PWM Channel 3 Output
	23	I/O	P7.4 CC28IO CAPCOM2: CC28 Capture Input/Compare Output

26	I/O	P7.7 CC31IO CAPCOM2: CC31 Capture Input/Compare Output	
P5.0 - P5.9 P5.10 - P5.15	27 - 36 39 - 44	I I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as the (up to 16) analog input channels for the A/D converter, where P5.x equals ANx (Analog input channel x), or they serve as timer inputs:
	39	I	P5.10 T6EUD GPT2 Timer T6 External Up/Down Control Input
	40	I	P5.11 T5EUD GPT2 Timer T5 External Up/Down Control Input
	41	I	P5.12 T6IN GPT2 Timer T6 Count Input
	42	I	P5.13 T5IN GPT2 Timer T5 Count Input
	43	I	P5.14 T4EUD GPT1 Timer T4 External Up/Down Control Input
	44	I	P5.15 T2EUD GPT1 Timer T2 External Up/Down Control Input

II - PIN DATA (continued)

Table 1 : Pin list (continued)

Symbol	Pin	Type	Function
P2.0 - P2.7 P2.8 - P2.15	47 - 54 57 - 64	I/O	16-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins have alternate functions:
	47	I/O	P2.0 CC0IO CAPCOM: CC0 Capture Input/Compare Output

	54	I/O	P2.7 CC7IO CAPCOM: CC7 Capture Input/Compare Output
	57	I/O	P2.8 CC8IO CAPCOM: CC8 Capture Input/Compare Output
			EX0IN Fast External Interrupt 0 Input

	64	I/O	P2.15 CC15IO CAPCOM: CC15 Capture Input/Compare Output
			EX7IN Fast External Interrupt 7 Input
			T7IN CAPCOM2 Timer T7 Count Input
P3.0 - P3.5 P3.6 - P3.13 P3.15	65 - 70 73 - 80 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins have alternate functions:
	65	I	P3.0 T0IN CAPCOM Timer T0 Count Input
	66	O	P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output
	67	I	P3.2 CAPIN GPT2 Register CAPREL Capture Input
	68	O	P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output
	69	I	P3.4 T3EUD GPT1 Timer T3 External Up/Down Control Input
	70	I	P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture
	73	I	P3.6 T3IN GPT1 Timer T3 Count/Gate Input
	74	I	P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture
	75	I/O	P3.8 MRST SSC Master-Receive/Slave-Transmit I/O
	76	I/O	P3.9 MTSR SSC Master-Transmit/Slave-Receive O/I
	77	I/O	P3.10 TxD0 ASC0 Clock/Data Output (Asynchronous/Synchronous)
	78	O	P3.11 RxD0 ASC0 Data Input (Asyn.) or I/O (Synchronous)
	79	O	P3.12 $\overline{\text{BHE}}$ External Memory High Byte Enable Signal, $\overline{\text{WRH}}$ External Memory High Byte Write Strobe
	80	I/O	P3.13 SCLK SSC Master Clock Output/Slave Clock Input
	81	O	P3.15 CLKOUT System Clock Output (=CPU Clock)
P4.0 - P4.7	85 - 92	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. For external bus configuration, Port 4 can be used to output the segment address lines:
	85 - 89	O	P4.0 - P4.4 A16 - A20 Least Significant Segment Address Line
	90	O	P4.5 A21 Segment Address Line
			CAN_RxD CAN Receive Data Input
	91	O	P4.6 A22 Segment Address Line,
			CAN_TxD CAN Transmit Data Output
	92	O	P4.7 A23 Most Significant Segment Address Line
$\overline{\text{RD}}$	95	O	External Memory Read Strobe. $\overline{\text{RD}}$ is activated for every external instruction or data read access.

II - PIN DATA (continued)

Table 1 : Pin list (continued)

Symbol	Pin	Type	Function
$\overline{WR}/\overline{WRL}$	96	O	External Memory Write Strobe. In \overline{WR} -mode this pin is activated for every external data write access. In \overline{WRL} -mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}/\overline{READY}$	97	I	Ready Input. The active level is programmable. When the Ready function is enabled, the selected inactive level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to the selected active level.
ALE	98	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
\overline{EA}	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the ST10R167 to begin instruction execution out of external memory. A high level forces execution out of the internal Flash Memory.
P0L.0 - P0L.7 P0H.0 P0H.1 - P0H.7	100 - 107 108 111 - 117	I/O	Port 0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. Demultiplexed bus modes: Data Path Width : 8-bit 16-bit P0L.0 – P0L.7 : D0 – D7 D0 - D7 P0H.0 – P0H.7 : I/O D8 - D15 Multiplexed bus modes: Data Path Width : 8-bit 16-bit P0L.0 – P0L.7 : AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7 : A8 - A15 AD8 - AD15
P1L.0 - P1L.7 P1H.0 - P1H.7	118 - 125 128 - 135	I/O	Port 1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions:
	132	I	P1H.4 CC24IO CAPCOM2: CC24 Capture Input
	133	I	P1H.5 CC25IO CAPCOM2: CC25 Capture Input
	134	I	P1H.6 CC26IO CAPCOM2: CC26 Capture Input
	135	I	P1H.7 CC27IO CAPCOM2: CC27 Capture Input
XTAL1	138	I	Input to the oscillator amplifier and input to the internal clock generator
XTAL2	137	O	Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
\overline{RSTIN}	140	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10R167. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS} . In bidirectional reset mode (enabled by setting bit BDRSTEN in SYSCON register), the \overline{RSTIN} line is pulled low for the duration of the internal reset sequence.

II - PIN DATA (continued)

Table 1 : Pin list (continued)

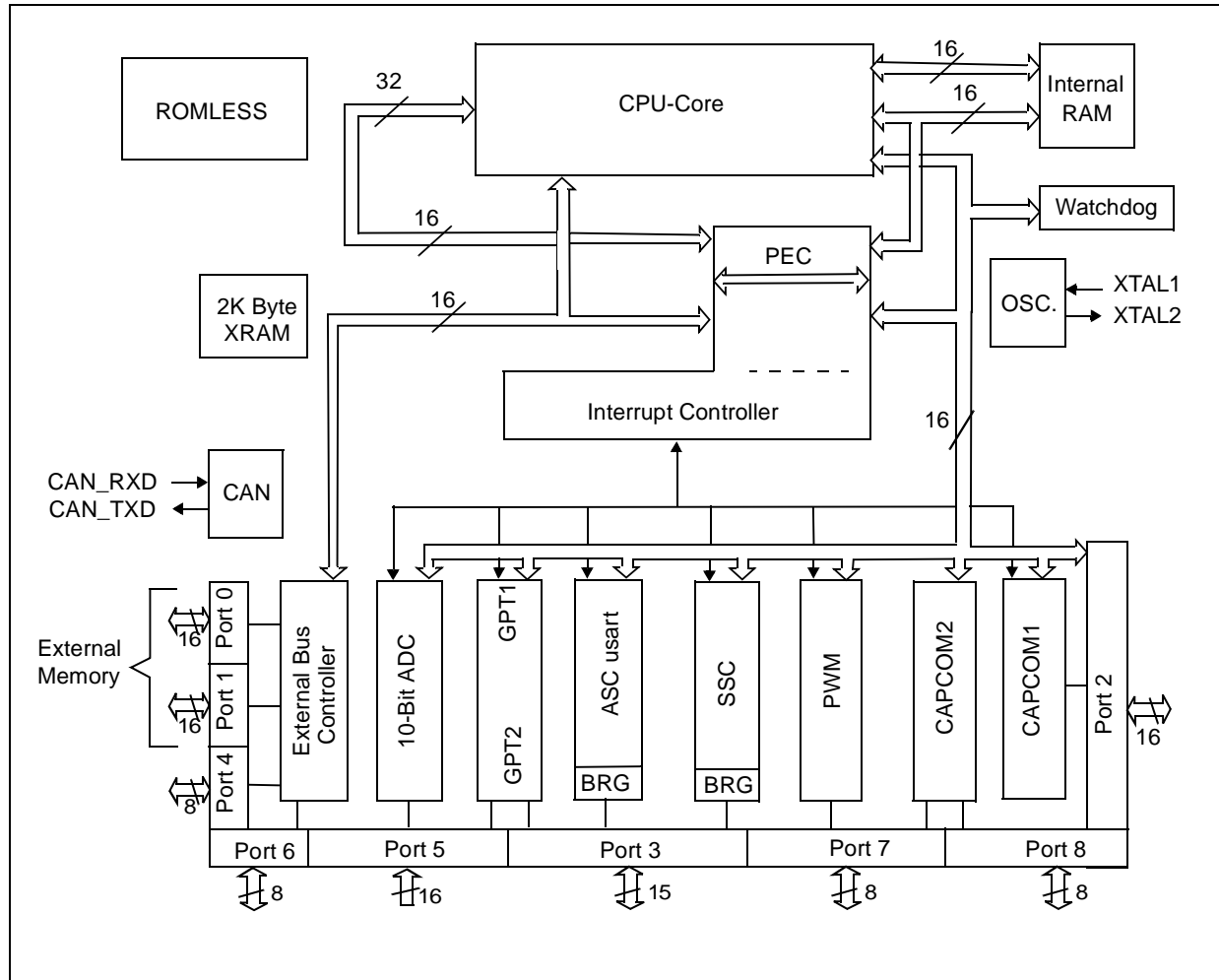
Symbol	Pin	Type	Function
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is set to a low level when the part is <u>executing</u> either a hardware-, a software- or a watchdog-timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10R167 to go into power down mode. If $\overline{\text{NMI}}$ is high and PWDCFG = '0', when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.
V_{AREF}	37	-	Reference voltage for the A/D converter.
V_{AGND}	38	-	Reference ground for the A/D converter.
RPD	84	-	This pin is used as the timing pin for the return from powerdown circuit and power-up asynchronous reset.
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	-	Digital Supply Voltage: = + 5V during normal operation and idle mode. ≥ + 2.5V during power down mode
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	-	Digital Ground.

III - FUNCTIONAL DESCRIPTION

The architecture of the ST10R167 combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The

block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10R167.

Figure 3 : Block diagram



IV - MEMORY ORGANIZATION

The memory space of the ST10R167 is configured in a Von-Neumann architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16M Byte.

The entire memory space can be accessed Byte-wise or Wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

ROM : 32K Byte of on-chip ROM.

RAM : 2K Byte of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. The register bank can consist of up to 16 wordwide (R0 to R15) and/or Byte-wide (RL0, RH0, ..., RL7, RH7) general purpose registers.

XRAM : 2K Byte of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.

The XRAM is connected to the internal XBUS and is accessed like an external memory in 16-bit demultiplexed bus-mode without waitstate or read/write delay (80ns access at 25MHz CPU clock). Byte and Word access is allowed.

The XRAM address range is 00'E000h - 00'E7FFh if the XRAM is enabled (XPEN bit 2 of SYSCON register). As the XRAM appears like external memory, it cannot be used for the ST10R167's system stack or register banks. The

XRAM is not provided for single bit storage and therefore is not bit addressable. If bit XRAMEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

SFR/ESFR : 1024 Byte (2 * 512 Byte) of address space is reserved for the special function register areas. SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units.

CAN : Address range 00'EF00h - 00'FFFFh is reserved for the CAN Module access. The CAN is enabled by setting XPEN bit 2 of the SYSCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (Byte accesses are possible). Two wait states give an access time of 160ns at 25MHz CPU clock. No tristate waitstate is used.

Note If the CAN module is used, Port 4 can not be programmed to output all 8 segment address lines. Thus, only 4 segment address lines can be used, reducing the external memory space to 5M Byte (1M Byte per CS line).

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16M Byte of external RAM and/or ROM can be connected to the microcontroller.

V - CENTRAL PROCESSING UNIT (CPU)

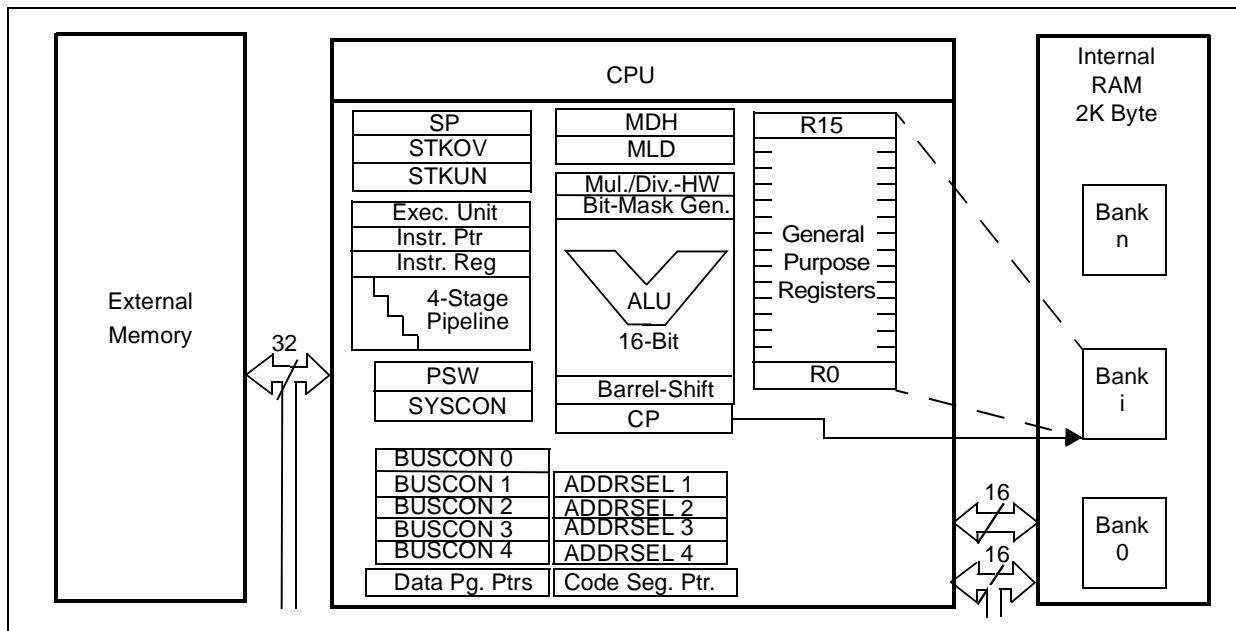
The CPU includes a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been added for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Most of the ST10R167's instructions can be executed in one instruction cycle which requires 80ns at 25MHz CPU clock. For example, shift and rotate instructions are processed in one instruction cycle independent of the number of bits to be shifted. Multiple-cycle instructions have been optimized: branches are carried out in 2 cycles, 16 x 16 bit multiplication in 5 cycles and a 32/16 bit division in 10 cycles. The jump cache reduces the execution time of repeatedly performed jumps in a loop, from 2 cycles to 1 cycle.

The CPU uses an actual register context consisting of up to 16 Word wide GPRs physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 Byte is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

Figure 4 : CPU Block Diagram



VI - EXTERNAL BUS CONTROLLER

All of the external memory accesses are performed by the on-chip external bus controller. The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

- 16-/18-/20-/24-bit addresses and 16-bit data, demultiplexed.
- 16-/18-/20-/24-bit addresses and 16-bit data, multiplexed.
- 16-/18-/20-/24-bit addresses and 8-bit data, multiplexed.
- 16-/18-/20-/24-bit addresses and 8-bit data, demultiplexed.

In demultiplexed bus modes addresses are output on Port1 and data is input/output on Port0 or POL, respectively. In the multiplexed bus modes both addresses and data use Port0 for input/output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read/write delay) are programmable giving the choice of a wide range of memories and external peripherals. Up to 4 independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external \overline{CS} signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a 'Ready' function.

A $\overline{HOLD}/\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 (\overline{BREQ} , \overline{HLDA} , \overline{HOLD}) are automatically controlled by the EBC. In master mode (default after reset) the \overline{HLDA} pin is an output. By setting bit DP6.7 to '1' the slave mode is selected where pin \overline{HLDA} is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1M Byte, 256K Byte or to 64K Byte. Port 4 outputs all 8 address lines if an address space of 16M Byte is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the CSx lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the CSx lines change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

VII - INTERRUPT SYSTEM

The interrupt response time for internal program execution is from 200ns to 480ns.

The ST10R167 architecture supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single Byte or Word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The ST10R167 has 8 PEC channels each of

which offers such fast interrupt-driven data transfer capabilities.

A interrupt control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield is dedicated to each existing interrupt source. Thanks to its related register, each source can be programmed to one of sixteen interrupt priority levels. Once starting to be processed by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 2 shows all the available ST10R167 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers :

Table 2 : Interrupt sources

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00'0040h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00'0044h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00'0048h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00'004Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00'0050h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00'0054h	15h
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	00'0058h	16h
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	00'005Ch	17h
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	00'0060h	18h
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	00'0064h	19h
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h

VII - INTERRUPT SYSTEM (continued)

Table 2 : Interrupt sources (continued)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00E0h	3Ch
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM Timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4h	29h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0h	2Ch
SSC Transmit	SCTIR	SCTIE	SCTINT	00'00B4h	2Dh
SSC Receive	SCRIR	SCRIE	SCRINT	00'00B8h	2Eh
SSC Error	SCEIR	SCEIE	SCEINT	00'00BCh	2Fh
PWM Channel 0...3	PWMIR	PWMIE	PWMINT	00'00FCh	3Fh
CAN Interface	XP0IR	XP0IE	XP0INT	00'0100h	40h
X-Peripheral Node	XP1IR	XP1IE	XP1INT	00'0104h	41h
X-Peripheral Node	XP2IR	XP2IE	XP2INT	00'0108h	42h
PLL Unlock	XP3IR	XP3IE	XP3INT	00'010Ch	43h

VII - INTERRUPT SYSTEM (continued)

Hardware traps are exceptions or error conditions that arise during run-time. They cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location).

The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag regis-

ter (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 3 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 3 : Exceptions or error conditions that can arise during run time

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:					
Hardware Reset		RESET	00'0000h	00h	III
Software Reset		RESET	00'0000h	00h	III
Watchdog Timer Overflow		RESET	00'0000h	00h	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	00'0008h	02h	II
Stack Overflow	STKOF	STOTRAP	00'0010h	04h	II
Stack Underflow	STKUF	STUTRAP	00'0018h	06h	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	00'0028h	0Ah	I
Protected Instruction Fault	PRTFLT	BTRAP	00'0028h	0Ah	I
Illegal Word Operand	ILLOPA	BTRAP	00'0028h	0Ah	I
Access	ILLINA	BTRAP	00'0028h	0Ah	I
Illegal Instruction Access	ILLBUS	BTRAP	00'0028h	0Ah	I
Illegal External Bus Access					
Reserved			[2Ch –3Ch]	[0Bh – 0Fh]	
Software Traps					
TRAP Instruction			Any [00'0000h– 00'01FCh] in steps of 4h	Any [00h – 7Fh]	Current CPU Priority

VIII - CAPTURE/COMPARE (CAPCOM) UNIT

The ST10R167 has two 16 channel CAPCOM units. They support generation and control of timing sequences on up to 32 channels with a maximum resolution of 320ns at 25MHz CPU clock. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Each of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare functions. Each register has one associated port pin which serves as an input pin

for triggering the capture function, or as an output pin (except for CC24...CC27) to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (captured) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode (see Table 4).

The input frequencies f_{Tx} for Tx are determined as a function of the CPU clocks. The formulas are detailed in the user manual. The timer input frequencies, resolution and periods which result from the selected pre-scaler option in TxI when using a 25MHz CPU clock are listed in the table below. The numbers for the timer periods are based on a reload value of 0000_H. Note that some numbers may be rounded to 3 significant figures (see Table 5).

Table 4 : Compare modes

Compare Modes	Function
Mode 0	Interrupt-only compare mode ; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match ; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode ; only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare time overflow ; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match ; several compare events per timer period are possible.

Table 5 : CAPCOM timer input frequencies, resolution and periods

$f_{CPU} = 25MHz$	Timer Input Selection TxI							
	000 _B	001 _B	010 _B	011 _B	100 _B	101 _B	110 _B	111 _B
Pre-scaler for f_{CPU}	8	16	32	64	128	256	512	1024
Input Frequency	3.125MHz	1.56MHz	781KHz	391KHz	195KHz	97.7KHz	48.8KHz	24.4KHz
Resolution	320ns	640ns	1.28 μ s	2.56 μ s	5.12 μ s	10.24 μ s	20.48 μ s	40.96 μ s
Period	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s	2.68s

IX - GENERAL PURPOSE TIMER UNIT

The GPT unit is a flexible multifunctional timer/counter structure which is used for time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. The GPT unit contains five 16-bit timers organized into two separate modules GPT1 and GPT2. Each timer in each module may operate independently in several different modes, or may be concatenated with another timer of the same module.

IX.1 - GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer, gated timer, counter mode and incremental interface mode**. In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. In counter mode, the timer is clocked in reference to external events. Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which is the gate or the clock input.

The table below lists the timer input frequencies, resolution and periods for each pre-scaler option at 25MHz CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode (see Table 6).

The count direction (up/down) for each timer is programmable by software or may additionally be

altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow/underflow. The state of this latch may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for high resolution measurement of long time periods.

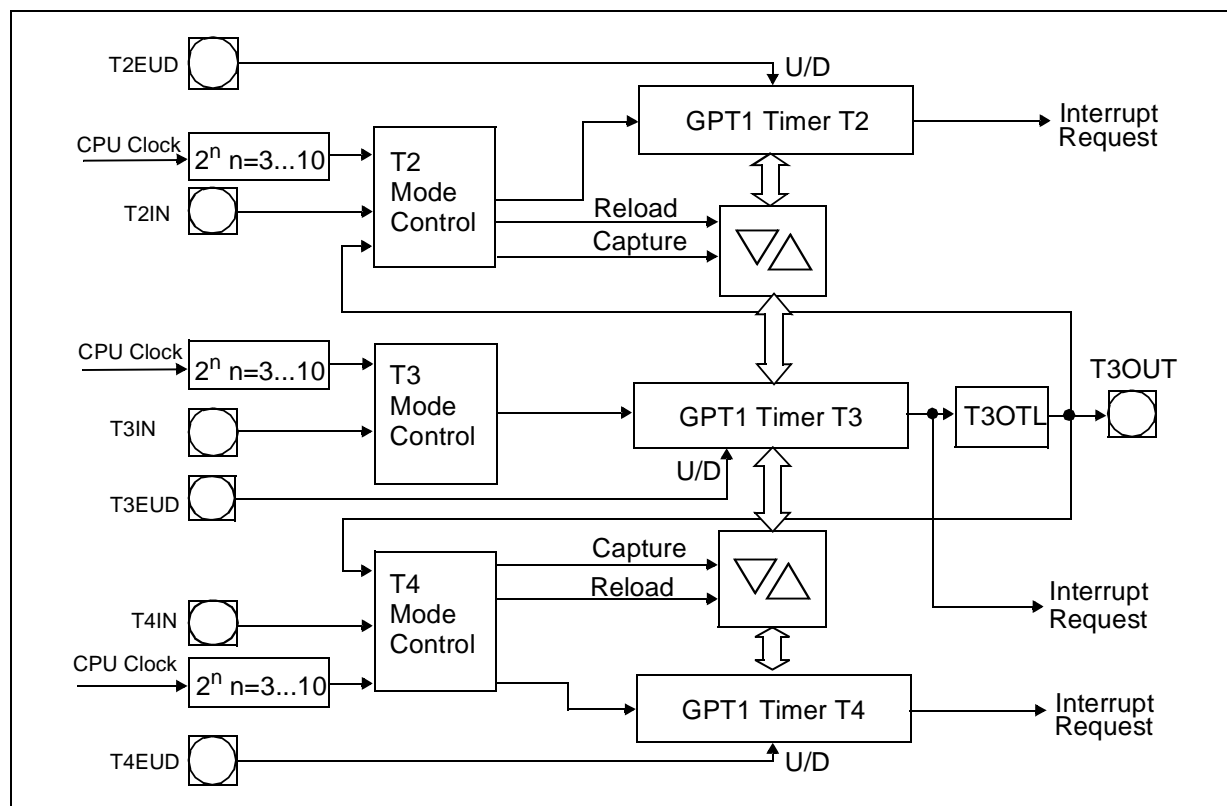
In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

Table 6 : GPT1 timer input frequencies, resolution and periods

$f_{CPU} = 25MHz$	Timer Input Selection T2I / T3I / T4I							
	000 _B	001 _B	010 _B	011 _B	100 _B	101 _B	110 _B	111 _B
Pre-scaler factor	8	16	32	64	128	256	512	1024
Input Frequency	3.125MHz	1.563MHz	781.3KHz	390.6KHz	195.3KHz	97.66KHz	48.83KHz	24.41KHz
Resolution	320ns	640ns	1.28 μ s	2.56 μ s	5.12 μ s	10.24 μ s	20.48 μ s	40.96 μ s
Period	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s	2.68s

IX - GENERAL PURPOSE TIMER UNIT (continued)

Figure 5 : Block diagram of GPT1



IX.2 - GPT2

The GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6 which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is advantageous when T3 operates in Incremental Interface Mode.

Table 7 lists the timer input frequencies, resolution and periods for each pre-scaler option at 25MHz CPU clock.

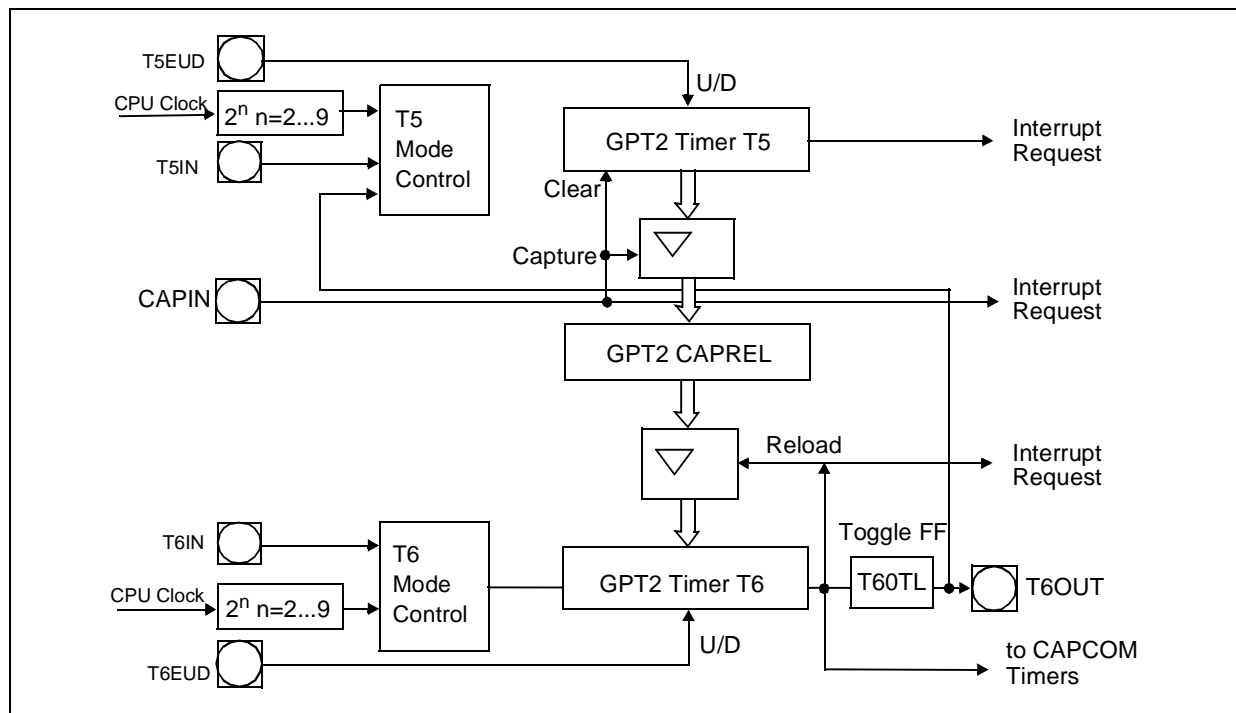
This also applies to the Gated Timer Mode of T6 and to the auxiliary timer T5 in Timer and Gated Timer Mode.

IX - GENERAL PURPOSE TIMER UNIT (continued)

Table 7 : GPT2 timer input frequencies, resolution and periods

f _{CPU} = 25MHz	Timer Input Selection T5I / T6I							
	000B	001B	010B	011B	100B	101B	110B	111B
Pre-scaler factor	4	8	16	32	64	128	256	512
Input Frequency	6.25MHz	3.125MHz	1.563MHz	781.3KHz	390.6KHz	195.3KHz	97.66KHz	48.83KHz
Resolution	160ns	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs
Period	10.49ms	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s

Figure 6 : Block diagram of GPT2



X - PWM MODULE

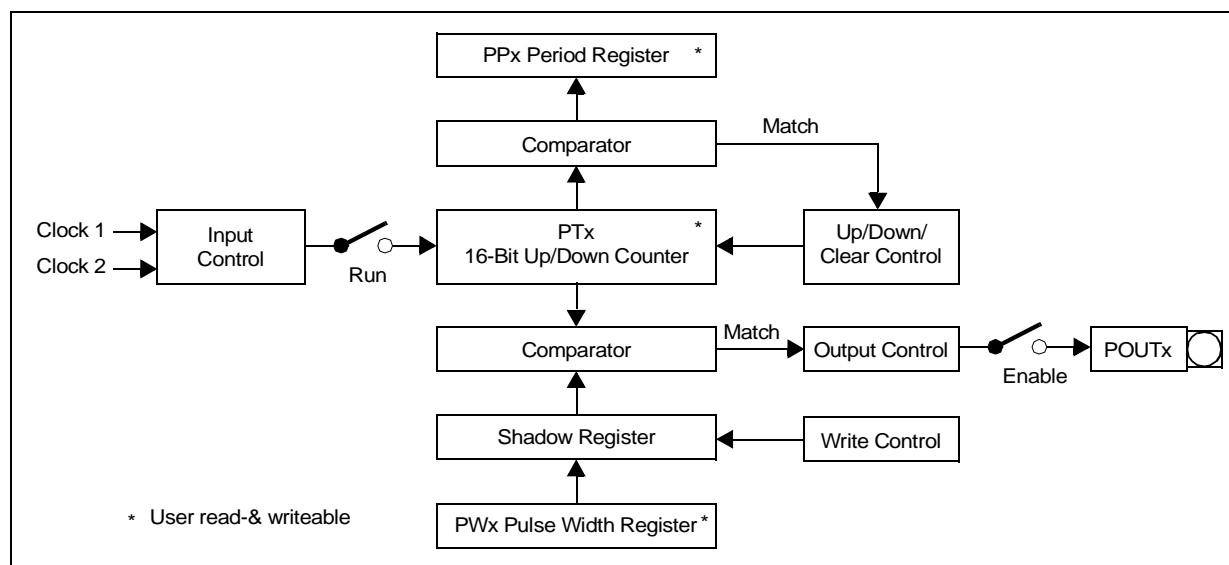
The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and sin-

gle shot outputs. Table 8 shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

Table 8 : PWM unit frequencies and resolution at 25MHz clock

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	40ns	97.66KHz	24.41KHz	6.104KHz	1.526KHz	0.381KHz
CPU Clock/64	2.56ns	1.526KHz	381.5Hz	95.37Hz	23.84Hz	5.96Hz
Mode 1	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	40ns	48.82KHz	12.20KHz	3.05KHz	762.9Hz	190.7Hz
CPU Clock/64	2.56ns	762.9Hz	190.7 Hz	47.68Hz	11.92Hz	2.98Hz

Figure 7 : Block diagram of PWM module



XI - PARALLEL PORTS

The ST10R167 provides up to 111 I/O lines organized into eight input/output ports and one input port.

All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as input or output via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs.

The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7 and Port 8 is selectable (TTL-or CMOS-like), where the special CMOS-like input threshold reduces noise sensitivity due to the input hysteresis.

The input thresholds are selected with bit of PICON register dedicated to blocks of 8 input pins (2-bit for port2, 2-bit for port3, 1-bit for port7, 1-bit for port8).

All pins of I/O ports also support an alternate programmable function:

- Port0 and Port1 may be used as address and data lines when accessing external memory.
- Port 2, Port 7 and Port 8 are associated with the capture inputs or with the compare outputs of the CAPCOM units and/or with the outputs of the PWM module.
- Port 3 includes the alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$ and the system clock output (CLKOUT).
- Port 4 outputs the additional segment address bits A16 to A23 in systems where segmentation is enabled to access more than 64K Byte of memory.
- Port 5 is used as analog input channels of the A/D converter or as timer control signals.
- Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

XII - A/D CONVERTER

A10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit is integrated on-chip. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry. Overrun error detection/protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins. The AD converter of the ST10F168 supports different conversion modes :

- **Single channel single conversion** : the analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.
- **Single channel continuous conversion** : the analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.
- **Auto scan single conversion** : the analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transferred to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.
- **Auto scan continuous conversion** : the analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register. The data can be transferred to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.
- **Wait for ADDAT read mode** : when using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register

must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.

- **Channel injection mode** : when using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10 bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed.

The Table : 9 ADC sample clock and conversion time shows the ADC unit conversion clock, sample clock.

A complete conversion will take $14t_{CC} + 2 t_{SC} + 4 TCL$. This time includes the conversion it-self, the sampling time and the time required to transfer the digital value to the result register. For example, at 25MHz of CPU clock, minimum complete conversion time is 7.76 μ s.

The A/D converter provides automatic offset and linearity self calibration. The calibration operation is performed in two ways:

- A full calibration sequence is performed after a reset and lasts 1.6ms minimum (at 25MHz CPU clock). During this time, the ADBSY flag is set to indicate the operation. Normal conversion can be performed during this time. The duration of the calibration sequence is then extended by the time consumed by the conversions.

Note : After a power-on reset, the total unadjusted error (TUE) of the ADC might be worse than $\pm 2LSB$ (max. $\pm 4LSB$). During the full calibration sequence, the TUE is constantly improved until at the end of the cycle, TUE is within the specified limits of $\pm 2LSB$.

- One calibration cycle is performed after each conversion : each calibration cycle takes 4 ADC clock cycles. These operation cycles ensure constant updating of the ADC accuracy, compensating changing operating conditions.

Table 9 : ADC sample clock and conversion time

ADCTC	Conversion Clock t_{CC}		ADSTC	Sample Clock t_{SC}	
	$TCL^1 = 1/2 \times f_{XTAL}$	At $f_{CPU} = 25MHz$		-	At $f_{CPU} = 25MHz$
00	$TCL \times 24$	0.48 μ s	00	t_{CC}	0.48 μ s ²
01	Reserved, do not use	-	01	$t_{CC} \times 2$	0.96 μ s ²
10	$TCL \times 96$	1.92 μ s	10	$t_{CC} \times 4$	1.92 μ s ²
11	$TCL \times 48$	0.96 μ s	11	$t_{CC} \times 8$	3.84 μ s ²

Note 1. See chapter XX.
2. $t_{CC} = TCL \times 24$.

XIII - SERIAL CHANNELS

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces: the asynchronous/synchronous serial channel (ASCO) and the high-speed synchronous serial channel (SSC).

Two dedicated Baud rate generators set up all standard Baud rates without the requirement of oscillator tuning.

For transmission, reception and erroneous reception, 3 separate interrupt vectors are provided for each serial channel.

ASCO

ASCO supports full-duplex asynchronous communication up to 781.25K Baud and half-duplex synchronous communication up to 5M Baud at 25MHz system clock. For asynchronous operation, the Baud rate generator provides a clock with 16 times the rate of the established Baud rate.

The table below lists various commonly used Baud rates together with the required reload values and the deviation errors compared to the intended Baud rate (see Table 10).

For synchronous operation, the Baud rate generator provides a clock with 4 times the rate of the established Baud rate.

Table 10 : Commonly used Baud rates by reload value and deviation errors

S0BRS = '0', f _{CPU} = 25MHz			S0BRS = '1', f _{CPU} = 25MHz		
Baud Rate (Baud)	Deviation Error	Reload Value	Baud Rate (Baud)	Deviation Error	Reload Value
781250	±0.0%	0000 _H	520833	±0.0%	0000 _H
56000	+7.3% / -0.4%	000C _H / 000D _H	56000	+3.3% / -7.0%	0008 _H / 0009 _H
38400	+1.7% / -3.1%	0013 _H / 0014 _H	38400	+4.3% / -3.1%	000C _H / 000D _H
19200	+1.7% / -0.8%	0027 _H / 0028 _H	19200	+0.5% / -3.1%	001A _H / 001B _H
9600	+0.5% / -0.8%	0050 _H / 0051 _H	9600	+0.5% / -1.4%	0035 _H / 0036 _H
4800	+0.5% / -0.1%	00A1 _H / 00A2 _H	4800	+0.5% / -0.5%	006B _H / 006C _H
2400	+0.2% / -0.1%	0144 _H / 0145 _H	2400	+0.0% / -0.5%	00D8 _H / 00D9 _H
1200	+0.0% / -0.1%	028A _H / 028B _H	1200	+0.0% / -0.2%	01B1 _H / 01B2 _H
600	+0.0% / -0.1%	0515 _H / 0516 _H	600	+0.0% / -0.1%	0363 _H / 0364 _H
95	+0.4% / 0.4%	1FFF _H / 1FFF _H	75	+0.0% / 0.0%	1B1F _H / 1B20 _H
			63	+0.9% / 0.9%	1FFF _H / 1FFF _H

Note The deviation errors given in the table above are rounded. Using a Baud rate crystal will provide correct Baud rates without deviation errors.

XIII - SERIAL CHANNELS (continued)**High Speed Synchronous Serial Channel (SSC)**

The High-Speed Synchronous Serial Interface SSC provides flexible high-speed serial communication between the ST10R167 and other microcontrollers, microprocessors or external peripherals.

The SSC supports full-duplex and half-duplex synchronous communication; The serial clock signal can be generated by the SSC itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows

communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A 16-bit Baud rate generator provides the SSC with a separate serial clock signal. The serial channel SSC has its own dedicated 16-bit Baud rate generator with 16-bit reload capability, allowing Baud rate generation independent from the timers.

SSCBR is the dual-function Baud Rate Generator/Reload register. Table 11 lists some possible Baud rates against the required reload values and the resulting bit times for a 25MHz CPU clock.

Table 11 : Synchronous Baud rate and reload values

Baud Rate	Bit Time	Reload Value
Reserved use a reload value > 0.	---	0000 _H
5M Baud	200ns	0001 _H
3.3M Baud	303ns	0002 _H
2.5M Baud	400ns	0004 _H
2M Baud	500ns	0005 _H
1M Baud	1μs	000B _H
100K Baud	10μs	007C _H
10K Baud	100μs	04E1 _H
1K Baud	1ms	30D3 _H
190.7 Baud	5.2ms	FFFF _H