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## GENERAL DESCRIPTION

The ST16C654/654D[1] (654) is an enhanced quad Universal Asynchronous Receiver and Transmitter (UART) each with 64 bytes of transmit and receive FIFOs, transmit and receive FIFO trigger levels, automatic hardware and software flow control, and data rates of up to 1.5 Mbps. Each UART has a set of registers that provide the user with operating status and control, receiver error indications, and modem serial interface controls. Selectable interrupt polarity provides flexibility to meet design requirements. An internal loopback capability allows onboard diagnostics. The 654 is available in 64 pin LQFP, 68 pin PLCC and 100 pin QFP packages. The 64 pin package only offers the 16 mode interface, but the 68 and 100 pin packages offer an additional 68 mode interface which allows easy integration with Motorola processors. The ST16C654CQ64 (64 pin) offers three state interrupt output while the ST16C654DCQ64 provides continuous interrupt output. The 100 pin package provides additional FIFO status outputs (TXRDY# and RXRDY# A-D), separate infrared transmit data outputs (IRTX A-D) and channel C external clock input (CHCCLK). The ST16C654/654D is compatible with the industry standard ST16C454 and ST16C654/554D.

***NOTE:*** *1 Covered by U.S. Patent #5,649,122.*

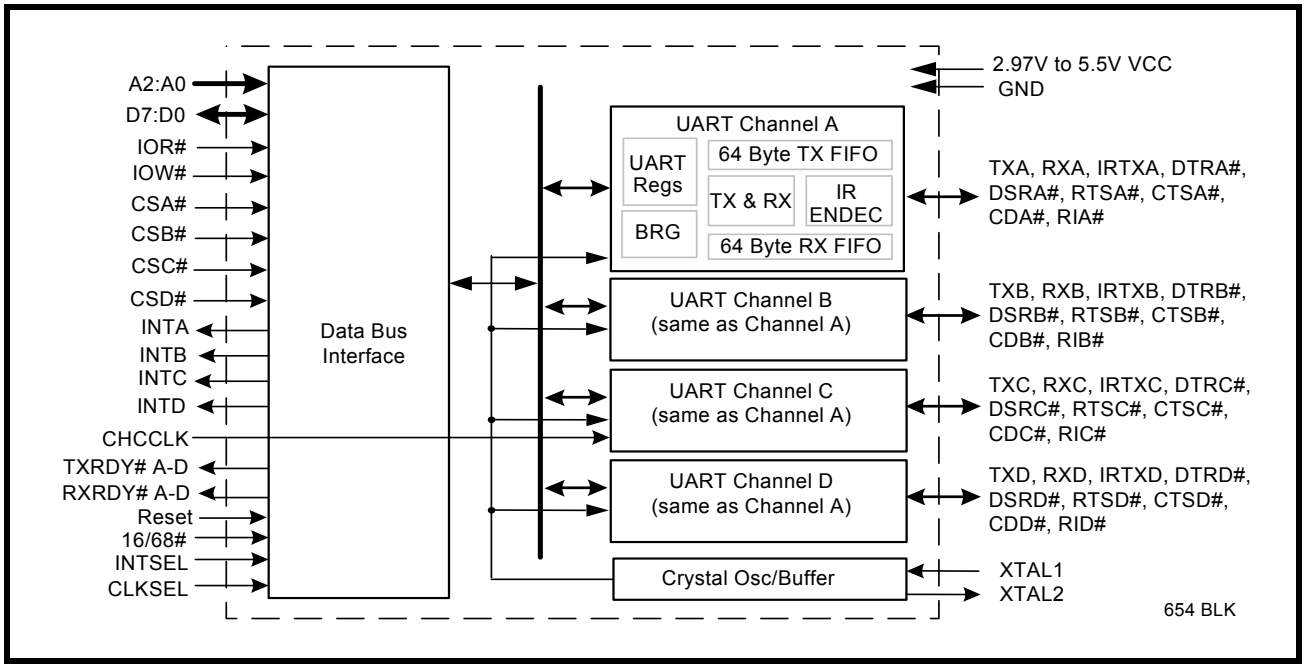
### *FEATURES*

- Pin-to-pin compatible with ST16C454, ST16C554 and TI's TL16C554AFN and TL16C754BFN
- Intel or Motorola Data Bus Interface select
- Four independent UART channels
  - Register Set Compatible to 16C550
  - Data rates of up to 1.5 Mbps
  - 64 Byte Transmit FIFO
  - 64 Byte Receive FIFO with error tags
  - 4 Selectable TX and RX FIFO Trigger Levels
  - Automatic Hardware (RTS/CTS) Flow Control
  - Automatic Software (Xon/Xoff) Flow Control
  - Progammable Xon/Xoff characters
  - Wireless Infrared (IrDA 1.0) Encoder/Decoder
  - Full modem interface
- 2.97V to 5.5V supply operation
- Sleep Mode (200 uA typical)
- Crystal oscillator or external clock input

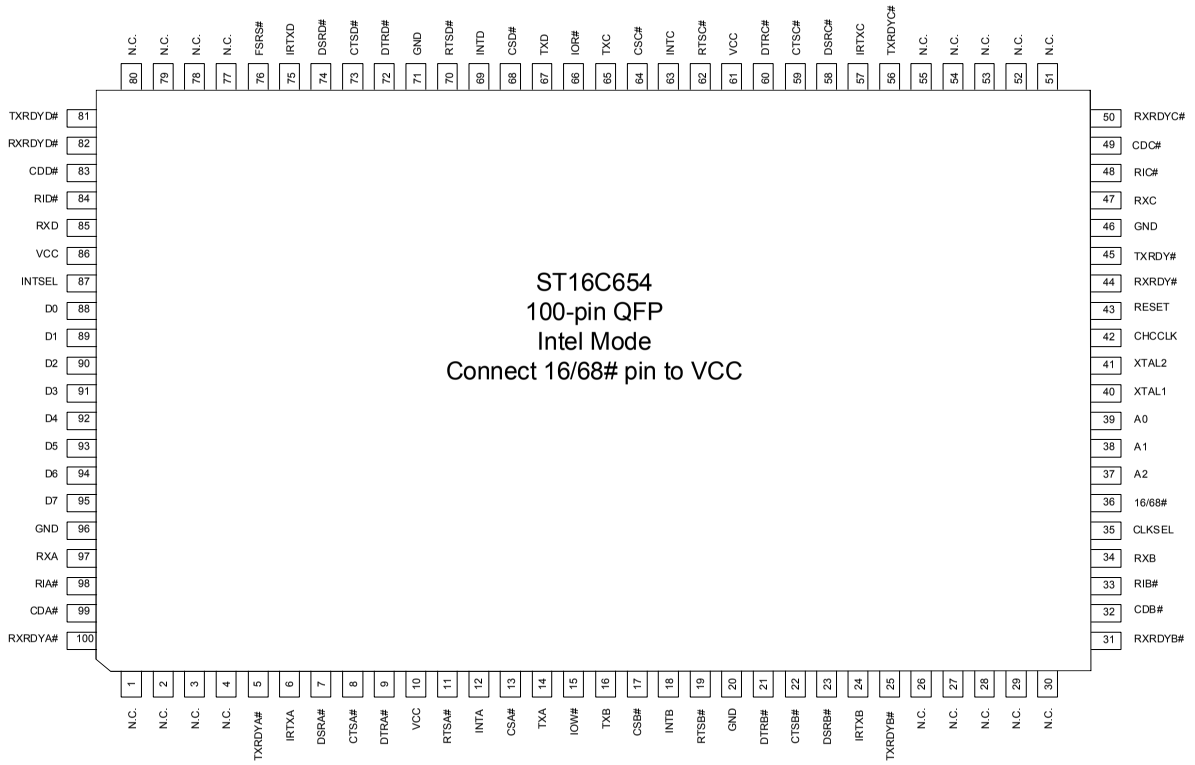
### *APPLICATIONS*

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

**FIGURE 1. ST16C654 BLOCK DIAGRAM**



## FIGURE 2. PIN OUT ASSIGNMENT FOR 100-PIN QFP PACKAGES IN 16 AND 68 MODE



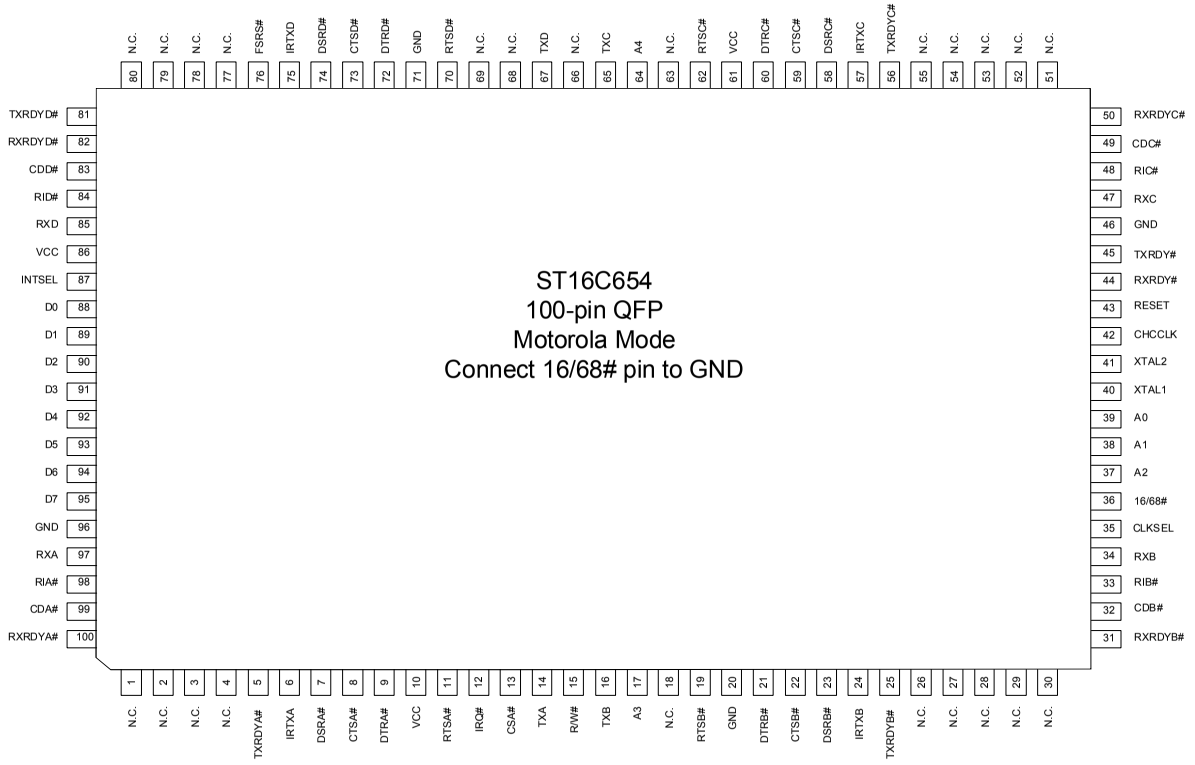
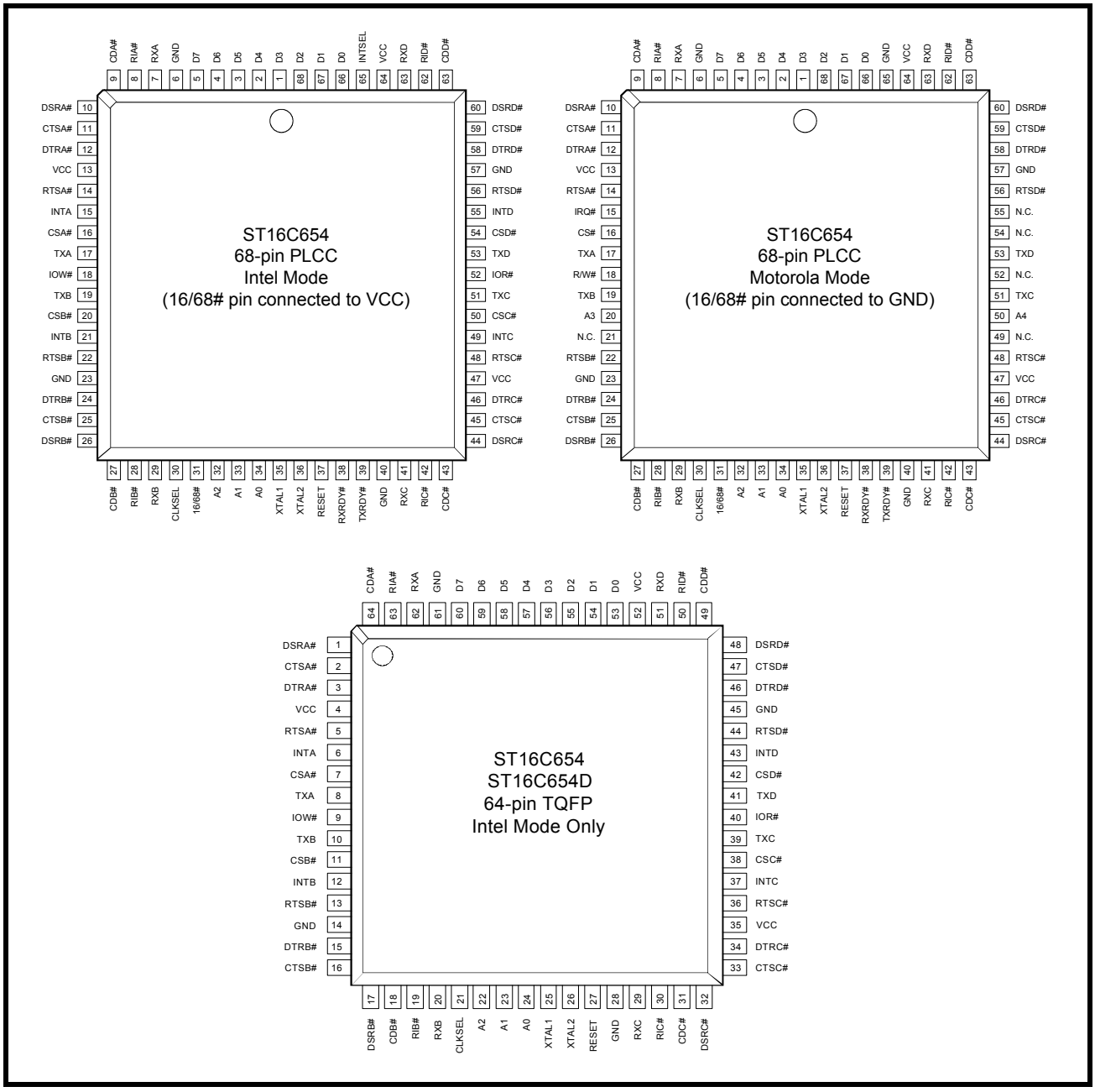



**FIGURE 3. PIN OUT ASSIGNMENT FOR PLCC PACKAGES IN 16 AND 68 MODE AND LQFP PACKAGES**




***ORDERING INFORMATION***

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE | DEVICE STATUS | PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE | DEVICE STATUS |
|---|---|---|---|---|---|---|---|
| ST16C654CJ68 | 68-Lead PLCC | 0°C to +70°C | Active | ST16C654DCQ64 | 64-Lead LQFP | 0°C to +70°C | Active |
| ST16C654IJ68 | 68-Lead PLCC | -40°C to +85°C | Active | ST16C654DIQ64 | 64-Lead LQFP | -40°C to +85°C | Active |
| ST16C654CQ64 | 64-Lead LQFP | 0°C to +70°C | Active | ST16C654CQ100 | 100-Lead QFP | 0°C to +70°C | Active |
| ST16C654IQ64 | 64-Lead LQFP | -40°C to +85°C | Active | ST16C654IQ100 | 100-Lead QFP | -40°C to +85°C | Active |

# PIN DESCRIPTIONS

## Pin Description

| NAME | 64-LQFP PIN # | 68-PLCC PIN# | 100-QFP PIN # | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| **DATA BUS INTERFACE** | | | | | |
| A2<br>A1<br>A0 | 22<br>23<br>24 | 32<br>33<br>34 | 37<br>38<br>39 | I | Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A-D during a data bus transaction. |
| D7<br>D6<br>D5<br>D4<br>D3<br>D2<br>D1<br>D0 | 60<br>59<br>58<br>57<br>56<br>55<br>54<br>53 | 5<br>4<br>3<br>2<br>1<br>68<br>67<br>66 | 95<br>94<br>93<br>92<br>91<br>90<br>89<br>88 | I/O | Data bus lines [7:0] (bidirectional). |
| IOR#<br>(VCC) | 40 | 52 | 66 | I | When 16/68# pin is at logic 1, the Intel bus interface is selected and this input becomes read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge.<br>When 16/68# pin is at logic 0, the Motorola bus interface is selected and this input is not used and should be connected to VCC. |
| IOW#<br>(R/W#) | 9 | 18 | 15 | I | When 16/68# pin is at logic 1, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines.<br>When 16/68# pin is at logic 0, the Motorola bus interface is selected and this input becomes read (logic 1) and write (logic 0) signal. |
| CSA#<br>(CS#) | 7 | 16 | 13 | I | When 16/68# pin is at logic 1, this input is chip select A (active low) to enable channel A in the device.<br>When 16/68# pin is at logic 0, this input becomes the chip select (active low) for the Motorola bus interface. |
| CSB#<br>(A3) | 11 | 20 | 17 | I | When 16/68# pin is at logic 1, this input is chip select B (active low) to enable channel B in the device.<br>When 16/68# pin is at logic 0, this input becomes address line A3 which is used for channel selection in the Motorola bus interface. |
| CSC#<br>(A4) | 38 | 50 | 64 | I | When 16/68# pin is at logic 1, this input is chip select C (active low) to enable channel C in the device.<br>When 16/68# pin is at logic 0, this input becomes address line A4 which is used for channel selection in the Motorola bus interface. |
| CSD#<br>(VCC) | 42 | 54 | 68 | I | When 16/68# pin is at logic 1, this input is chip select D (active low) to enable channel D in the device.<br>When 16/68# pin is at logic 0, this input is not used and should be connected VCC. |

## Pin Description

| NAME | 64-LQFP PIN # | 68-PLCC PIN# | 100-QFP PIN # | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| INTA (IRQ#) | 6 | 15 | 12 | O (OD) | When 16/68# pin is at logic 1 for Intel bus interface, this ouput becomes channel A interrupt output. The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode when MCR[3] is set to a logic 1. INTA is set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3].<br>When 16/68# pin is at logic 0 for Motorola bus interface, this output becomes device interrupt output (active low, open drain). An external pull-up resistor is required for proper operation. |
| INTB<br>INTC<br>INTD<br>(N.C.) | 12<br>37<br>43 | 21<br>49<br>55 | 18<br>63<br>69 | O | When 16/68# pin is at logic 1 for Intel bus interface, these ouputs become the interrupt outputs for channels B, C, and D. The output state is defined by the user through the software setting of MCR[3]. The interrupt outputs are set to the active mode when MCR[3] is set to a logic 1 and are set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3].<br>When 16/68# pin is at logic 0 for Motorola bus interface, these outputs are unused and will stay at logic zero level. Leave these outputs unconnected. |
| INTSEL | - | 65 | 87 | I | Interrupt Select (active high, input with internal pull-down).<br>When 16/68# pin is at logic 1 for Intel bus interface, this pin can be used in conjunction with MCR bit-3 to enable or disable the INT A-D pins or override MCR bit-3 and enable the interrupt outputs. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR bit-3 to enable and disable the interrupt output pins. In this mode, MCR bit-3 is set to a logic 1 to enable the continuous output. See MCR bit-3 description for full detail. This pin must be at logic 0 in the Motorola bus interface mode. Due to pin limitations on 64 pin packages, this pin is not available. To cover this limitation, two 64 pin LQFP packages versions are offered. This pin is bonded to VCC internally in the ST16C654D so the INT outputs operate in the continuous interrupt mode. This pin is bonded to GND internally in the ST16C654 and therefore requires setting MCR bit-3 for enabling the interrupt output pins. |
| TXRDYA#<br>TXRDYB#<br>TXRDYC#<br>TXRDYD# | -<br>-<br>-<br>- | -<br>-<br>-<br>- | 5<br>25<br>56<br>81 | O | UART channels A-D Transmitter Ready (active low). The outputs provide the TX FIFO/THR status for transmit channels A-D. See Table 5. If these outputs are unused, leave them unconnected. |
| RXRDYA#<br>RXRDYB#<br>RXRDYC#<br>RXRDYD# | -<br>-<br>-<br>- | -<br>-<br>-<br>- | 100<br>31<br>50<br>82 | O | UART channels A-D Receiver Ready (active low). This output provides the RX FIFO/RHR status for receive channels A-D. See Table 5. If these outputs are unused, leave them unconnected. |
| TXRDY# | - | 39 | 45 | O | Transmitter Ready (active low). This output is a logically ANDed status of TXRDY# A-D. See Table 5. If this output is unused, leave it unconnected. |
| RXRDY# | - | 38 | 44 | O | Receiver Ready (active low). This output is a logically ANDed status of RXRDY# A-D. See Table 5. If this output is unused, leave it unconnected. |

## Pin Description

| NAME | 64-LQFP PIN # | 68-PLCC PIN# | 100-QFP PIN # | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| FSRS# | - | - | 76 | I | FIFO Status Register Select (active low input with internal pull-up). The content of the FSTAT register is placed on the data bus when this pin becomes active. However it should be noted, D0-D3 contain the inverted logic states of TXRDY# A-D pins, and D4-D7 the logic states (un-inverted) of RXRDY# A-D pins. A valid address is not required when reading this status register. |
| **MODEM OR SERIAL I/O INTERFACE** | | | | | |
| TXA<br>TXB<br>TXC<br>TXD | 8<br>10<br>39<br>41 | 17<br>19<br>51<br>53 | 14<br>16<br>65<br>67 | O | UART channels A-D Transmit Data and infrared transmit data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be a logic 1 during reset, or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is a logic 0. |
| IRTXA<br>IRTXB<br>IRTXC<br>IRTXD | -<br>-<br>-<br>- | -<br>-<br>-<br>- | 6<br>24<br>57<br>75 | O | UART channel A-D Infrared Transmit Data. The inactive state (no data) for the Infrared encoder/decoder interface is a logic 0. Regardless of the logic state of MCR bit-6, this pin will be operating in the Infrared mode. |
| RXA<br>RXB<br>RXC<br>RXD | 62<br>20<br>29<br>51 | 7<br>29<br>41<br>63 | 97<br>34<br>47<br>85 | I | UART channel A-D Receive Data or infrared receive data. Normal receive data input must idle at logic 1 condition. |
| RTSA#<br>RTSB#<br>RTSC#<br>RTSD# | 5<br>13<br>36<br>44 | 14<br>22<br>48<br>56 | 11<br>19<br>62<br>70 | O | UART channels A-D Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], and IER[6]. Also see Figure 11. If these outputs are not used, leave them unconnected. |
| CTSA#<br>CTSB#<br>CTSC#<br>CTSD# | 2<br>16<br>33<br>47 | 11<br>25<br>45<br>59 | 8<br>22<br>59<br>73 | I | UART channels A-D Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. Also see Figure 11. These inputs should be connected to VCC when not used. |
| DTRA#<br>DTRB#<br>DTRC#<br>DTRD# | 3<br>15<br>34<br>46 | 12<br>24<br>46<br>58 | 9<br>21<br>60<br>72 | O | UART channels A-D Data-Terminal-Ready (active low) or general purpose output. If these outputs are not used, leave them unconnected. |
| DSRA#<br>DSRB#<br>DSRC#<br>DSRD# | 1<br>17<br>32<br>48 | 10<br>26<br>44<br>60 | 7<br>23<br>58<br>74 | I | UART channels A-D Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| CDA#<br>CDB#<br>CDC#<br>CDD# | 64<br>18<br>31<br>49 | 9<br>27<br>43<br>61 | 99<br>32<br>49<br>83 | I | UART channels A-D Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |

## Pin Description

| NAME | 64-LQFP PIN # | 68-PLCC PIN# | 100-QFP PIN # | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| RIA#<br>RIB#<br>RIC#<br>RID# | 63<br>19<br>30<br>50 | 8<br>28<br>42<br>62 | 98<br>33<br>48<br>84 | I | UART channels A-D Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| **ANCILLARY SIGNALS** | | | | | |
| XTAL1 | 25 | 35 | 40 | I | Crystal or external clock input. |
| XTAL2 | 26 | 36 | 41 | O | Crystal or buffered clock output. |
| 16/68# | - | 31 | 36 | I | Intel or Motorola Bus Select (input with internal pull-up).<br>When 16/68# pin is at logic 1, 16 or Intel Mode, the device will operate in the Intel bus type of interface.<br>When 16/68# pin is at logic 0, 68 or Motorola mode, the device will operate in the Motorola bus type of interface.<br>Motorola bus interface is not available on the 64 pin package. |
| CLKSEL | 21 | 30 | 35 | I | Baud-Rate-Generator Input Clock Prescaler Select for channels A-D. This input is only sampled during power up or a reset. Connect to VCC for divide by 1 (default) and GND for divide by 4. MCR[7] can override the state of this pin following a reset or initialization. See MCR bit-7 and Figure 6 in the Baud Rate Generator section. |
| CHCCLK | - | - | 42 | I | This input provides the clock for UART channel C. An external 16X baud clock or the crystal oscillator's output, XTAL2, must be connected to this pin for normal operation. This input may also be used with MIDI (Musical Instrument Digital Interface) applications when an external MIDI clock is provided. This pin is only available in the 100-pin QFP package. |
| RESET (RESET#) | 27 | 37 | 43 | I | When 16/68# pin is at logic 1 for Intel bus interface, this input becomes the Reset pin (active high). In this case, a 40 ns minimum logic 1 pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held at logic 1, the receiver input will be ignored and outputs are reset during reset period (Table 16). When 16/68# pin is at a logic 0 for Motorola bus interface, this input becomes Reset# pin (active low). This pin functions similarly, but instead of a logic 1 pulse, a 40 ns minimum logic 0 pulse will reset the internal registers and outputs.<br>Motorola bus interface is not available on the 64 pin package. |
| VCC | 4, 35, 52 | 13, 47, 64 | 10, 61, 86 | Pwr | 2.97V to 5.5V power supply. The inputs are not 5V tolerant when operating at 3.3V. |
| GND | 14, 28, 45, 61 | 6, 23, 40, 57 | 20, 46, 71, 96 | Pwr | Power supply common, ground. |
| N.C. | - | - | 1- 4, 26-28, 29, 30, 51-55, 77, 78, 79, 80 | | No Connection. These pins are not used in either the Intel or Motorola bus modes. These pins are open, but typically, should be connected to GND for good design practice. |

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

## 1.0 PRODUCT DESCRIPTION

The ST16C654 (654) integrates the functions of 4 enhanced 16C550 Universal Asynchrounous Receiver and Transmitter (UART). Each UART is independently controlled having its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 64-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 1.5 Mbps. The ST16C654 can operate from 2.97 to 5.5 volts. The 654 is fabricated with an advanced CMOS process.

### Enhanced FIFO

The 654 QUART provides a solution that supports 64 bytes of transmit and receive FIFO memory, instead of 16 bytes in the ST16C554, or one byte in the ST16C454. The 654 is designed to work with high performance data communication systems, that require fast data processing time. Increased performance is realized in the 654 by the larger transmit and receive FIFOs, FIFO trigger level control and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C554 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 64 byte FIFO in the 654, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

### Data Rate

The 654 is capable of operation up to 1.5 Mbps at 5V with 16x internal sampling clock rate. The device can operate at 5V with a crystal oscillator of up to 24 MHz crystal on pins XTAL1 and XTAL2, or external clock source of 24 MHz on XTAL1 pin. With a typical crystal of 14.7456 MHz and through a software option, the user can set the prescaler bit for data rates of up to 921.6 kbps.

### Enhanced Features

The rich feature set of the 654 is available through the internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. MCR bit-5 provides a facility for turning off (Xon) software flow control with any incoming (RX) character. In the 16 mode INTSEL and MCR bit-3 can be configured to provide a software controlled or continuous interrupt capability. Due to pin limitations for the 64 pin 654 this feature is offered by two different LQFP packages. The ST16C654DCV operates in the continuous interrupt enable mode by internally bonding INTSEL to VCC. The ST16C654CV operates in conjunction with MCR bit-3 by internally bonding INTSEL to GND.

The ST16C654 offers a clock prescaler select pin to allow system/board designers to preset the default baud rate table on power up. The CLKSEL pin selects the div-by-1 or div-by-4 prescaler for the baud rate generator. It can then be overridden following initialization by MCR bit-7.

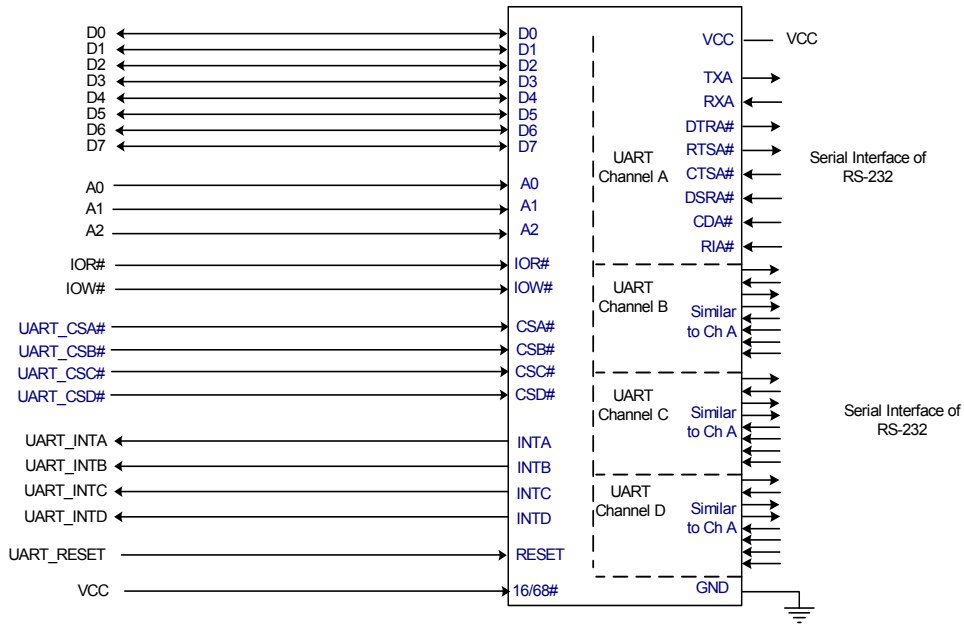
The 100 pin packages offer several other enhanced features. These features include a CHCCLK clock input, FSTAT register and separate IrDA TX outputs. The CHCCLK must be connected to the XTAL2 pin for normal operation or to external MIDI (Music Instrument Digital Interface) oscillator for MIDI applications. A separate register (FSTAT) is provided for monitoring the real time status of the FIFO signals TXRDY# and RXRDY# for each of the four UART channels (A-D). This reduces polling time involved in accessing individual channels. The 100 pin QFP package also offers four separate IrDA (Infrared Data Association Standard) TX outputs for Infrared applications. These outputs are provided in addition to the standard asynchronous modem data outputs.

## 2.0 FUNCTIONAL DESCRIPTIONS

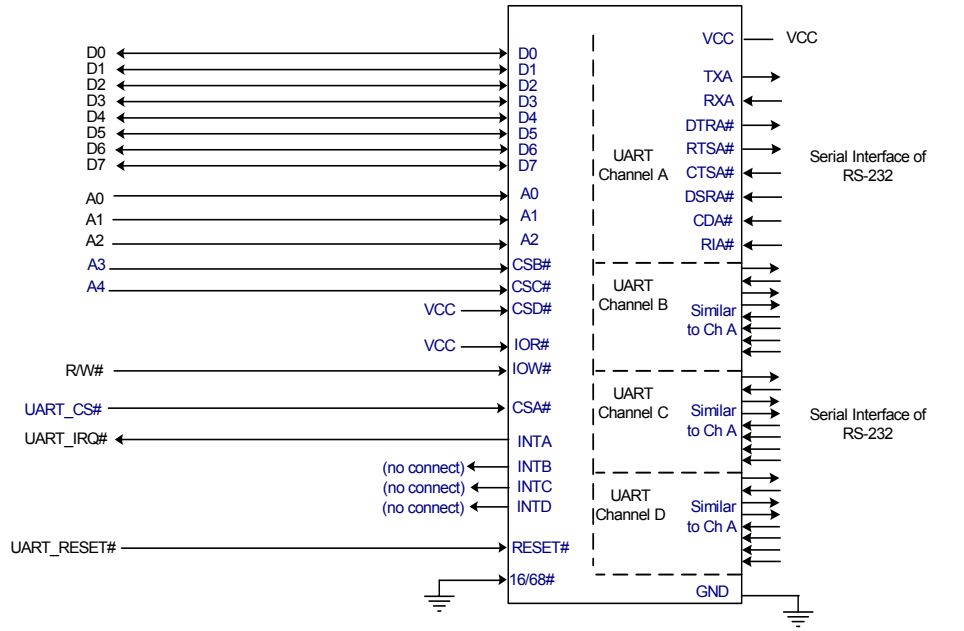
### 2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The 654 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS# A-D, IOR# and IOW# or CS#, R/W#, A4 and A3 inputs. All four UART channels share the same data bus for host operations. A typical data bus interconnection for Intel and Motorola mode is shown in Figure 4.

**FIGURE 4. ST16C654/654D TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS**




**Intel Data Bus (16 Mode) Interconnections**




**Motorola Data Bus (68 Mode) Interconnections**

### 2.2 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 16). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device. Following a power-on reset or an external reset, the 654 is software compatible with previous generation of UARTs, 16C454 and 16C554.

### 2.3 Channel Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. During Intel Bus Mode (16/68# pin is connected to VCC), a logic 0 on chip select pins, CSA#, CSB#, CSC# or CSD# allows the user to select UART channel A, B, C or D to configure, send transmit data and/or unload receive data to/from the UART. Selecting all four UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from all four uarts simultaneously. Individual channel select functions are shown in Table 1.

**TABLE 1: CHANNEL A-D SELECT IN 16 MODE**

| CSA # | CSB # | CSC # | CSD # | FUNCTION |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | UART de-selected |
| 0 | 1 | 1 | 1 | Channel A selected |
| 1 | 0 | 1 | 1 | Channel B selected |
| 1 | 1 | 0 | 1 | Channel C selected |
| 1 | 1 | 1 | 0 | Channel D selected |
| 0 | 0 | 0 | 0 | Channels A-D selected |

During Motorola Bus Mode (16/68# pin is connected to GND), the package interface pins are configured for connection with Motorola, and other popular microprocessor bus types. In this mode the 654 decodes two additional addresses, A3 and A4, to select one of the four UART ports. The A3 and A4 address decode function is used only when in the Motorola Bus Mode. See Table 2.

**TABLE 2: CHANNEL A-D SELECT IN 68 MODE**

| CS# | A4 | A3 | FUNCTION |
|---|---|---|---|
| 1 | N/A | N/A | UART de-selected |
| 0 | 0 | 0 | Channel A selected |
| 0 | 0 | 1 | Channel B selected |
| 0 | 1 | 0 | Channel C selected |
| 0 | 1 | 1 | Channel D selected |

### 2.4 Channels A-D Internal Registers

Each UART channel in the 654 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scratchpad register (SPR).

Beyond the general 16C550 features and capabilities, the 654 offers enhanced feature registers (EFR, Xon/Xoff 1, Xon/Xoff 2, FSTAT) that provide automatic RTS and CTS hardware flow control and automatic Xon/Xoff software flow control. All the register functions are discussed in full detail later in "Section 3.0, UART INTERNAL REGISTERS" on page 22.

### 2.5 INT Ouputs for Channels A-D

The interrupt outputs change according to the operating mode and enhanced features setup. Table 3 and 4 summarize the operating behavior for the transmitter and receiver. Also see Figure 20 through 25.

**TABLE 3: INT PINS OPERATION FOR TRANSMITTER FOR CHANNELS A-D**

| | FCR BIT-0 = 0 (FIFO DISABLED) | FCR BIT-0 = 1 (FIFO ENABLED) | |
|---|---|---|---|
| | | FCR Bit-3 = 0 (DMA Mode Disabled) | FCR Bit-3 = 1 (DMA Mode Enabled) |
| INT Pin | 0 = a byte in THR<br>1 = THR empty | 0 = FIFO above trigger level<br>1 = FIFO below trigger level or FIFO empty | 0 = FIFO above trigger level<br>1 = FIFO below trigger level or FIFO empty |

**TABLE 4: INT PIN OPERATION FOR RECEIVER FOR CHANNELS A-D**

| | FCR BIT-0 = 0 (FIFO DISABLED) | FCR BIT-0 = 1 (FIFO ENABLED) | |
|---|---|---|---|
| | | FCR Bit-3 = 0 (DMA Mode Disabled) | FCR Bit-3 = 1 (DMA Mode Enabled) |
| INT Pin | 0 = no data<br>1 = 1 byte | 0 = FIFO below trigger level<br>1 = FIFO above trigger level | 0 = FIFO below trigger level<br>1 = FIFO above trigger level |

### 2.6 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document does not mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A-D and TXRDY# A-D output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFOs are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 654 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. The following table show their behavior. Also see Figure 20 through 25.

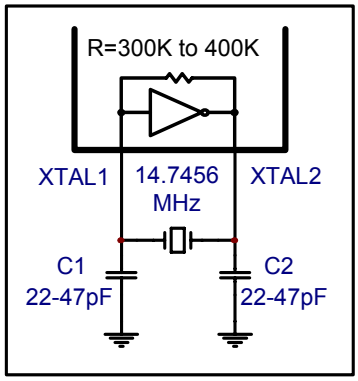
**TABLE 5: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE FOR CHANNELS A-D**

| PINS | FCR BIT-0=0 (FIFO DISABLED) | FCR BIT-0=1 (FIFO ENABLED) | |
|---|---|---|---|
| | | FCR BIT-3 = 0 (DMA MODE DISABLED) | FCR BIT-3 = 1 (DMA MODE ENABLED) |
| RXRDY# | 0 = 1 byte<br>1 = no data | 0 = at least 1 byte in FIFO<br>1 = FIFO empty | 1 to 0 transition when FIFO reaches the trigger level, or timeout occurs.<br>0 to 1 transition when FIFO empties. |
| TXRDY# | 0 = THR empty<br>1 = byte in THR | 0 = FIFO empty<br>1 = at least 1 byte in FIFO | 0 = FIFO has at least 1 empty location.<br>1 = FIFO is full. |

## 2.7 Crystal Oscillator or External Clock Input

The 654 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see "Section 2.8, Programmable Baud Rate Generator" on page 12

**FIGURE 5. TYPICAL OSCILLATOR CONNECTIONS**




The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins. Typical oscillator connections are shown in Figure 5. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

## 2.8 Programmable Baud Rate Generator

Each UART has its own Baud Rate Generator (BRG) with a prescaler. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and ($2^{16}$ -1) to obtain a 16X sampling rate clock of the serial data rate. The sampling rate clock is used by the transmitter for data bit shifting and receiver for data sampling.

**FIGURE 6. BAUD RATE GENERATOR AND PRESCALER**

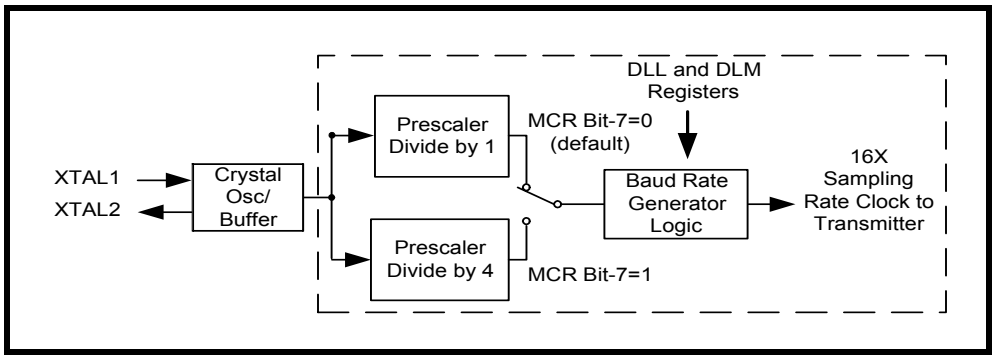



Table 6 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X sampling rate. When using a non-standard frequency crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

**TABLE 6: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK**

| OUTPUT Data Rate MCR Bit-7=1 | OUTPUT Data Rate MCR Bit-7=0 (DEFAULT) | DIVISOR FOR 16x Clock (Decimal) | DIVISOR FOR 16x Clock (HEX) | DLM PROGRAM VALUE (HEX) | DLL PROGRAM VALUE (HEX) | DATA RATE ERROR (%) |
|---|---|---|---|---|---|---|
| 100 | 400 | 2304 | 900 | 09 | 00 | 0 |
| 600 | 2400 | 384 | 180 | 01 | 80 | 0 |
| 1200 | 4800 | 192 | C0 | 00 | C0 | 0 |
| 2400 | 9600 | 96 | 60 | 00 | 60 | 0 |
| 4800 | 19.2k | 48 | 30 | 00 | 30 | 0 |
| 9600 | 38.4k | 24 | 18 | 00 | 18 | 0 |
| 19.2k | 76.8k | 12 | 0C | 00 | 0C | 0 |
| 38.4k | 153.6k | 6 | 06 | 00 | 06 | 0 |
| 57.6k | 230.4k | 4 | 04 | 00 | 04 | 0 |
| 115.2k | 460.8k | 2 | 02 | 00 | 02 | 0 |
| 230.4k | 921.6k | 1 | 01 | 00 | 01 | 0 |

## 2.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

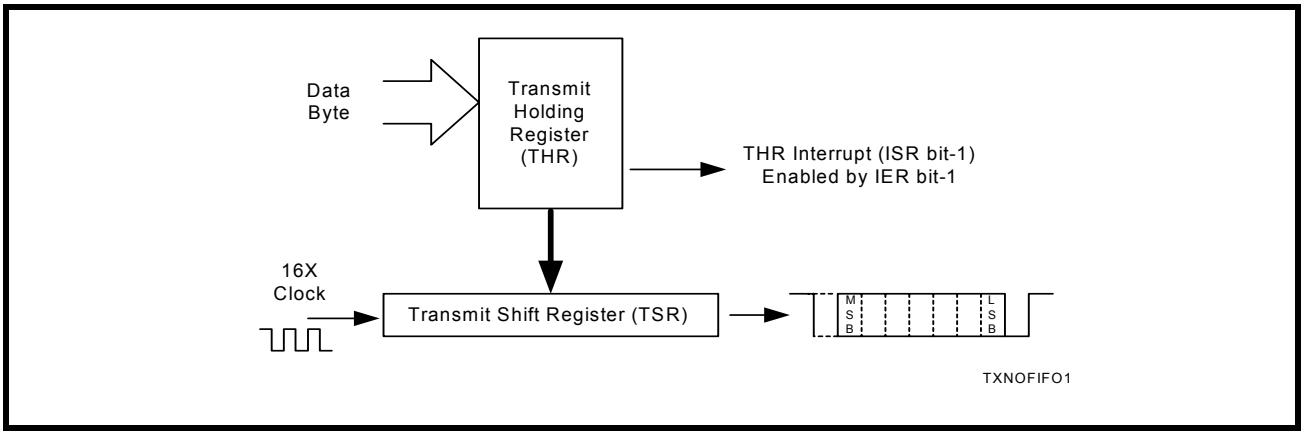
### 2.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

### 2.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

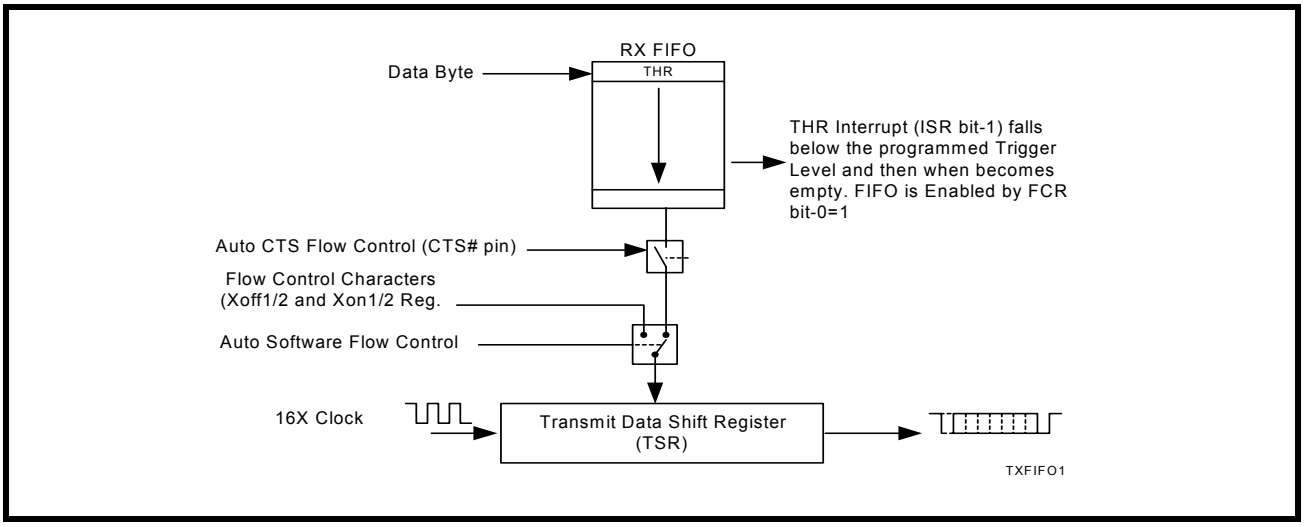
**FIGURE 7. TRANSMITTER OPERATION IN NON-FIFO MODE**




### 2.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the FIFO becomes empty. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

**FIGURE 8. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE**



### 2.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

#### 2.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

**FIGURE 9. RECEIVER OPERATION IN NON-FIFO MODE**

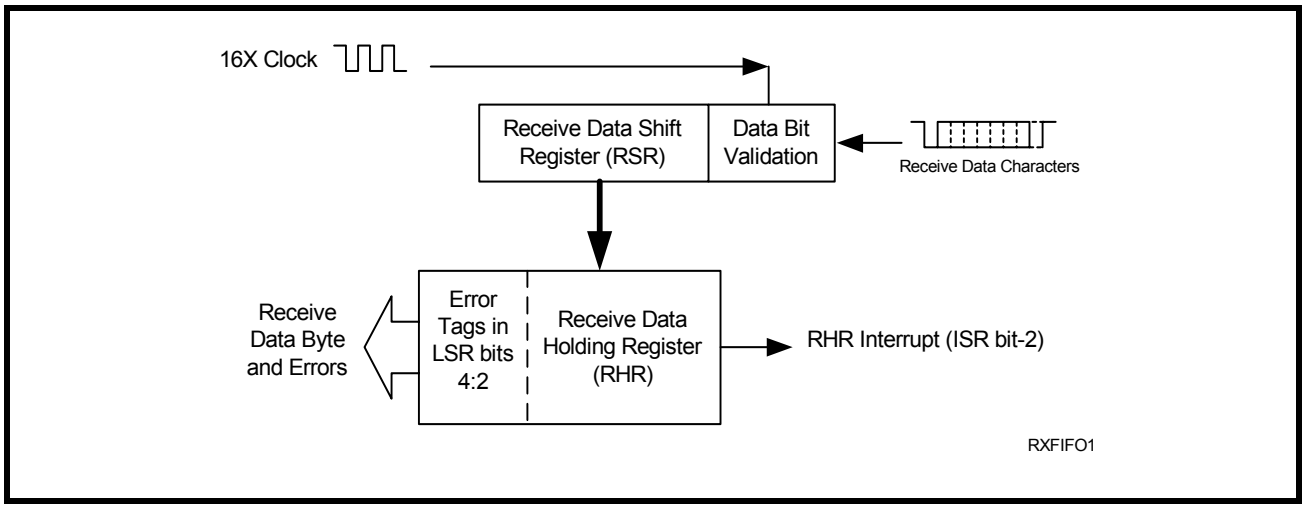
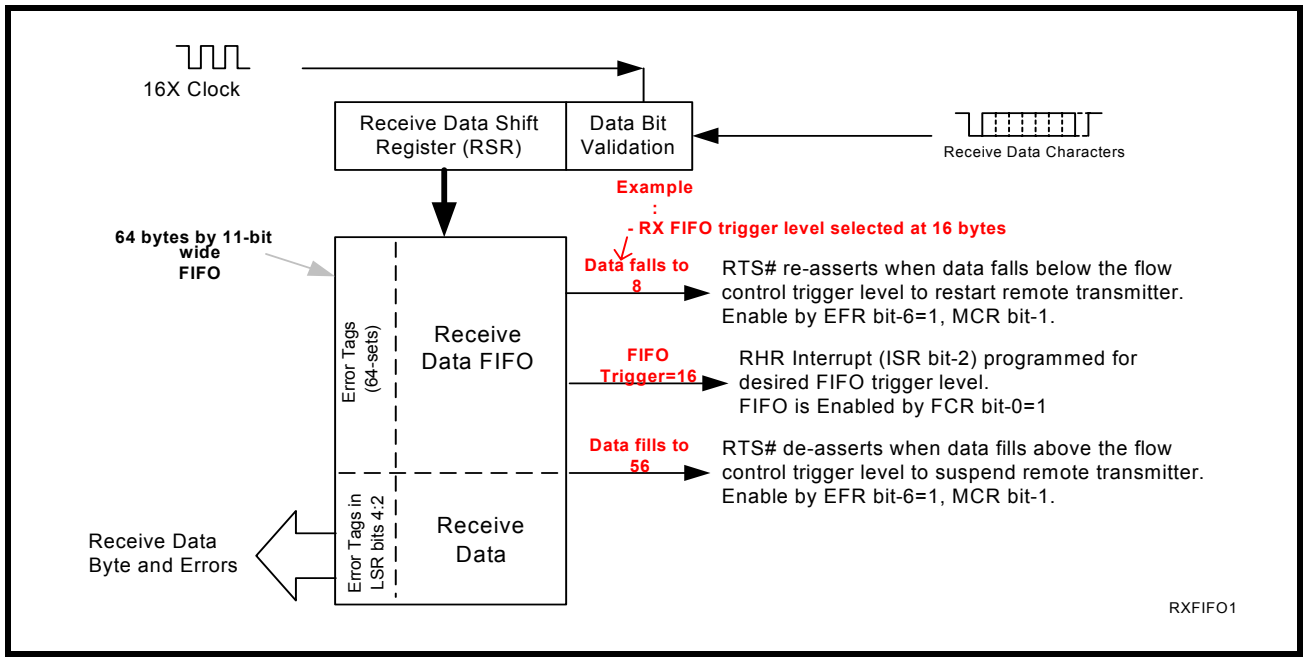


FIGURE 10. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE




## 2.11 Auto RTS Hardware Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 11):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If needed, the RTS interrupt can be enabled through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

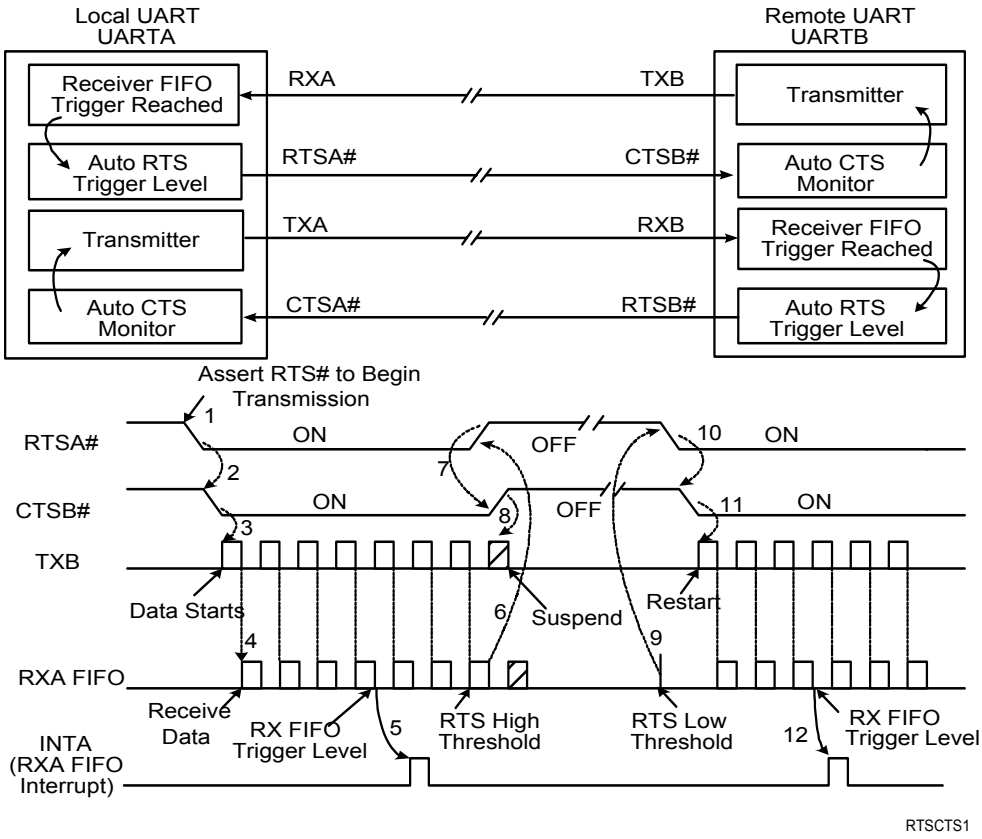
## 2.12 Auto CTS Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see Figure 11):

- Enable auto CTS flow control using EFR bit-7.

If needed, the CTS interrupt can be enabled through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

**FIGURE 11. AUTO RTS AND CTS FLOW CONTROL OPERATION**




*The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.*

**TABLE 7: AUTO RTS/CTS FLOW CONTROL**

| SELECTED TRIGGER LEVEL | INT PIN ACTIVATION | RTS# PIN DE-ASSERTED (LOGIC 1) | RTS# PIN RE-ASSERTED (LOGIC 0) |
|---|---|---|---|
| 8 | 8 | 16 | 0 |
| 16 | 16 | 56 | 8 |
| 56 | 56 | 60 | 16 |
| 60 | 60 | 60 | 56 |

### 2.13 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 15), the 654 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 654 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the 654 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the 654 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 15) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 654 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 654 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 654 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the 654 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level. Table 8 below explains this.

**TABLE 8: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL**

| RX TRIGGER LEVEL | INT PIN ACTIVATION | XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO) | XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO) |
|---|---|---|---|
| 8 | 8 | 8* | 0 |
| 16 | 16 | 16* | 8 |
| 56 | 56 | 56* | 16 |
| 60 | 60 | 60* | 56 |

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2* characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.

### 2.14 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 654 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

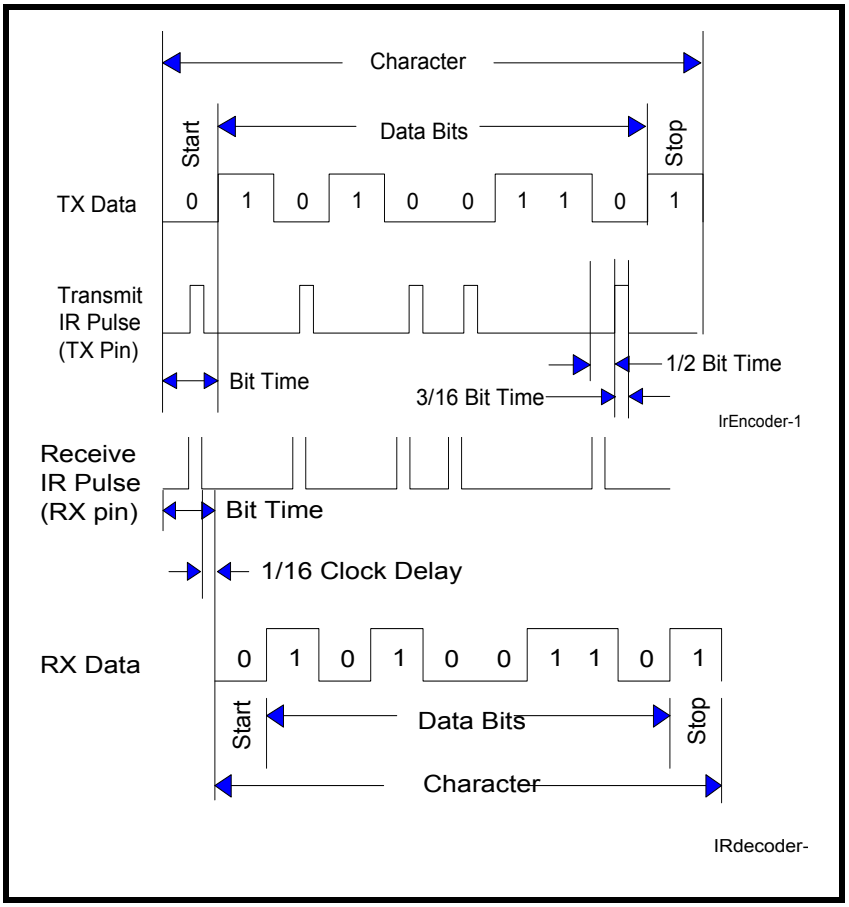
## 2.15 Infrared Mode

The 654 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 12 below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see Figure 12.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream.

**FIGURE 12. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING**



### 2.16 Sleep Mode with Auto Wake-Up

The 654 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the 654 to enter sleep mode:

- no interrupts pending for all four channels of the 654 (ISR bit-0 = 1)
- sleep mode of both channels are enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idling at a logic 1

The 654 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 654 resumes normal operation by any of the following:

- a receive data start bit transition (logic 1 to 0)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the 654 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 2750 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The 654 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

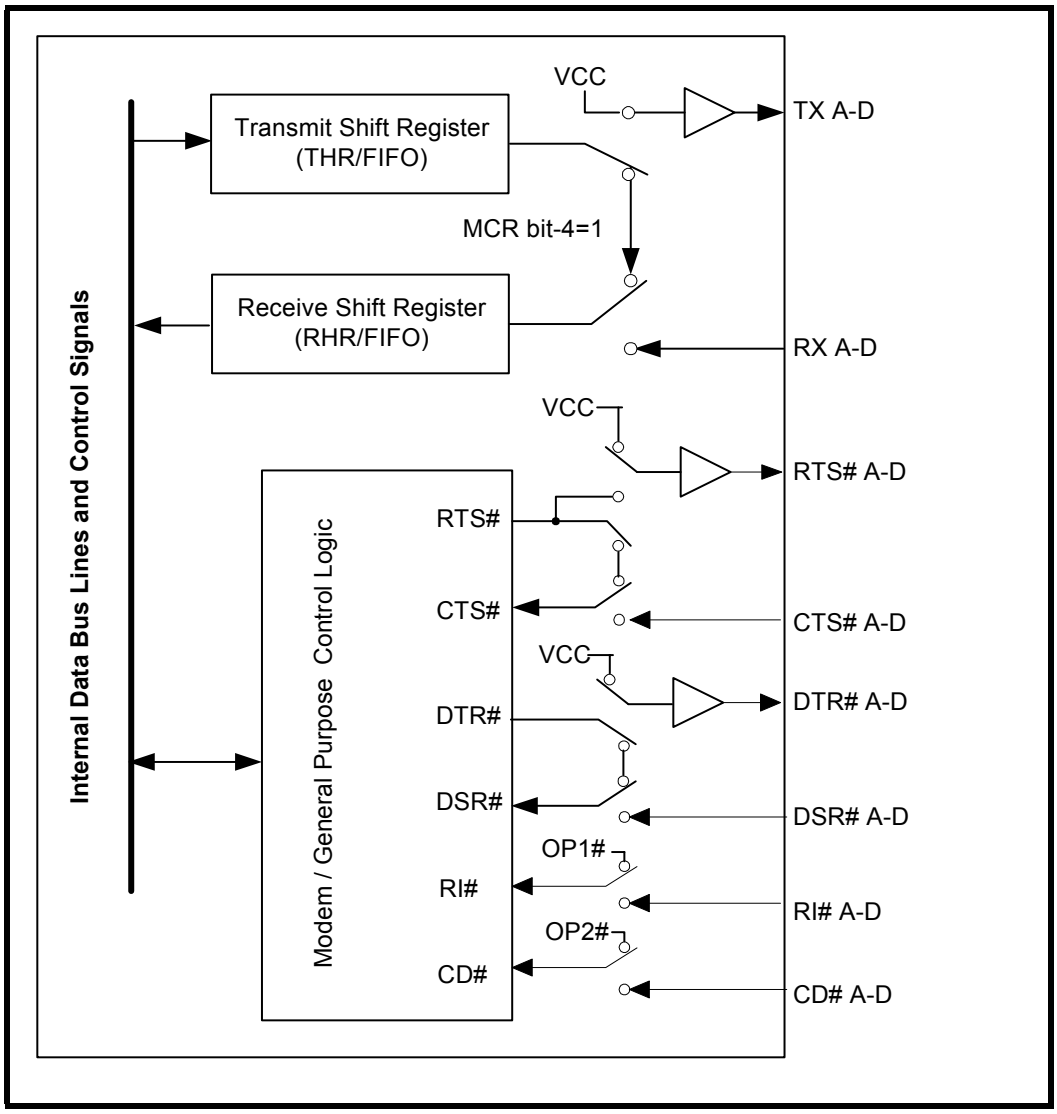
If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, CSC#, CSD# and modem input lines remain steady when the 654 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 37. If the input lines are floating or are toggling while the 654 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX A-D pins are idling at logic 1 or “marking” condition during sleep mode. This may not occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on each of the RX A-D inputs.

### 2.17 Internal Loopback

The 654 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 13 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

**FIGURE 13. INTERNAL LOOP BACK IN CHANNEL A AND B**



## 3.0 UART INTERNAL REGISTERS

Each UART channel in the 654 has its own set of configuration registers selected by address lines A0, A1 and A2 with a specific channel selected (See Table 1 and Table 2). The complete register set is shown on Table 9 and Table 10.

.

**TABLE 9: UART CHANNEL A AND B UART INTERNAL REGISTERS**

| A2,A1,A0 ADDRESSES | REGISTER | READ/WRITE | COMMENTS |
|---|---|---|---|
| **16C550 COMPATIBLE REGISTERS** | | | |
| 0 0 0 | RHR - Receive Holding Register<br>THR - Transmit Holding Register | Read-only<br>Write-only | LCR[7] = 0 |
| 0 0 0 | DLL - Div Latch Low Byte | Read/Write | LCR[7] = 1, LCR ≠ 0xBF |
| 0 0 1 | DLM - Div Latch High Byte | Read/Write | |
| 0 0 1 | IER - Interrupt Enable Register | Read/Write | LCR[7] = 0 |
| 0 1 0 | ISR - Interrupt Status Register<br>FCR - FIFO Control Register | Read-only<br>Write-only | |
| 0 1 1 | LCR - Line Control Register | Read/Write | |
| 1 0 0 | MCR - Modem Control Register | Read/Write | LCR[7] = 0 |
| 1 0 1 | LSR - Line Status Register<br>Reserved | Read-only<br>Write-only | |
| 1 1 0 | MSR - Modem Status Register<br>Reserved | Read-only<br>Write-only | |
| 1 1 1 | SPR - Scratch Pad Register | Read/Write | |
| **ENHANCED REGISTERS** | | | |
| 0 1 0 | EFR - Enhanced Function Reg | Read/Write | LCR = 0xBF |
| 1 0 0 | Xon-1 - Xon Character 1 | Read/Write | |
| 1 0 1 | Xon-2 - Xon Character 2 | Read/Write | |
| 1 1 0 | Xoff-1 - Xoff Character 1 | Read/Write | |
| 1 1 1 | Xoff-2 - Xoff Character 2 | Read/Write | |
| | | | |
| X X X | FSTAT - FIFO Status Register | Read-only | FSRS# pin is logic 0 |

**TABLE 10: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1**

| ADDRESS A2-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **16C550 Compatible Registers** | | | | | | | | | | | |
| 0 0 0 | RHR | RD | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 0 0 0 | THR | WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 0 0 1 | IER | RD/WR | 0/ CTS# Int. Enable | 0/ RTS# Int. Enable | 0/ Xoff Int. Enable | 0/ Sleep Mode Enable | Modem Stat. Int. Enable | RX Line Stat. Int. Enable | TX Empty Int Enable | RX Data Int. Enable | |
| 0 1 0 | ISR | RD | FIFOs Enabled | FIFOs Enabled | 0/ INT Source Bit-5 | 0/ INT Source Bit-4 | INT Source Bit-3 | INT Source Bit-2 | INT Source Bit-1 | INT Source Bit-0 | LCR[7] = 0 |
| 0 1 0 | FCR | WR | RXFIFO Trigger | RXFIFO Trigger | 0/ TXFIFO Trigger | 0/ TXFIFO Trigger | DMA Mode Enable | TX FIFO Reset | RX FIFO Reset | FIFOs Enable | |
| 0 1 1 | LCR | RD/WR | Divisor Enable | Set TX Break | Set Par-ity | Even Parity | Parity Enable | Stop Bits | Word Length Bit-1 | Word Length Bit-0 | |
| 1 0 0 | MCR | RD/WR | 0/ BRG Pres-caler | 0/ IR Mode ENable | 0/ XonAny | Internal Lopback Enable | INT Out-put Enable (OP2#) | Rsvd (OP1#) | RTS# Output Control | DTR# Output Control | |
| 1 0 1 | LSR | RD | RX FIFO Global Error | THR & TSR Empty | THR Empty | RX Break | RX Fram-ing Error | RX Parity Error | RX Over-run Error | RX Data Ready | LCR[7] = 0 |
| 1 1 0 | MSR | RD | CD# Input | RI# Input | DSR# Input | CTS# Input | Delta CD# | Delta RI# | Delta DSR# | Delta CTS# | |
| 1 1 1 | SPR | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7] = 0 |
| **Baud Rate Generator Divisor** | | | | | | | | | | | |
| 0 0 0 | DLL | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7] = 1 LCR ≠ 0xBF |
| 0 0 1 | DLM | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |

**TABLE 10: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1**

| ADDRESS A2-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Enhanced Registers** | | | | | | | | | | | |
| 0 1 0 | EFR | RD/WR | Auto CTS# Enable | Auto RTS# Enable | Special Char Select | Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5] | Soft-ware Flow Cntl Bit-3 | Soft-ware Flow Cntl Bit-2 | Soft-ware Flow Cntl Bit-1 | Soft-ware Flow Cntl Bit-0 | LCR=0xBF |
| 1 0 0 | XON1 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 0 1 | XON2 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 0 | XOFF1 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 1 | XOFF2 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| | | | | | | | | | | | |
| X X X | FSTAT | RD | RX-RDYD# | RX-RDYC# | RX-RDYB# | RX-RDYA# | TX-RDYD# | TX-RDYC# | TX-RDYB# | TX-RDYA# | FSRS# pin is a logic 0. No address lines required. |

## 4.0 INTERNAL REGISTER DESCRIPTIONS

### 4.1 Receive Holding Register (RHR) - Read- Only

See “Receiver” on page 15.

### 4.2 Transmit Holding Register (THR) - Write-Only

See “Transmitter” on page 13.

### 4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

#### 4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

**A.** The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

**B.** FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

**C.** The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

### 4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the ST16C654 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

**A.** LSR BIT-0 indicates there is data in RHR or RX FIFO.

**B.** LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

**C.** LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

**D.** LSR BIT-5 indicates THR is empty.

**E.** LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

**F.** LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

**IER[0]: RHR Interrupt Enable**

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

Logic 0 = Disable the receive data ready interrupt (default).

Logic 1 = Enable the receiver data ready interrupt.

**IER[1]: THR Interrupt Enable**

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

Logic 0 = Disable Transmit Ready interrupt (default).

Logic 1 = Enable Transmit Ready interrupt.

**IER[2]: Receive Line Status Interrupt Enable**

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when an overrun occurs. LSR bits 2-4 generate an interrupt when the character in the RHR has an error.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

**IER[3]: Modem Status Interrupt Enable**

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

**IER[4]: Sleep Mode Enable (requires EFR[4] = 1)**

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

**IER[5]: Xoff Interrupt Enable (requires EFR[4]=1)**

- Logic 0 = Disable the software flow control, receive Xoff interrupt. (default)
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

**IER[6]: RTS# Output Interrupt Enable (requires EFR[4]=1)**

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from low to high (if enabled by EFR bit-6).