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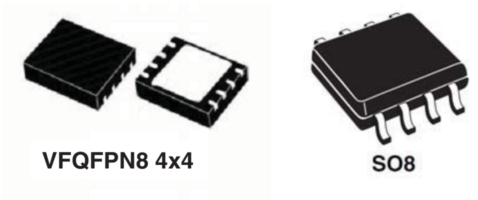
ST1CC40

3 A monolithic step-down current source with synchronous rectification

Datasheet - production data



Features

- 3.0 V to 18 V operating input voltage range
- 850 kHz fixed switching frequency
- 100 mV typ. current sense voltage drop
- 6 µA standby current in inhibit mode
- ± 7% output current accuracy
- Synchronous rectification
- 95 mΩ HS / 69 mΩ LS typical $R_{DS(on)}$
- Peak current mode architecture
- Embedded compensation network
- Internal current limiting
- Ceramic output capacitor compliant
- Thermal shutdown

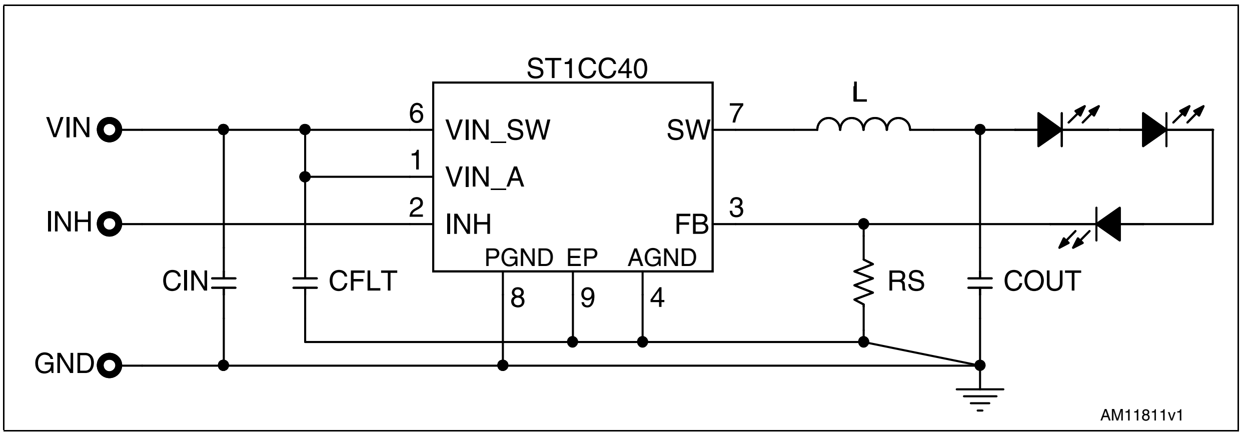
Applications

- Battery charger
- Signage
- Emergency lighting
- High brightness LED driving
- General lighting

Description

The ST1CC40 device is an 850 kHz fixed switching frequency monolithic step-down DC-DC converter designed to operate as precise constant current source with an adjustable current capability up to 3 A DC. The regulated output current is set connecting a sensing resistor to the feedback pin. The embedded synchronous rectification and the 100 mV typical R_{SENSE} voltage drop enhance the efficiency performance. The size of the overall application is minimized thanks to the high switching frequency and ceramic output capacitor compatibility. The device is fully protected against thermal overheating, overcurrent and output short-circuit. Inhibit mode minimizes the current consumption in standby. The ST1CC40 is available in VFQFPN8 4 mm x 4 mm 8-lead, and standard SO8 package.

Figure 1. Typical application circuit



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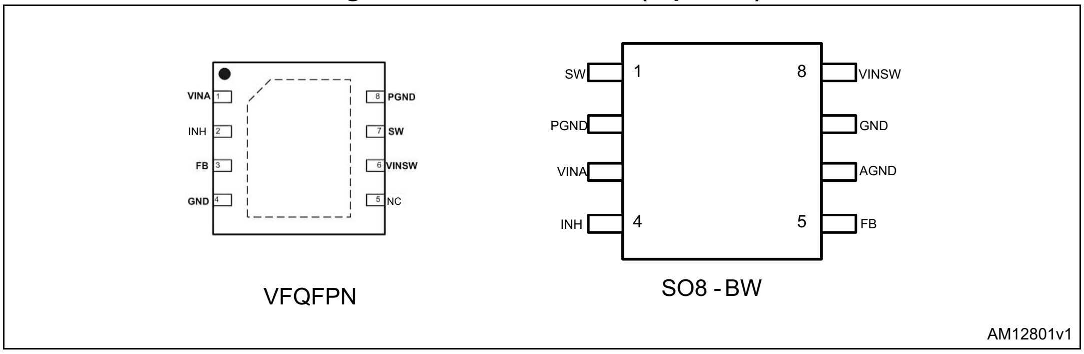
1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.		Type	Description
VFQFPN8	S08-BW		
1	3	VIN_A	Analog circuitry power supply connection
2	4	INH	Inhibit input pin. Low signal level disables the device. Leave this pin floating if not used
3	5	FB	Feedback input. Connect a proper sensing resistor to set the LED current
4	6	AGND	Analog circuitry ground connection
5	-	NC	Not connected
6	8	V_{INSW}	Power input voltage
7	1	SW	Regulator switching pin
8	2	PGND	Power ground
-	7	GND	Connect to AGND

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{INSW}	Power input voltage	-0.3 to 20	V
V_{INA}	Input voltage	-0.3 to 20	
V_{INH}	Inhibit voltage	-0.3 to V_{INA}	
V_{SW}	Output switching voltage	-1 to V_{IN}	
V_{PG}	Power Good	-0.3 to V_{IN}	
V_{FB}	Feedback voltage	-0.3 to 2.5	
I_{FB}	FB current	-1 to +1	mA
P_{TOT}	Power dissipation at T_A < 60 °C	2	W
T_{OP}	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient(1)	VFQFPN8	40	°C/W
		SO8-BW	65	

1. Package mounted on demonstration board.

4 Electrical characteristics

T_J= 25 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IN}	Operating input voltage range	See(1)	3		18	V
	Device ON level		2.6	2.75	2.9	
	Device OFF level		2.4	2.55	2.7	
V_{FB}	Feedback voltage	T_J = 25 °C	90	97	104	mV
		T_J = 125 °C	90	100	110	
I_{FB}	V_{FB} pin bias current				600	nA
R_{DSON}-P	High-side switch on-resistance	I_{SW} = 750 mA		95		mΩ
R_{DSON}-N	Low-side switch on-resistance	I_{SW} = 750 mA		69		mΩ
I_{LIM}	Maximum limiting current	See(2)		5		A
Oscillator						
F_{SW}	Switching frequency		0.7	0.85	1	MHz
D	Duty cycle	See(2)	0		100	%
DC characteristics						
I_q	Quiescent current	Duty cycle = 0 V_{fb} > 100 mV		1.5	2.5	mA
I_{QST-BY}	Total standby quiescent current	OFF		2.4	4.5	µA
		See(1)			6	
Inhibit						
V_{INH}	INH threshold voltage	Device ON level	1.2			V
		Device OFF level			0.4	
I_{INH}	INH current			2		µA
Soft-start						
T_{SS}	Soft-start duration			1		ms
Protection						
T_{SHDN}	Thermal shutdown			150		°C
	Hystereris			15		

1. Specifications referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.

2. Guaranteed by design.

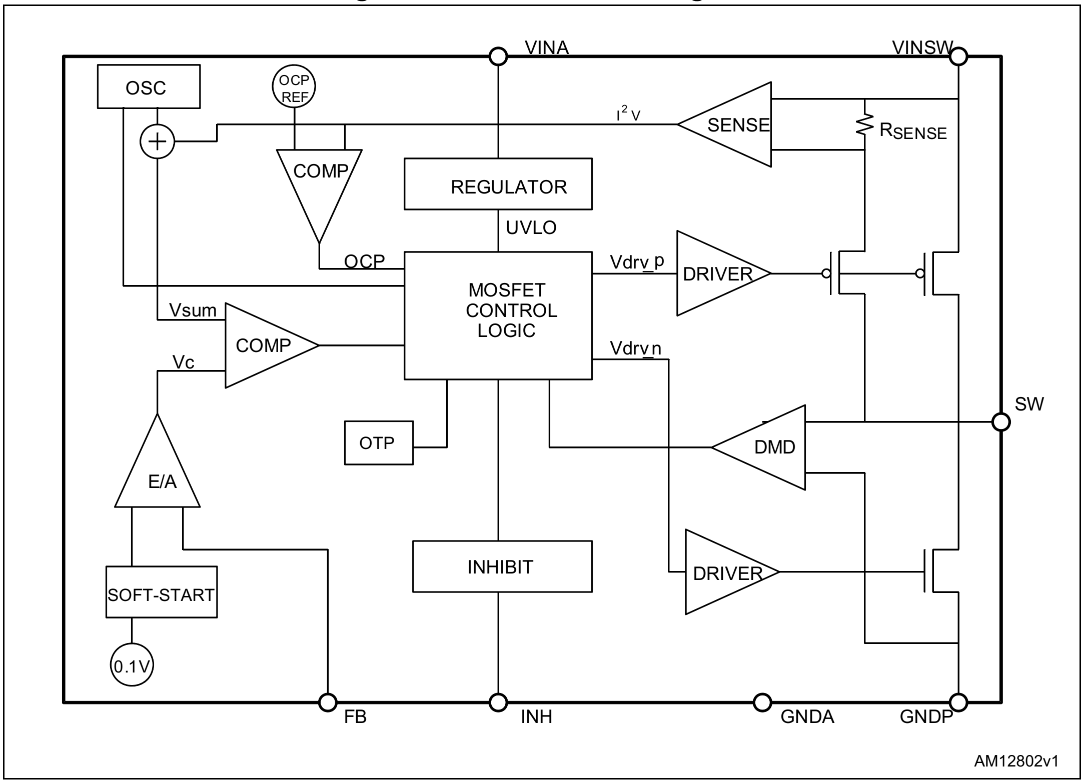
5 Functional description

The ST1CC40 device is based on a “peak current mode” architecture with fixed frequency control. As a consequence, the intersection between the error amplifier output and the sensed inductor current generates the control signal to drive the power switch.

The main internal blocks shown in the block diagram in *Figure 3* are:

- High-side and low-side embedded power element for synchronous rectification
- A fully integrated sawtooth oscillator with a typical frequency of 850 kHz
- A transconductance error amplifier
- A high-side current sense amplifier to track the inductor current
- A pulse width modulator (PWM) comparator and the circuitry necessary to drive the internal power element
- The soft-start circuitry to decrease the inrush current at power-up
- The current limitation circuit based on the pulse-by-pulse current protection with frequency divider
- The inhibit circuitry
- The thermal protection function circuitry

Figure 3. ST1CC40 block diagram



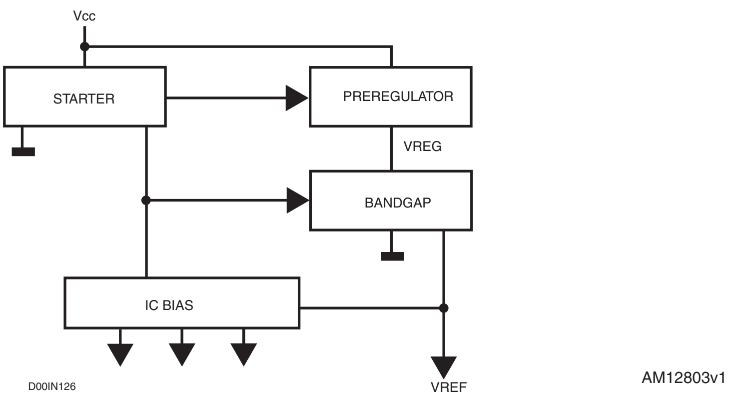
5.1 Power supply and voltage reference

The internal regulator circuit consists of a startup circuit, an internal voltage pre-regulator, the BandGap voltage reference and the bias block that provides current to all the blocks. The starter supplies the startup current to the entire device when the input voltage goes high and the device is enabled (INHIBIT pin connected to ground). The pre-regulator block supplies the bandgap cell with a pre-regulated voltage that has a very low supply voltage noise sensitivity.

5.2 Voltage monitor

An internal block continuously senses the V_{cc}, V_{ref} and V_{bg}. If the monitored voltages are good, the regulator begins operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



5.3 Soft-start

The startup phase is implemented ramping the reference of the embedded error amplifier in 1 msec typ. time. It minimizes the inrush current and decreases the stress of the power components at power-up.

During normal operation a new soft-start cycle takes place in case of:

- Thermal shutdown event
- UVLO event.

5.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non-inverting input is connected to the internal voltage reference (100 mV), while the inverting input (FB) is connected to the output current sensing resistor.

The error amplifier is internally compensated to minimize the size of the final application.

Table 5. Uncompensated error amplifier characteristics

Description	Value
Transconductance	250 μS
Low frequency gain	96 dB
C_C	195 pF
R_C	70 KΩ

The error amplifier output is compared with the inductor current sense information to perform PWM control.

5.5 Inhibit

The inhibit block disables most of the circuitry when the INH input signal is low. The current drawn from the input voltage is 6 μA typical in inhibit mode.

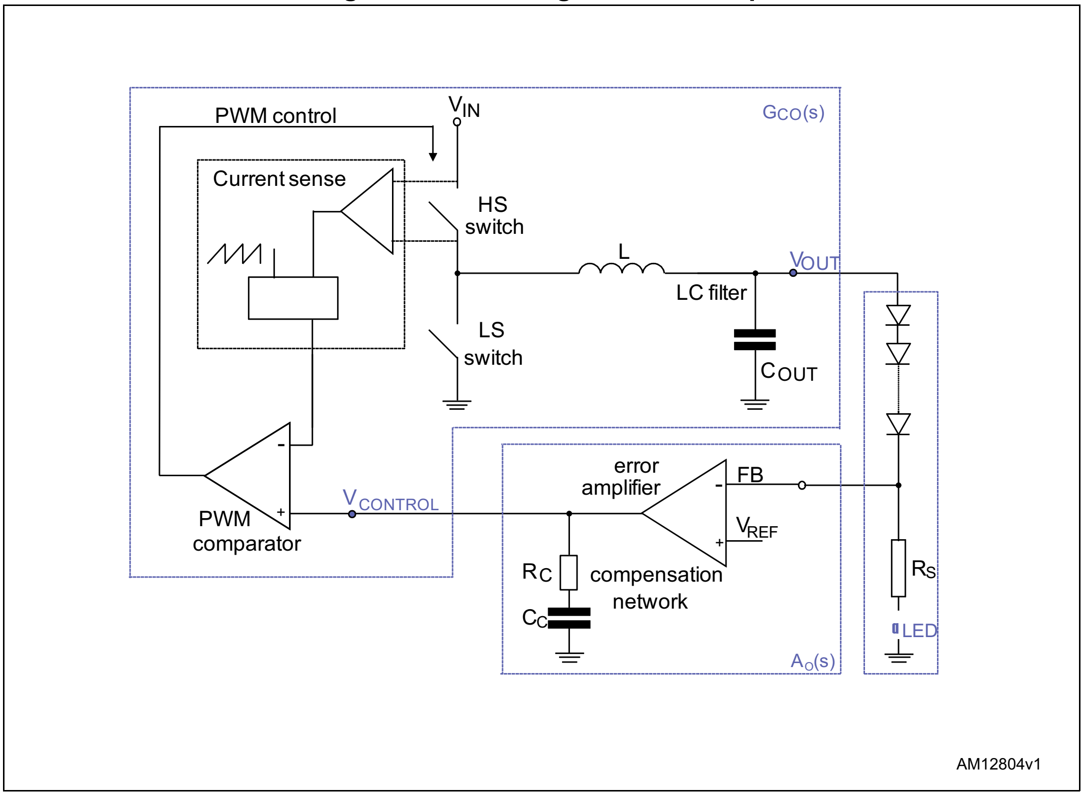
5.6 Thermal shutdown

The shutdown block generates a signal that disables the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 ± 10 °C typical). The sensing element of the chip is close to the PDMOS area, ensuring fast and accurate temperature detection. A 15 °C typical hysteresis prevents the device from turning ON and OFF continuously during the protection operation.

6 Application notes

6.1 Closing the loop

Figure 5. Block diagram of the loop



6.2 $G_{CO}(s)$ control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

Equation 1

$$G_{CO}(s) = \frac{R_0}{R_i} \cdot \frac{1}{1 + \frac{R_0 \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0{,}5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_0 represents the load resistance, R_i the equivalent sensing resistor of the current sense circuitry, ω_p the single pole introduced by the LC filter and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts for the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 2

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

Equation 3

$$\omega_P = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1-D) - 0{,}5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 4

$$\begin{cases} m_C = 1 + \dfrac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \dfrac{V_{IN} - V_{OUT}}{L} \cdot R_i \end{cases}$$

S_n represents the slope of the sensed inductor current, S_e the slope of the external ramp (V_{PP} peak-to-peak amplitude) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

Equation 5

$$F_H(s) = \frac{1}{1 + \dfrac{s}{\omega_n \cdot Q_P} + \dfrac{s^2}{\omega_n^2}}$$

where:

Equation 6

$$\omega_n = \pi \cdot f_{SW}$$

and

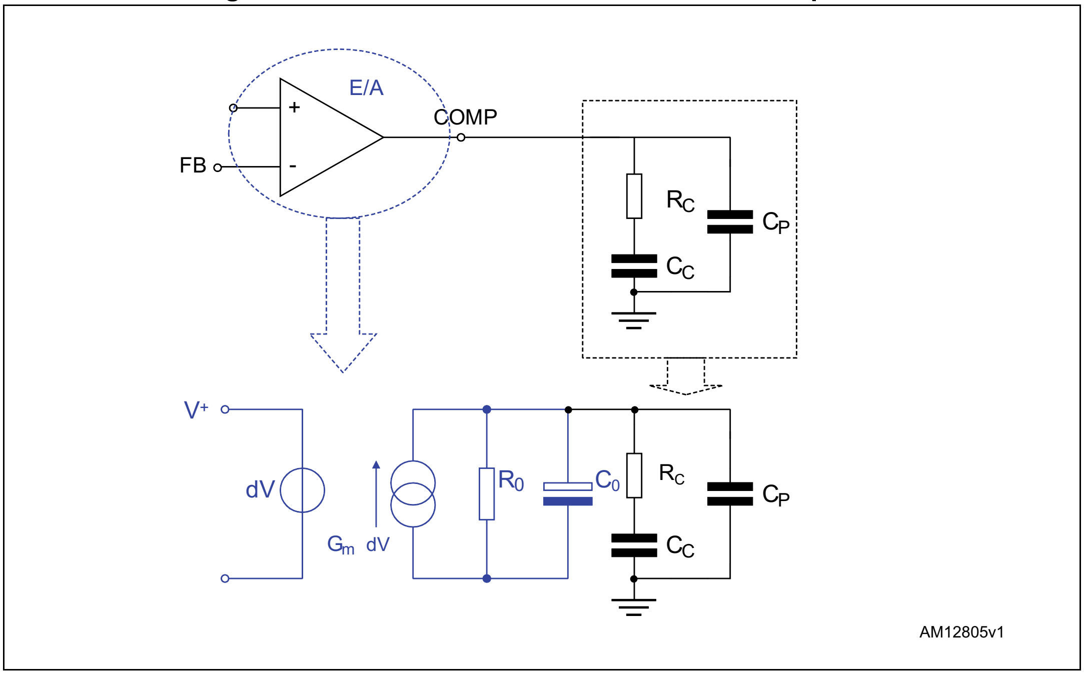
Equation 7

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1-D) - 0{,}5]}$$

6.3 Error amplifier compensation network

The ST1CC40 device embeds the error amplifier (see *Figure 6*) and a pre-defined compensation network which is effective in stabilizing the system in most of the application conditions.

Figure 6. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

Equation 8

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

where $A_{vo} = G_m \cdot R_o$.

The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 9

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 10

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 11

$$F_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

The embedded compensation network is R_C = 70 K, C_C = 195 pF while C_P and C_O can be considered as negligible. The error amplifier output resistance is 240 MΩ so the relevant singularities are:

Equation 12

$$f_Z = 11,6\ \text{kHz} \qquad f_{P\ LF} = 3,4\ \text{Hz}$$

6.4 LED small signal model

Once the system reaches the working condition the LEDs composing the row are biased and their equivalent circuit can be considered as a resistor for frequencies << 1 MHz.

The LED manufacturer typically provides the equivalent dynamic resistance of the LED biased at different DC current. This parameter is required to study the behavior of the system in the small signal analysis.

For instance, the equivalent dynamic resistance of Luxeon III Star from Lumiled measured with a different biasing current level is reported below:

$$r_{LED} \quad \begin{cases} 1{,}3\Omega & I_{LED} = 350\text{mA} \\ 0{,}9\Omega & I_{LED} = 700\text{mA} \end{cases}$$

In case the LED datasheet doesn't report the equivalent resistor value, it can be simply derived as the tangent to the diode I-V characteristic in the present working point (see *Figure 7*).

Figure 7. Equivalent series resistor

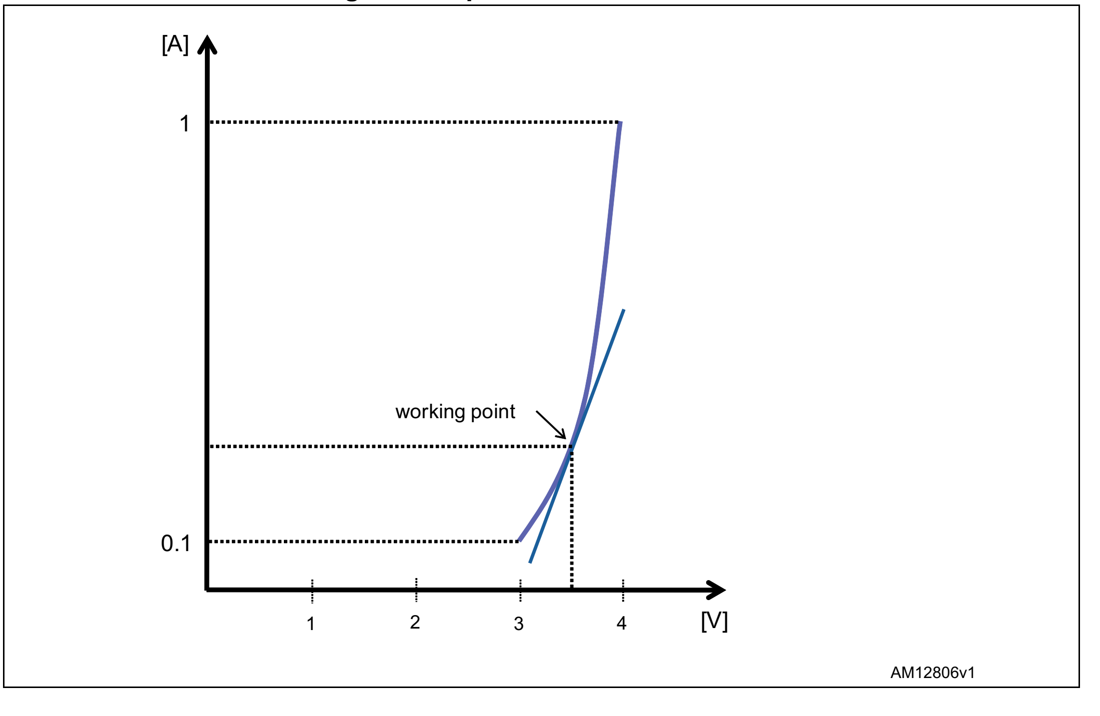
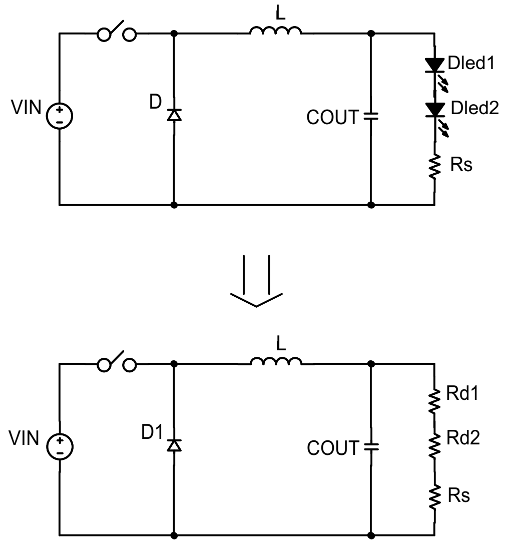


Figure 8 shows the equivalent circuit of the LED constant current generator.

Figure 8. Load equivalent circuit



As a consequence, the LED equivalent circuit gives the α_{LED}(s) term correlating the output voltage with the high impedance FB input:

Equation 13

$$\alpha_{LED}(n_{LED}) = \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE}}$$

6.5 Total loop gain

In summary, the open loop gain can be expressed as:

Equation 14

$$G(s) = G_{CO}(s) \cdot A_0(s) \cdot \alpha_{LED}(n_{LED})$$

Example

Design specifications:

V_{IN} = 12 V, V_{FW_LED} = 3.5 V, n_{LED} = 2, r_{LED} = 1.1 Ω, I_{LED} = 700 mA, $I_{LED\ RIPPLE}$ = 2%

The inductor and capacitor value are dimensioned in order to meet the $I_{LED\ RIPPLE}$ specifications (see *Section 7.1.2* for output capacitor and inductor selection guidelines)*:*

L = 10 µH, C_{OUT} = 2.2 µF MLCC (negligible ESR)

Accordingly, with *Section 7.1.1* the sensing resistor value is:

Equation 15

$$R_S = \frac{100\ \text{mV}}{700\ \text{mA}} \cong 140\ \text{m}\Omega$$

Equation 16

$$\alpha_{LED}(n_{LED}) = \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE}} = \frac{140\ \text{m}\Omega}{2 \cdot 1{,}1\Omega + 140\ \text{m}\Omega} = 0{,}06$$

The gain and phase margin Bode diagrams are plotted respectively in *Figure 9* and *Figure 10*.

Figure 9. Module plot

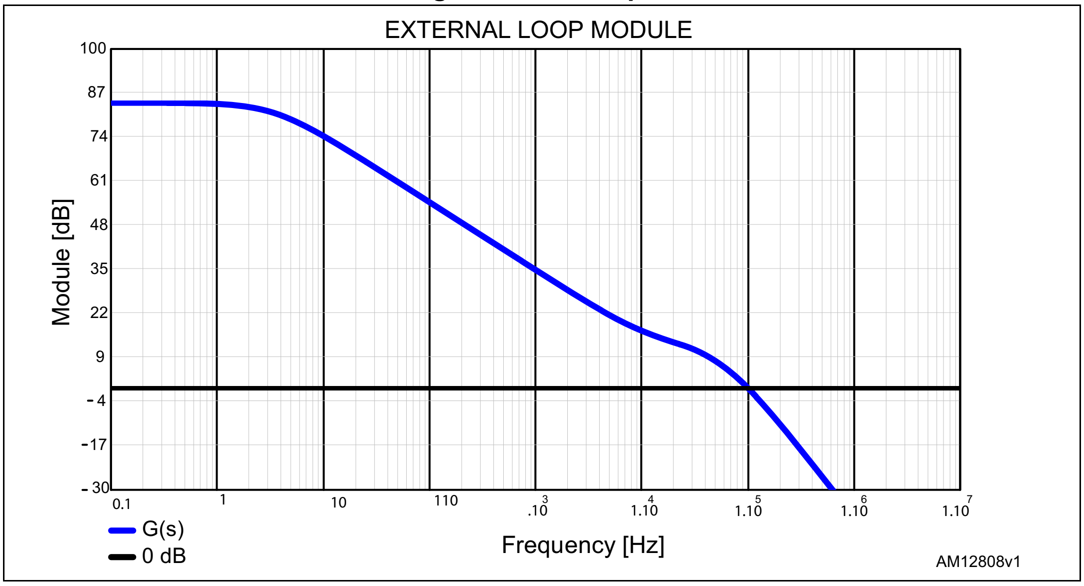
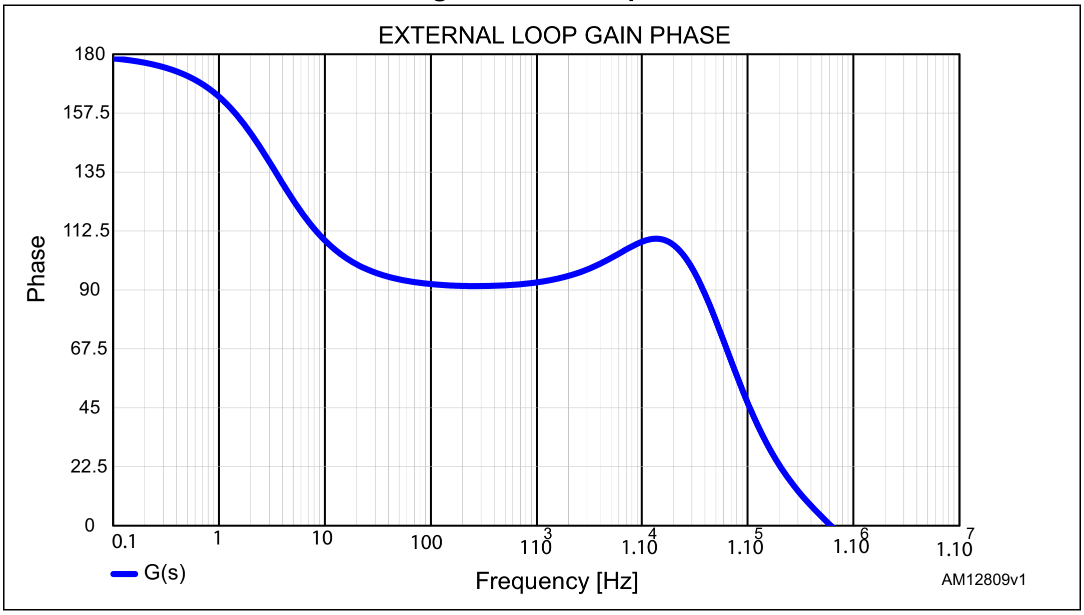


Figure 10. Phase plot



The cutoff frequency and the phase margin are:

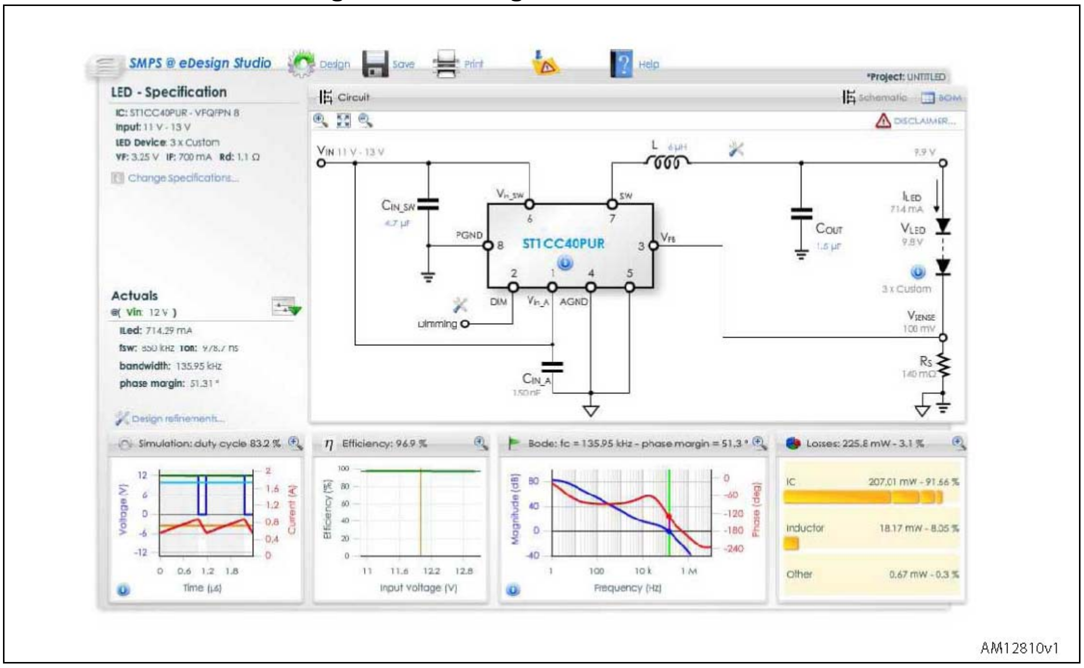
Equation 17

$$f_C = 100\ \text{kHz} \qquad pm = 47°$$

6.6 eDesign studio software

The ST1CC40 device is supported by the eDesign software which can be seen online on the STMicroelectronics® home page (www.st.com).

Figure 11. eDesign studio screenshot



The software easily supports the component sizing according to the technical information given in this datasheet (see *Section 6*).

The final user is requested to fill in the requested information such as the input voltage range, the selected LED parameters and the number of LEDs composing the row.

The software calculates external components according to the internal database. It is also possible to define new components and ask the software to have them used.

Bode plots, estimated efficiency and thermal performance are provided.

Finally, the user can save the design and print all the information including the bill of material of the board.

7 Application information

7.1 Component selection

7.1.1 Sensing resistor

In closed loop operation the ST1CC40 feedback pin voltage is 100 mV so the sensing resistor calculation is expressed as:

Equation 18

$$R_S = \frac{100\ mV}{I_{LED}}$$

Since the main loop (see *Section 6.1*) regulates the sensing resistor voltage drop, the average current is regulated into the LEDs. The integration period is at minimum 5 * T_{SW} since the system bandwidth can be dimensioned up to $F_{SW}/5$ at maximum.

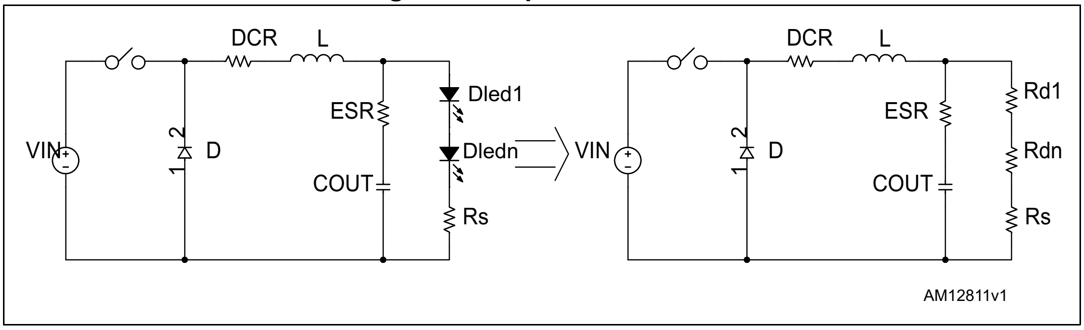
The system performs the output current regulation over a period which is at least five times longer than the switching frequency. The output current regulation neglects the ripple current contribution and its reliance on external parameters like input voltage and output voltage variations (line transient and LED forward voltage spread). This performance can not be achieved with simpler regulation loops like a hysteretic control.

For the same reason the switching frequency is constant over the application conditions, that helps to tune the EMI filtering and to guarantee the maximum LED current ripple specifications in the application range. This performance cannot be achieved using constant on/off-time architecture.

7.1.2 Inductor and output capacitor selection

The output capacitor filters the inductor current ripple that, given the application conditions, depends on the inductor value. As a consequence, the LED current ripple, that is the main specification for a switching current source, depends on the inductor and output capacitor selection.

Figure 12. Equivalent circuit



The LED ripple current can be calculated as the inductor ripple current ratio flowing into the output impedance using the Laplace transform (see *Figure 11*):

Equation 19

$$\Delta I_{RIPPLE}(s) = \frac{\frac{8}{\pi^2} \cdot \Delta I_L \cdot (1 + s \cdot ESR \cdot C_{OUT})}{1 + s \cdot (R_S + ESR + n_{LED} \cdot R_{LED}) \cdot C_{OUT}}$$

where the term $8/\pi^2$ represents the main harmonic of the inductor current ripple (which has a triangular shape) and ΔI_L is the inductor current ripple.

Equation 20

$$\Delta I_L = \frac{V_{OUT}}{L} \cdot T_{OFF} = \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{L} \cdot T_{OFF}$$

so L value can be calculated as:

Equation 21

$$L = \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{\Delta I_L} \cdot T_{OFF} = \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{\Delta I_L} \cdot \left(1 - \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{V_{IN}}\right)$$

where T_{OFF} is the off-time of the embedded high switch, given by 1-D.

As a consequence, the lower the inductor value (so the higher the current ripple), the higher the C_{OUT} value would be to meet the specifications.

A general rule to dimension L value is:

Equation 22

$$\frac{\Delta I_L}{I_{LED}} \leq 0,5$$

Finally the required output capacitor value can be calculated equalizing the LED current ripple specification with the module of the Fourier transformer (see *Equation 19*) calculated at F_{SW} frequency.

Equation 23

$$|\Delta I_{RIPPLE}(s=j \cdot \omega)| = \Delta I_{RIPPLE\_SPEC}$$

Example (see *Section : Example*):

V_{IN} = 12 V, I_{LED} = 700 mA, Δ_{ILED}/I_{LED} = 2%, V_{FW_LED} = 3.5 V, n_{LED} = 2

The output capacitor value must be dimensioned according to Equation 23.

Finally, given the selected inductor value, a 2.2 µF ceramic capacitor value keeps the LED current ripple ratio lower than 2% of the nominal current. An output ceramic capacitor type (negligible ESR) is suggested to minimize the ripple contribution given a fixed capacitor value.

Table 6. Inductor selection

Manufacturer	Series	Inductor value (μH)	Saturation current (A)
Würth Elektronik	WE-HCI 7040	1 to 4.7	20 to 7
	WE-HCI 7050	4.9 to 10	20 to 4.0
Coilcraft	XPL 7030	2.2 to 10	29 to 7.2

7.1.3 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor must absorb all this switching current, whose RMS value can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS current flowing through the capacitor. The maximum RMS input current (flowing through the input capacitor) is:

Equation 24

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle and I_O is the output DC current. Considering η = 1, this function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2. The maximum and minimum duty cycles are:

Equation 25

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 26

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the max. I_{RMS} going through the input capacitor. Capacitors that can be considered are:

Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

Tantalum capacitors:

Small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is recommended to avoid this type of capacitor for the input filter of the device as they may be stressed by a high surge current when connected to the power supply.

Table 7. List of ceramic capacitors for the ST1CC40

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)
TAIYO YUDEN	UMK325BJ106MM-T	10	50
MURATA	GRM42-2 X7R 475K 50	4.7	50

In case the selected capacitor is ceramic (so neglecting the ESR contribution), the input voltage ripple can be calculated as:

Equation 27

$$V_{IN\,PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

7.2 Layout considerations

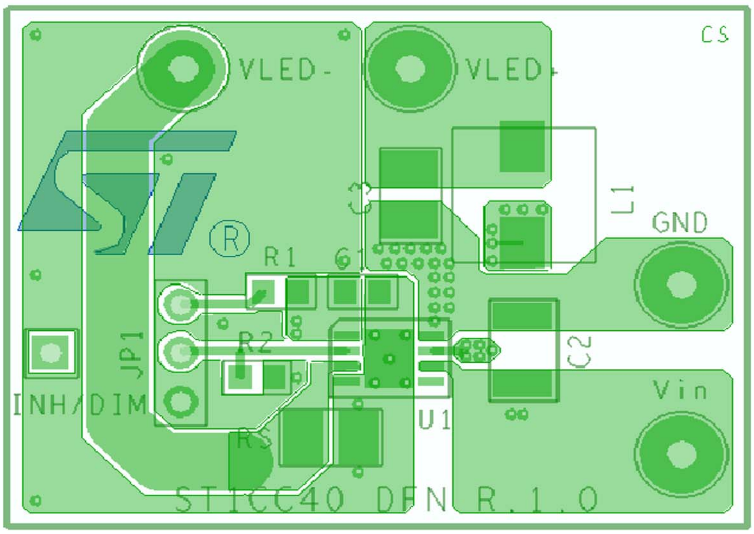
The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in *Figure 13*.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin to the sensing resistor path must be designed as short as possible to avoid pick-up noise. Another important issue is the ground plane of the board. Since the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction-to-ambient.

To increase the design noise immunity, different signal and power ground should be implemented in the layout (see *Section 7.5: Application circuit*). The signal ground serves the small signal components, the device analog ground pin, the exposed pad and a small filtering capacitor connected to the V_{INA} pin. The power ground serves the device ground pin and the input filter. The different grounds are connected underneath the output capacitor. Neglecting the current ripple contribution, the current flowing through this component is constant during the switching activity and so this is the cleanest ground point of the buck application circuit.

Figure 13. Layout example



7.3 Thermal considerations

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the $R_{DS(on)}$, which are equal to:

Equation 28

$$P_{ON} = R_{RDSON\_HS} \cdot (I_{OUT})^2 \cdot D$$

$$P_{OFF} = R_{RDSON\_LS} \cdot (I_{OUT})^2 \cdot (1 - D)$$

where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} ($n_{LED} * V_{LED}$ + 100 mV) and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the conduction losses related to the $R_{DS(on)}$ increase compared to an ideal case.

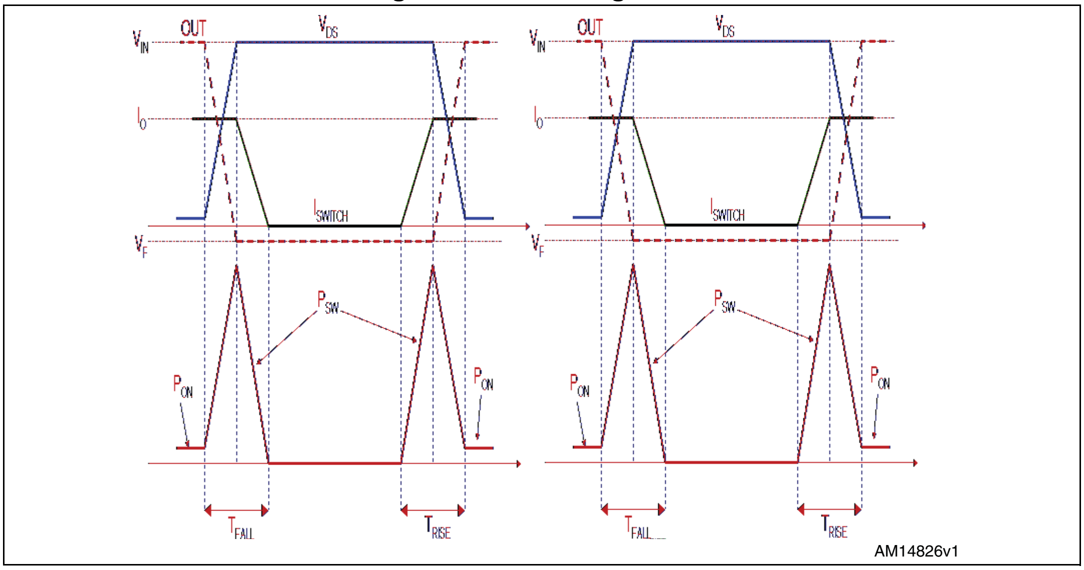
- Switching losses due to turning ON and OFF. These are derived using *Equation 29*:

Equation 29

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW\_EQ} \cdot F_{SW}$$

where T_{RISE} and T_{FALL} represent the switching times of the power element that causes the switching losses when driving an inductive load (see *Figure 14*). T_{SW} is the equivalent switching time.

Figure 14. Switching losses



Quiescent current losses.

Equation 30

$$P_Q = V_{IN} \cdot I_Q$$

Example (see *Section : Example*):

$V_{IN} = 12\ V,\ V_{FW\_LED} = 3.5\ V,\ n_{LED} = 2,\ I_{LED} = 700\ mA$

The typical output voltage is:

Equation 31

$$V_{OUT} = n_{LED} \cdot V_{FW\_LED} + V_{FB} = 7{,}1V$$

R_{DSON_HS} has a typical value of 95 mΩ and $R_{DS(on)\_LS}$ is 69 mΩ at 25 °C.

For the calculation we can estimate $R_{DS(on)\_HS}$ = 140 mΩ and $R_{DS(on)\_LS}$ = 100 mΩ as a consequence of T_J increase during the operation.

T_{SW_EQ} is approximately 12 ns.

I_Q has a typical value of 1.5 mA at V_{IN} = 12 V.