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ST1S14

Up to 3 A step-down switching regulator

HSOP8 - exposed pad
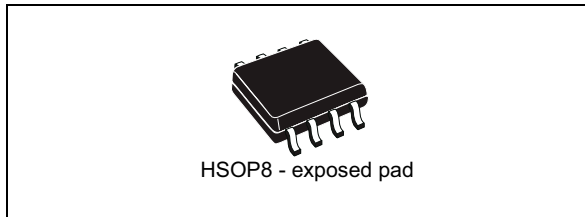
Applications

- Factory automation
- Printers
- DC-DC modules
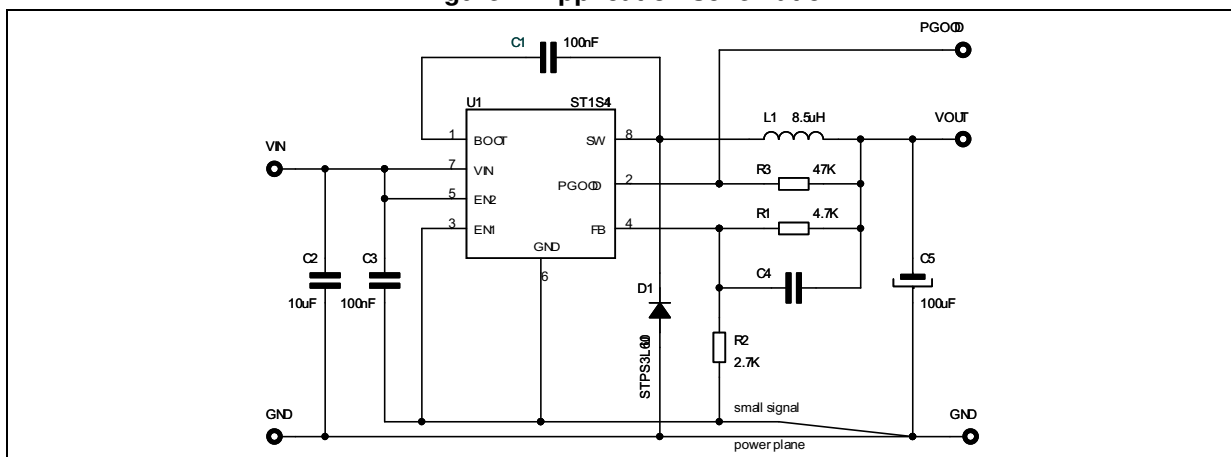- High current LED drivers

Features

- 3 A DC output current
- Operating input voltage from 5.5 V to 48 V
- 850 kHz internally fixed switching frequency
- Internal soft-start
- Power good open collector output
- Current mode architecture
- Embedded compensation network
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- 2 mA maximum quiescent current over temperature range
- 250 mΩ typ. $R_{DS(on)}$
- Thermal shutdown

Description

The ST1S14 is a step-down monolithic power switching regulator able to deliver up to 3 A DC current to the load depending on the application conditions. The high current level is also achieved thanks to a HSOP8 package with exposed frame, that allows to reduce the $R_{th(JA)}$ down to approximately 40 °C/W. The output voltage can be set from 1.22 V. The device uses an internal N-channel DMOS transistor (with a typical $R_{DS(on)}$ of 200 mΩ) as the switching element to minimize the size of the external components. The internal oscillator fixes the switching frequency at 850 kHz. Power good open collector output validates the regulated output voltage as soon as it reaches the regulation. Pulse-by-pulse current limit offers an effective constant current short-circuit protection. Current foldback decreases overstress in a persistent short-circuit condition.

Figure 1. Application schematic

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Contents

List of figure

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)
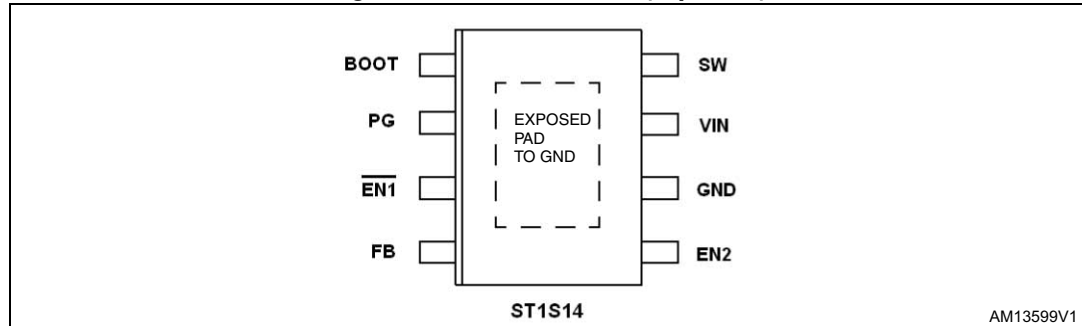
1.2 Pin description

Table 1. Pin description

N	Pin	Description
1	BOOT	Bootstrap capacitor for N-channel gate driver. Connects 100 nF low ESR capacitor from BOOT pin to SW
2	PG	Power good
3	$\overline{EN1}$	Enable pin active low
4	FB	Feedback voltage
5	EN2	Enable pin active high
6	GND	Ground pin
7	V_{IN}	Input supply pin
8	SW	Switching node
	E.p.	Exposed pad must be connected to GND

1.3 Enable inputs

Table 2. Truth table

$\overline{EN1}$	EN2	Device status
H	L	INH
H	H	INH
L	L	INH
L	H	ON

2 Electrical data

2.1 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Power supply input voltage	-0.3 to 52	V
$V_{\overline{EN1}}$	Enable 1 voltage	-0.3 to 7	V
V_{EN2}	Enable 2 voltage	-0.3 to (V_{IN}+0.3)	V
PG	Power good	-0.3 to (V_{IN}+0.3)	V
BOOT	Bootstrap pin	-0.3 to 55	V
SW	Switching node	-1 to (V_{IN}+0.3)	V
V_{FB}	Feedback voltage	-0.3 to 3	V
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)	260	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction-ambient	40	°C/W

2.3 ESD protection

Table 5. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	4	kV
	MM	500	V

3 Electrical characteristics

All the population tested at T_J = 25 °C, V_{CC} =12 V, V_{EN1} = 0 V, V_{EN2} = V_{CC} unless otherwise specified.

The specification is guaranteed from (-40 to +125 °C) T_J temperature range by design, characterization, and statistical correlation.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
V_{IN}	Operating input voltage range			5.5		48	V
$R_{DS(on)}$	MOSFET on resistance	I_{SW}=1 A			0.2	0.4	Ω
I_{SW}	Maximum limiting current			3.7	4.5	5.2	A
t_{HICCUP}	Hiccup time				16		ms
f_{SW}	Switching frequency			600	850	1000	kHz
	Duty cycle		(1)		90		%
$T_{ON\ MIN}$	Minimum conduction time of the power element		(1)		90		ns
$T_{OFF\ MIN}$	Minimum conduction time of the external diode		(1)	75	90	120	ns
DC characteristics							
V_{FB}	Voltage feedback	I_{LOAD}=0 A		1.202	1.22	1.239	V
		I_{LOAD}=10 mA to 3 A		1.196	1.22	1.245	V
I_{FB}	FB biasing current				50		nA
I_q	Quiescent current	V_{FB}=2 V			1.3	2	mA
		V_{FB}=2 V, V_{IN}=48 V			1.7	2.4	mA
I_{qst-by}	Standby quiescent current	Device OFF (see *Table 2*)			16	34	µA
PG	Power good threshold	V_{FB} rising edge			0.92* V_{OUT}		V
		V_{FB} falling edge			0.8* V_{OUT}		V
	PG output voltage (open collector active)	I_{SINK}=6 mA				0.4	V
Inhibit							

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
V$_{\overline{EN1}}$	Enable 1 levels	Device ON V$_{IN}$=5.5 V to 48 V				0.5	V
		Device OFF V$_{IN}$=5.5 V to 48 V		1.5			V
I$_{\overline{EN1}}$	Enable 1 biasing current	V$_{\overline{EN1}}$=5 V		0.7	1.6	3.5	µA
V$_{EN2}$	Enable 2 levels	Device ON V$_{IN}$=5.5 V to 48 V		1.5			V
		Device OFF V$_{IN}$=5.5 V to 48 V				0.5	V
I$_{EN2}$	Enable 2 biasing current	V$_{EN1}$=0 V; V$_{EN2}$=0 V		-1	-2.4	-4.5	µA
		V$_{EN1}$=0 V; V$_{EN2}$=12 V		2.7	5.8	10	µA
		V$_{EN1}$=0 V; V$_{CC}$=V$_{EN2}$=48 V		3.0	6.0	10	µA
Thermal shutdown							
T$_{SHDWN}$	Thermal shutdown temperature		(1)	140	150	160	°C
T$_{HYS}$	Thermal shutdown hysteresis		(1)		15		°C

1. Parameter guaranteed by design

4 Function description

The ST1S14 is based on a "peak current mode", constant frequency control. As a consequence the intersection between the error amplifier output and the sensed inductor current generates the control signal to drive the power switch.

The main internal blocks shown in the block diagram in *Figure 3* are:

- A fully integrated sawtooth oscillator with a typical frequency of 850 kHz
- A transconductance error amplifier
- A high side current sense amplifier to track the inductor current
- A pulse width modulator (PWM) comparator and the circuitry necessary to drive the internal power element
- Soft-start circuitry to decrease the inrush current at power-up
- Current limitation circuit based on the pulse-by-pulse current protection with frequency divider based on FB voltage and the hiccup protection
- Bootstrap circuitry to drive the embedded N-MOS switch
- A multi input inhibit block for standby operation
- A circuit to implement the thermal protection function

Figure 3. Device block diagram
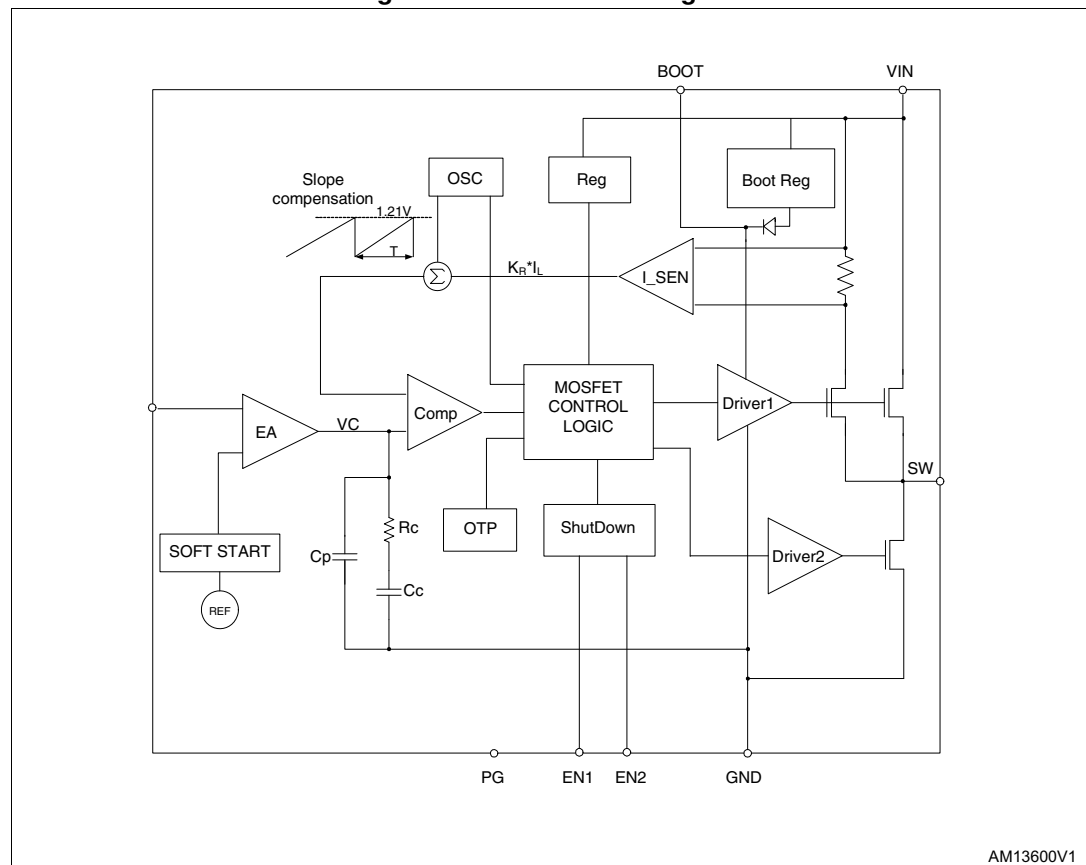
4.1 Power supply and voltage reference

The internal regulator circuit consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference, and the bias block that provides current to all the blocks. The starter supplies the start-up current to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the bandgap cell with a pre-regulated voltage that has a very low supply voltage noise sensitivity.

4.2 Voltage monitor

An internal block continuously senses the V_{cc}, V_{ref}, and V_{bg}. If the monitored voltages are good, the regulator begins operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit
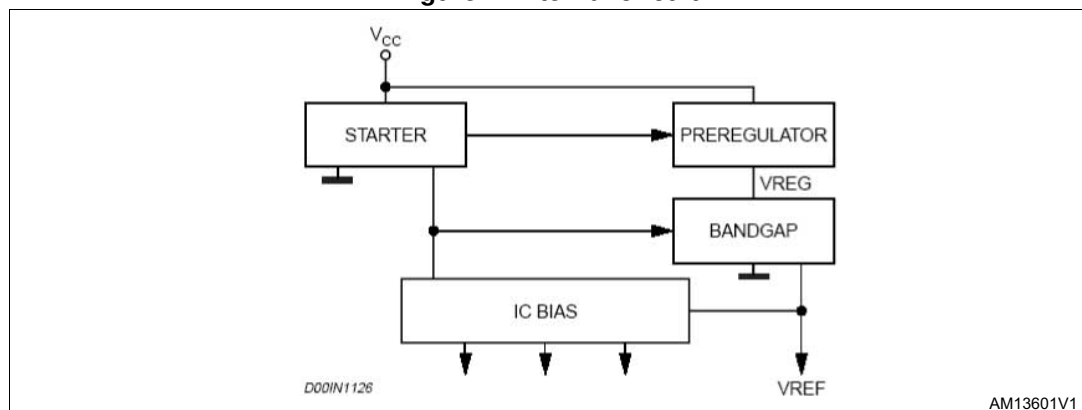
4.3 Soft-start

The startup phase minimizes the inrush current and decreases the stress of the power components at the power up. The startup takes place when VIN crosses the selected UVLO threshold. A internal counter (2816 clks) sets the soft start time (see Figure 5).

The reference of the error amplifier is ramped smootly in 704 steps (one step every 4 clks).

A low pass filter smooths each step to minimize output discontinuity. Considering the typical 850 kHz switching frequency, the phase two duration is 3.3 msec

The device has full load current capability during the soft start time in order to charge the output capacitor (see Figure 5).

Figure 5. Soft-start phases
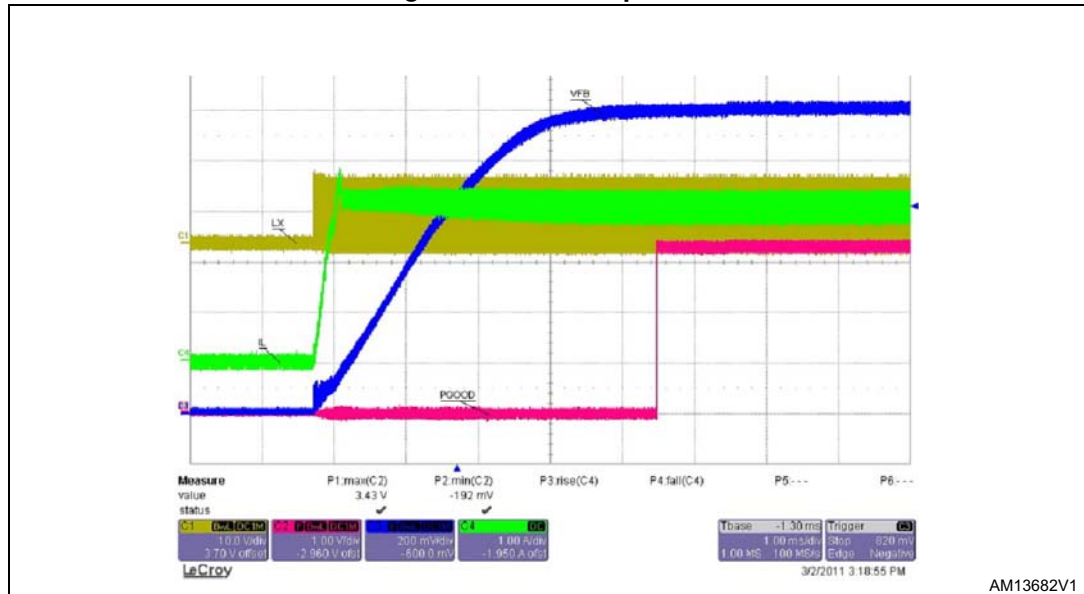
During normal operation a new soft start cycle takes place in case of:

- HICCUP mode current protection
- thermal shutdown event
- UVLO event
- the device is driven in INH mode

Figure 6. Soft-start block diagram
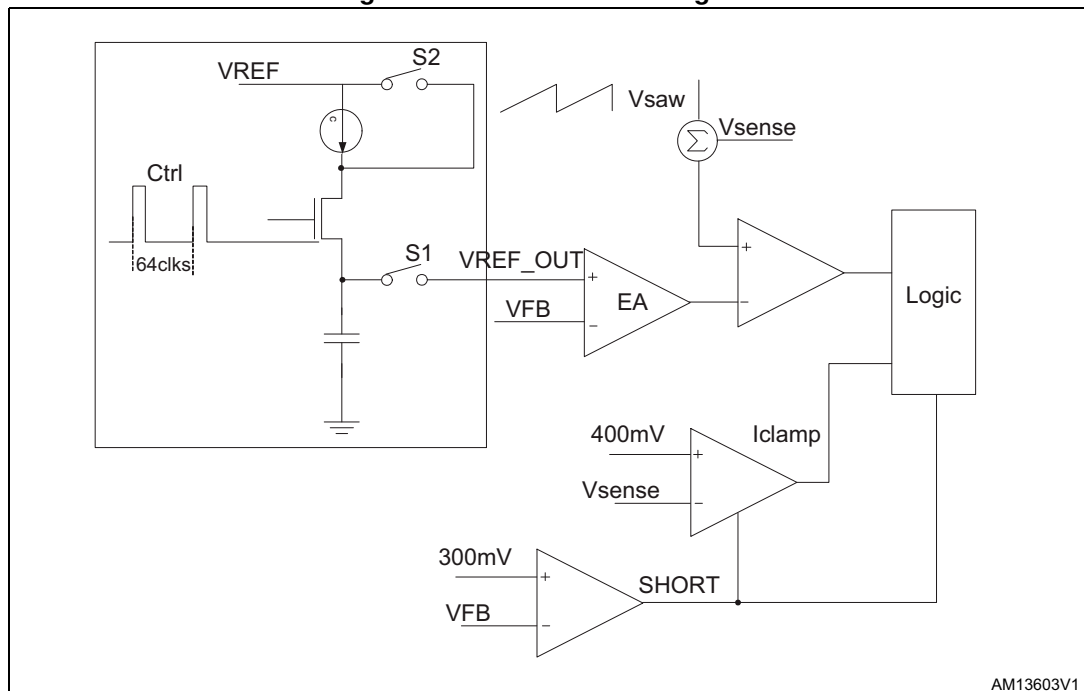
4.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.222 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage.

The error amplifier is internally compensated to minimize the size of the final application.

Table 7. Uncompensated error amplifier characteristics

Description	Values
Transconductance	218 µS
Low frequency gain	93 dB
C_P	24 pF
C_C	211 pF
R_C	200 kΩ

The error amplifier output is compared with the inductor current sense information to perform PWM control.

4.5 Inhibit function

The inhibit feature is used to set the device in standby mode according to *Table 2*. When the device is disabled, the power consumption is reduced to less than 40 µA. The EN2 pin is also V_{IN} compatible.

4.6 Thermal shutdown

The shutdown block generates a signal that turns off the power stage if the temperature of the chip goes higher than a fixed internal threshold (150±10 °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 15 °C keeps the device from turning on and off continuously.

5 Additional features and limitations

5.1 Maximum duty cycle

The bootstrap circuitry charges, cycle-by-cycle, the external bootstrap capacitor to generate a voltage higher than V_{IN} necessary to drive the internal N-channel power element.

An internal linear regulator charges the C_{BOOT} during the conduction time of the external freewheeling diode during the switching activity. The internal logic implements a minimum OFF time of the high side switch (90 nsec typ.) to prevent the bootstrap discharge at high duty cycle. As a consequence, the ST1S14 can operate at a maximum duty cycle of around 90 % typ.

The ST1S14 embeds the diode V_{D1} required for the bootstrap operation.

Figure 7. Bootstrap operation
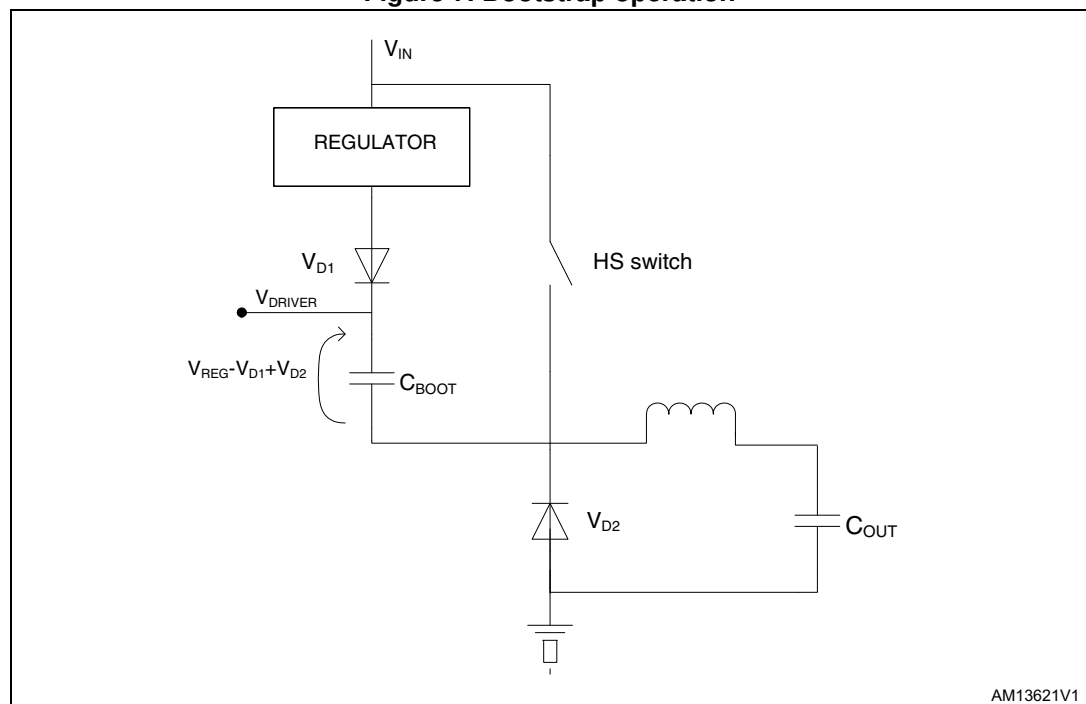
5.2   Minimum output voltage over V$_{IN}$ range

The minimum regulated output voltage at a given input voltage is limited by the minimum conduction time of the power element, that is 90 nsec typ. for the ST1S14:

Equation 1

$$V_{O\_MIN}(V_{IN}) = V_{IN} \cdot D_{MIN} = V_{IN} \cdot \frac{T_{ON\_MIN}}{T_{SW}} = V_{IN} \cdot \frac{90ns}{1.18\mu s}$$

which is plotted in *Figure 14*. The reference of the embedded error amplifier (1.22 V) sets the minimum V$_{O\_SET}$ at low V$_{IN}$.

Figure 8. V$_{O\ MIN}$ over input voltage range
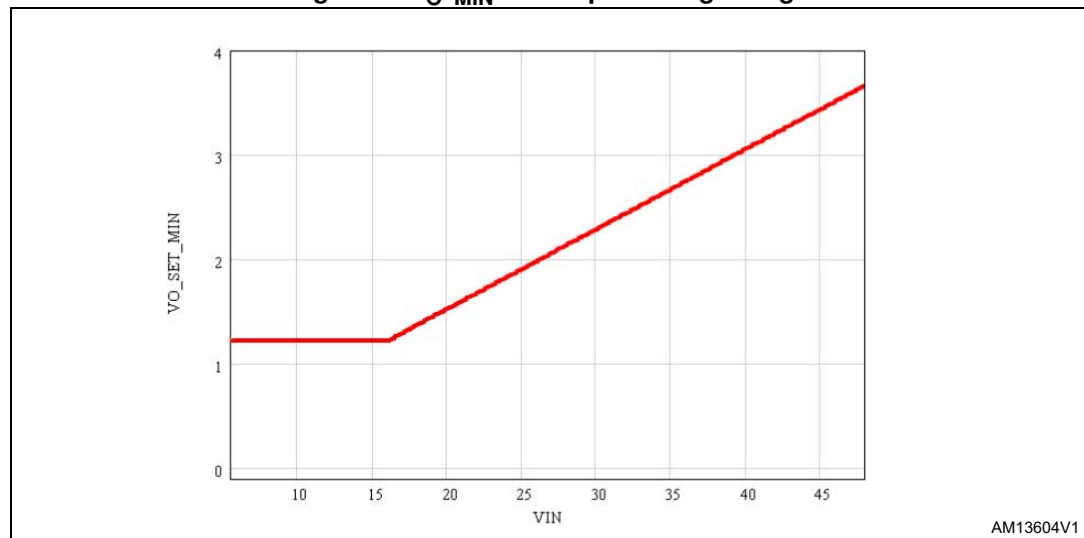
Figure 8 shows the minimum output voltage over input voltage range to have constant switching activity and a predictable output voltage ripple.

The regulator can, however, regulate the minimum input voltage over the entire input voltage range but, given the 90 ns minimum conduction time of the power element, it skips some pulses to keep the output voltage in regulation when *Equation 1* is not satisfied.

This operation is not recommended at the nominal input voltage of the application mainly because it affects the output voltage ripple, but it is generally accepted during a line transient event.

6   Closing the loop

Figure 9. Block diagram of the loop
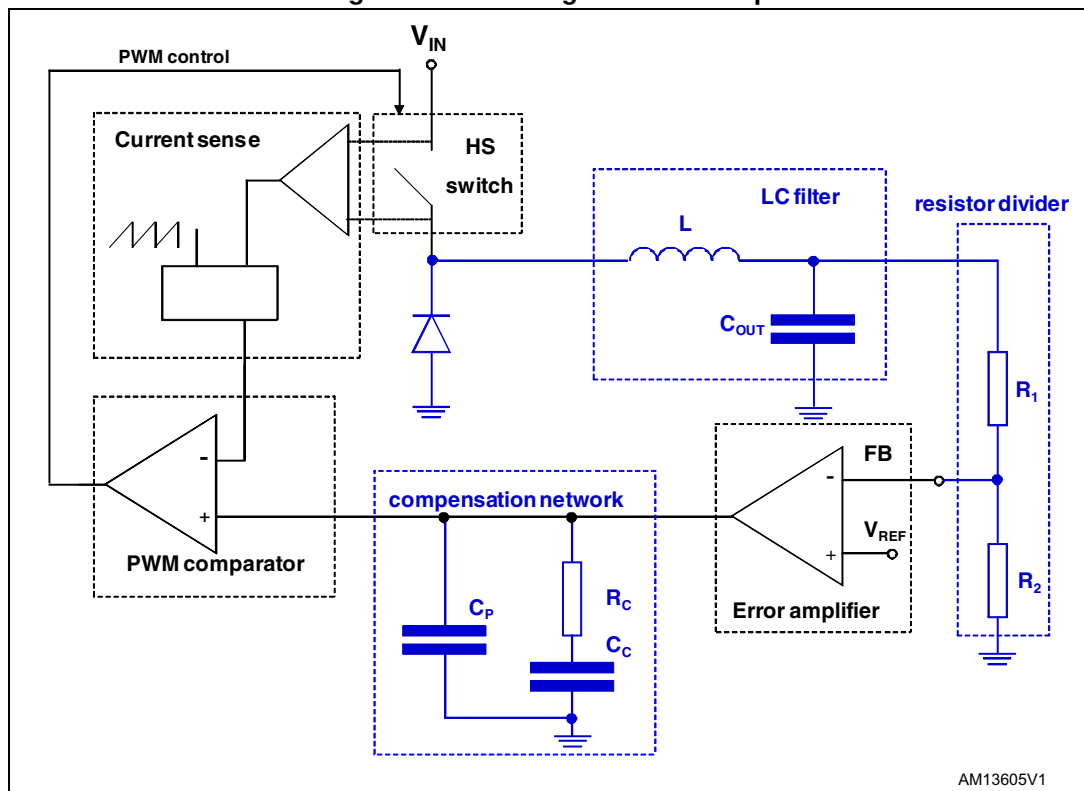
6.1 $G_{CO}(s)$ control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

Equation 2

$$G_{CO}(s) = \frac{R_0}{R_i} \cdot \frac{1}{1 + \frac{R_0 \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_0 represents the load resistance, R_i the equivalent sensing resistor of the current sense circuitry, ω_p the single pole introduced by the LC filter, and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts for the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 3

$$\omega_z = \frac{1}{ESR \cdot C_{OUT}}$$

Equation 4

$$\omega_p = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 5

$$\begin{cases} m_C = 1 + \dfrac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \dfrac{V_{IN} - V_{OUT}}{L} \cdot R_i \end{cases}$$

S_n represents the ON time slope of the sensed inductor current, and S_e the ON time slope of the external ramp (V_{PP} peak to peak amplitude) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50 %.

The sampling effect contribution $F_H(s)$ is:

Equation 6

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

where:

Equation 7

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

6.2 Error amplifier compensation network

The ST1S14 embeds the error amplifier (see *Figure 10*) and a pre-defined compensation network which is effective in stabilizing the system in most of the application conditions.

Figure 10. Transconductance embedded error amplifier
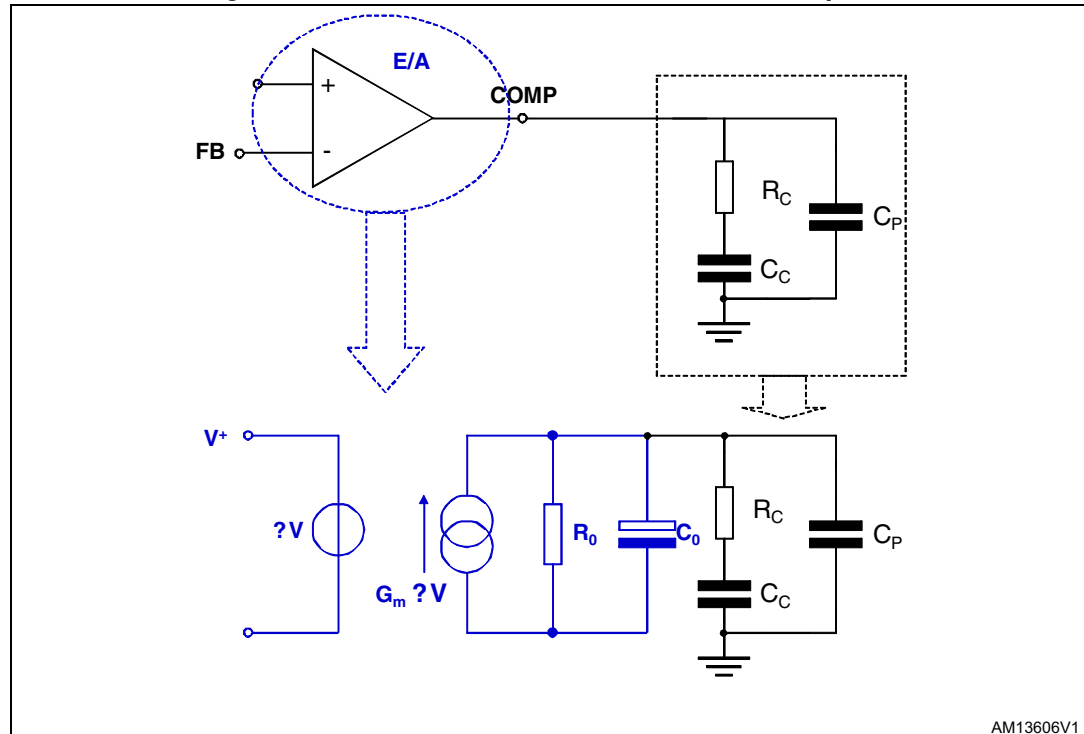
R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

Equation 8

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

where $A_{v0} = G_m \cdot R_0$.

The poles of this transfer function are (if $C_c \gg C_0 + C_P$):

Equation 9

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 10

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 11

$$F_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

The embedded compensation network is R_C=200 K, C_P=24 pF, C_C=211 pF and C_O can be considered negligible, so the singularities are:

Equation 12

$$f_Z = 3,\ 77 \text{ kHz} \qquad f_{P\,LF} = 3,\ 01 \text{ Hz} \qquad f_{P\,HF} = 33,\ 16 \text{ kHz}$$

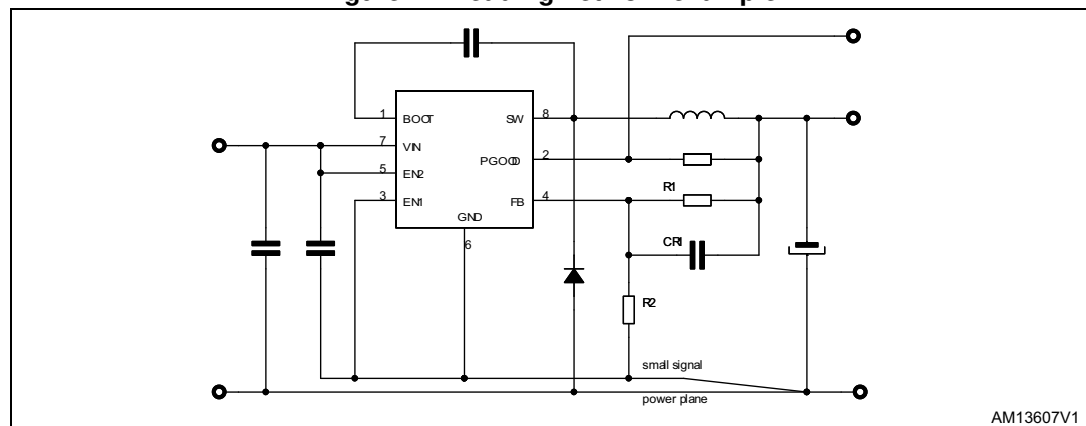## 6.3 Voltage divider

The contribution of a simple voltage divider is:

Equation 13

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

Figure 11. Leading network example

A small signal capacitor in parallel to the upper resistor (see *Figure 11.*) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$), sometimes necessary to improve the system phase margin:

Equation 14

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + s \cdot R_1 \cdot C_{R1})}{\left(1 + s \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}\right)}$$

where:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{R1}}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}}$$

$$f_Z < f_P$$

6.4 Total loop gain

In summary, the open loop gain can be expressed as:

Equation 15

$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_0(s)$$

Example: V_{IN} = 12 V, V_{OUT} = 3.3 V, R_{OUT} = 2 Ω

The resistor divider is R_1=5.6 K, R_2=3.3 K.

C_{R1}=150 nF implements a leading network (f_Z=190 kHz, f_P=510 kHz).

Selecting L = 8.2 µH, C_{OUT} = 100 µF, and ESR = 75 mΩ the gain and phase bode diagrams are plotted respectively in *Figure 12* and *13* over input voltage range (V_{IN}=6 V to 48 V, I_{OUT}=3 A).

Figure 12. Module plot
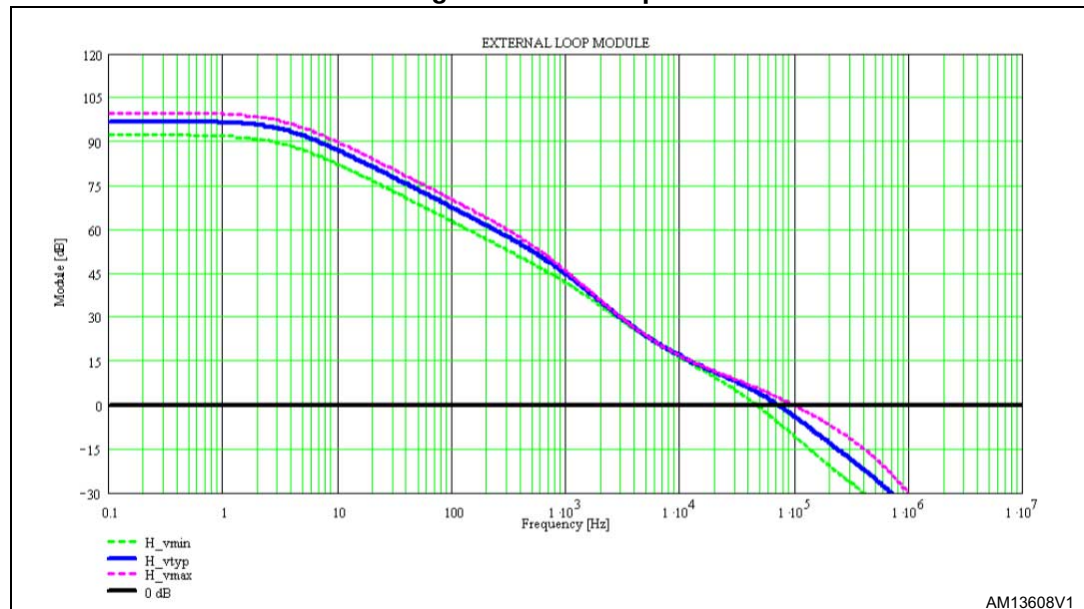
Figure 13. Phase plot

AM13609V1
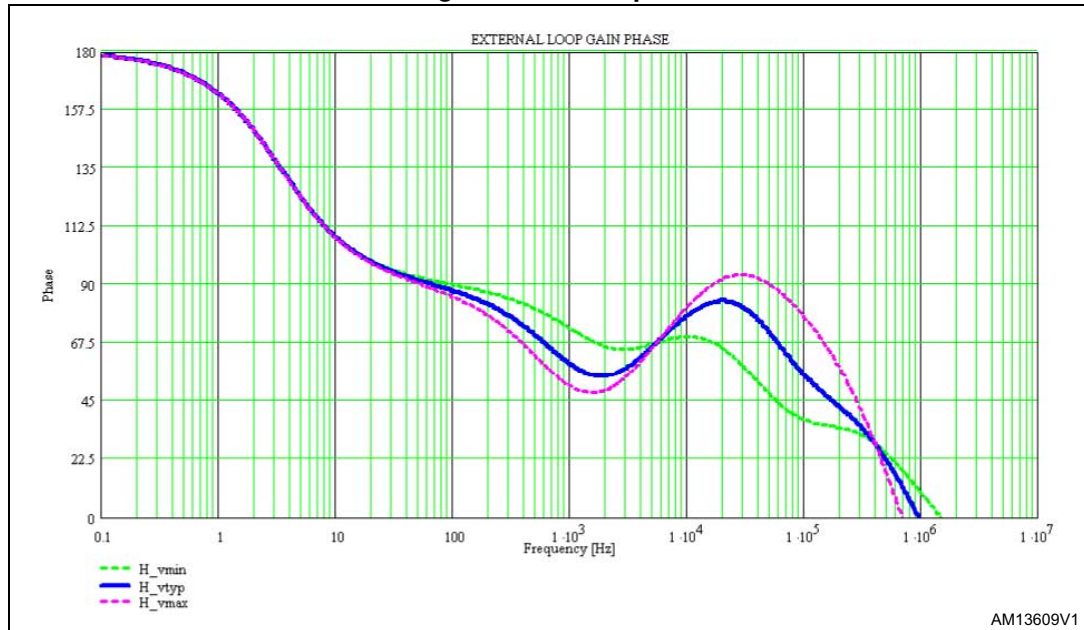
The cut-off frequency and the phase margin are:

Equation 16

$$V_{IN} = 6V \qquad f_C = 46 \text{ kHz} \qquad pm = 49°$$
$$V_{IN} = 12V \qquad f_C = 71 \text{ kHz} \qquad pm = 62°$$
$$V_{IN} = 48V \qquad f_C = 97 \text{ kHz} \qquad pm = 78°$$

7 Application information

7.1 Component selection

7.1.1 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, whose RMS value can be up to the load current divided by two (worst case, with duty cycle of 50 %). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS current flowing through the capacitor. The maximum RMS input current (flowing through the input capacitor) is:

Equation 17

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle, and I_O is the output DC current. Considering $\eta = 1$ this function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2. The maximum and minimum duty cycles are:

Equation 18

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 19

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the maximum IRMS going through the input capacitor. Capacitors that may be considered are:

Electrolytic capacitors:

These are widely used due to their low cost and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

Tantalum capacitors:

Small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is suggested to avoid this type of capacitor for the input filter of the device as they could be stressed by a high surge current when connected to the power supply.

Table 8. List of ceramic capacitors for the ST1S14

Manufacturer	Series	Capacitor value (μ)	Rated voltage (V)
TAIYO YUDEN	UMK325BJ106MM-T	10	50
MURATA	GRM42-2 X7R 475K 50	4.7	50

If the selected capacitor is ceramic (so neglecting the ESR contribution), the input voltage ripple can be calculated as:

Equation 20

$$V_{IN\,PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1-D) \right]$$

7.1.2 Output capacitor

The output capacitor is very important to meet the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but it increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to a very high frequency, its effect is negligible.

Ceramic capacitors

Ceramic capacitors and very low ESR capacitors that introduce a zero outside the designed bandwidth (f_Z=1/(2*pi*ESR*C_{OUT}, see *Section 6: Closing the loop*) in general should be avoided. A leading network across the upper resistor of the voltage divider is useful to increase the phase margin and compensate the system (see *Section 6.3: Voltage divider*). The effectiveness of the leading network increases at high output voltage because the singularities become more split.

High ESR capacitors

The "high ESR capacitor" definition stands for a capacitor having an ESR value able to introduce a zero into the designed system bandwidth, which can be, as a general rule, up to f_{SW}/5 at maximum. Tantalum or electrolytic capacitors belong to this group.

Equation 21

$$f_Z = \frac{1}{2 \cdot \pi \cdot ESR \cdot COUT} < BW < \frac{f_{SW}}{5}$$

A list of some tantalum capacitor manufacturers is provided in *Table 9*.

Table 9. Output capacitor selection

Manufacturer	Series	Rated voltage (V)	Cap value (μF)[1]	ESR (mΩ)[1]
Nippon Chemicon	KZE	6.3 to 50		
Sanyo POSCAP[2]	TAE	4 to 16		
	THB/C/E	4 to 16	$f_Z = \dfrac{1}{2 \cdot \pi \cdot ESR \cdot COUT} < BW$	
AVX	TPS	4 to 35		

1. see *Section 6: Closing the loop* for the selection of the output capacitor

2. POSCAP capacitors have some characteristics which are very similar to tantalum.

7.1.3 Inductor

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20 - 40 % of I_{omax}, which is 0.6 - 1.2 A with I_{Omax} = 3 A. The approximate inductor value is obtained using the following formula:

Equation 22

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \cdot T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T. For example, with V_{OUT} = 3.3 V, V_{IN} = 24 V, and ΔI_O = 0.8 A, the inductor value is about 4.7 µH. The peak current through the inductor is given by:

Equation 23

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In *Table 10*, some inductor manufacturers are listed.

Table 10. Inductor selection

Manufacturer	Series	Inductor value (μH)	Saturation current (A)
Wurth Elektronik	WE-HCI 7040	1 to 4.7	20 to 7
	WE-HCI 7050	4.9 to 10	20 to 4.0
Coilcraft	XPL 7030	2.2 to 10	29 to 7.2

7.2 Layout considerations

The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so

high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in *Figure 14* below.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device in order to avoid pick-up noise. Another important issue is the ground plane of the board. As the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction-to-ambient.

To increase the design noise immunity, different signal and power ground should be implemented in the layout (see *Section 7.5: Application circuit*). The signal ground serves the small signal components, the device ground pin, the exposed pad, and a small filtering capacitor connected to the VCC pin. The power ground serves the external diode and the input filter. The different grounds are connected underneath the output capacitor. Neglecting the current ripple contribution, the current flowing through this component is constant during the switching activity and so this is the cleanest ground point of the buck application circuit.

Figure 14. Layout example