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# ST2100

# Broadband powerline communication SoC optimized for audio/video streaming and consumer applications

**Datasheet - production data**


**TFBGA 12 x 12 x 1.2 mm**

## Features

- Configurable HW engine for multiple HomePlug® PHY and real-time MAC layers processing supporting:
  - HomePlug AV and 1.0 standards
  - HomePlug Green PHY™ standard
- Integrated analog front-end
- ARM926EJ-S™ 32-bit RISC CPU up to 333 MHz
- 8/16 bit DDR mobile at 166 MHz and DDR2 at 333 MHz memory controller
- Serial memory interface
- 8/16-bits NOR Flash/NAND Flash and SRAM memories controllers
- Multichannel DMA controller
- Ethernet 10/100 MAC with MII interface
- USB 2.0
- PCI Express and S-ATA
- Color LCD (CLCD) controller
- JPEG codec accelerator
- Cryptographic coprocessor
- Up to 40 GPIOs
- Enhanced $I^2S$ (digital audio interface)
- $I^2C$ master/slave mode
- Master/slave SSI
- Two independent UARTs
- Fast IrDA®
- Real-time clock
- Configurable serial port (SPORT) interface for external DSP and audio codec (ADC and DAC) in $I^2S$ mode
- Transport stream interface (video TS)
- Vectored interrupt controller (VIC)
- JTAG (IEEE1149.1) interface
- Three CPU instruction sets

## Applications

The STreamPlug ST2100 is configurable for a wide range of powerline applications such as:

- Smart gateway
- Powerline communication bridging, including wireless
- Smart grid
- Electromobility
- In house audio/video distribution
- Video surveillance
- Home automation
- “Network Area Storage” (NAS)
- Display panels control

**Table 1. Device summary**

| Order code | Operating temp. range | Package | Packing |
|---|---|---|---|
| ST2100 | -40 to +85 °C | TFBGA 12 x 12 x 1.2 mm, pitch 0.5 mm | Tray, tape and reel |

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# 1 Description

The STreamPlug ST2100 device is the STMicroelectronics® “Broad Band Powerline Communication” (BB PLC) solution, based on the powerful ARM926EJ-S™ processor (up to 333 MHz), widely used in applications where high computation performance is required, such as consumer (“Home Area Network” or HAN), industrial and smart grid applications.

In addition, the STreamPlug ST2100 has a memory management unit (MMU) that allows virtual memory management - making the system compliant with the Linux® operating system. It also offers 16 Kbyte of data cache, 32 Kbyte of instruction cache, JTAG and ETM™ (Embedded Trace Macrocell™ ) for debug operations.

A large set of peripherals allows a wide flexibility of the usage of the system in most of the possible PLC broadband applications (indoor and outdoor).

# 2 Main features

- Configurable hardware engine for multiple HomePlug PHY and real-time MAC layers
  - HomePlug™ AV and 1.0 standards
  - HomePlug Green PHY standard
- Integrated analog front-end
  - Programmable gain amplifier: gain range -12 dB to 48 dB
  - ADC and DAC
  - 2.5 V voltage regulator
  - Zero crossing (ZC) comparator
- ARM926EJ-S™ 32-bit RISC CPU up to 333 MHz
  - 16 Kbyte if instruction cache, 16 Kbyte of data cache
  - 32 Kbyte of instruction TCM and 16 Kbyte of data TCM
  - Three instruction sets: 32-bit for high performance, 16-bit (Thumb®) for efficient code density, bytecode Java™ mode (Jazelle™) for direct execution of Java code
  - AMBA™ bus interface with $f_{MAX}$ 166 MHz
- 48 Kbyte on-chip boot ROM
- 8 Kbyte on-chip SRAM
- 8/16 bit DDR mobile at 166 MHz and DDR2 at 333 MHz memory controller
- Serial memory interface
- 8/16-bits NOR Flash/NAND Flash and SRAM memory controller
- Boot capability from NAND Flash, serial/parallel NOR Flash, and UART
- Multichannel DMA controller (8 FIFOs and 16 dedicated channels)
- Ethernet 10/100 MAC with MII interface (IEEE 802.3), RevMII, IEEE 802.1-AS and 802.1-Qav for audio video (AV) traffic
- USB 2.0 (high-full-low speed) port with an integrated PHY able to work as a host or device
- PCI Express GEN1 (PCI Express standard version 1.1), single lane X1 dual mode (both “Root Complex” and “Endpoint” modes supported), the PHY is a standard 8-bit/16-bit PIPE PHY interface. This peripheral supports also the serial ATA compliant with the SATA/150.
- Color LCD controller (up to 1024 x 768 resolution at 24 bpp true color, STN/TFT display panels)
- JPEG codec accelerator (1 clock/pixel)
- Cryptographic coprocessor (DMA based programmable engine) with support for:
  - Advanced encryption standard (AES) cipher (128, 192, 256 bit keys) in ECB, CBC, CTR modes
  - Data encryption standard (DES) and triple DES (TDES) cipher in ECB and CBC modes
  - SHA-1, HMAC-SHA-1, SHA-256, HMAC-SHA-256, MD5, HMAC-MD5 digests
- Up to 40 GPIOs (multiplexed with peripheral I/Os), all the I/Os have interrupt capability, 24 application specific GPIOs: four I/Os support PWM and four I/Os support double PWM features.

- Enhanced $I^2S$ for 4-channel “Digital Audio Interface“ (DAI)
- Master/slave SSP (Motorola SPI, Texas Instruments, National Semiconductor protocols) up to 5 Mbits/s in slave mode and up to 20 Mbits/s in master mode
- $I^2C$ master/slave mode
- Two independent UARTs supporting hardware (HW) flow control
- Fast IrDA (SIR/MIR/FIR)
- Three pairs of 16-bit general purpose timers with programmable 8-bit prescaler
- Real-time clock (RTC)
- Configurable serial port (SPORT) interface for external DSP and audio codec (ADC and DAC in $I^2S$ mode)
- Transport stream interface (Video TS also called “Synchronous peripheral bus”) for external MPEG- 2/H.264 encoder and decoder. TS port also implements image sensor interface (CCD camera)
- Watchdog timer
- Clock synthesizer (4 outputs)
- Vectored interrupt controller (VIC)
- JTAG (IEEE1149.1) interface
- ETM9 interface
- Multichannel cryptographic coprocessor. DES/TDES and AES security for the powerline link
- PGC (IR) interface
- Supply voltages: 1.2 V core, 1.8 V / 2.5 V DDR, 2.5 V AFE and PLLs, 1.5 V RTC and 3.3 V I/Os
- Available in a TFBGA373 package (12 x 12 x 1.2 mm, pitch 0.5 mm).

# 3 Architecture description

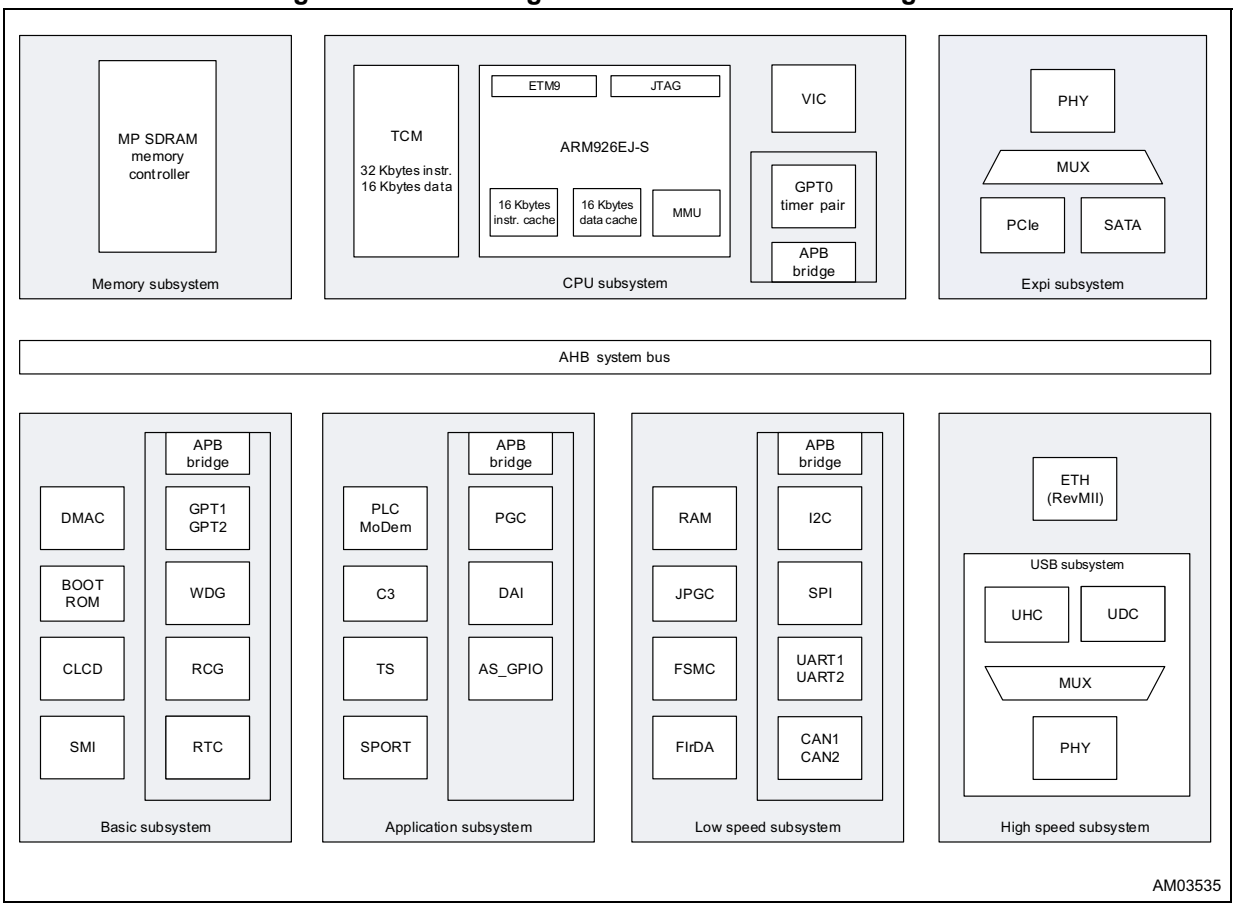
*Figure 1* is the architecture overview of the STreamPlug ST2100.

The internal architecture is based on several shared subsystems interconnected through a multilayer system bus.

The bus structure allows different subsystem data flows to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency.

**Figure 1. STreamPlug ST2100 functional block diagram**



## 3.1 CPU subsystem

- ARM926EJ-S™ running at 333 MHz with:
  - MMU
  - 16 Kbyte of instruction cache
  - 16 Kbyte of data cache
  - 32 Kbyte of instruction “Tightly Coupled Memory“ (TCM)
  - 16 Kbyte of data “Tightly Coupled Memory” (TCM)
  - AMBA bus interface
  - JTAG
  - ETM9 (Embedded Trace Macrocell) for debug, medium size version
- Interrupt controller managing sources which are prioritized and vectorized

## 3.2 System bus

The system bus structure allows different subsystem data flows to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

*Table 2* shows the system bus scheme and *Table 3* is the key to its contents.

**Table 2. System bus connectivity**

| | | CPU | PCIe/SATA | DMA 1 | DMA 2 | Eth. | TS/SPORT | UHC/UDC | PLC modem | Crypto | CLCD |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Targets (slave ports)** | MP SDRAM | X | X | X | X | X | X | X | X | X | X |
| | Low speed | X | X | X | | | | | | | |
| | Application | X | X | | X | | | | | | |
| | Basic | X | X | | | | | | | | |
| | High speed | X | X | | | | | | | | |
| | Expi | X | | | X | | | | | | |

**Table 3. Key to system bus connectivity matrix**

| Format | Definition |
|---|---|
| **Grey box** | No connection exists between target and initiator |
| X | A connection exists between target and initiator |

## 3.3 Memory subsystem

The multiport memory controller within the memory subsystem manages DDR mobile up to 166 MHz and DDR2 up to 333 MHz external memory. Internally, it handles 5 ports supporting all the chip master ports.

The multiport memory controller block has a programmable arbitration scheme and the transactions happen on a different layer from the main bus. It also offers a local FIFO to increase the throughput and reduce the latency.

## 3.4 Expi subsystem

- PCI Express Gen1 (PCI Express standard version 1.1) single lane X1 dual mode
  - Root Complex mode is supported.
  - Endpoint mode is supported.
- Serial ATA compliant with SATA/150 specifications
- PHY is standard 8-bit/16-bit PIPE PHY interface

## 3.5 Basic subsystem

- 8 FIFOs and 16 high performance DMA channels with two AHB interfaces to parallelize the activity when two channels are working at the same time.
- 48 Kbytes of ROM (for boot procedure)
- “Serial Memory Interface” (SMI) supporting external serial Flash.
- Color LCD controller (CLCD) up to 1024 x 768 resolution at 24 bpp (true color) supporting STN/TFT display panels
- Three pair of 16 bit general purpose timers with programmable prescaler
- Watchdog timer
- RTC with separate power supply allowing battery connection
- Up to 104 “Multi-Function” I/Os (MFIOs) multiplexed with peripheral I/Os:
  - Allows a large number of possible application scenarios
  - Up to 40 GPIOs with interrupt capability
- System controller, reset and clock generation, and miscellaneous registers array allowing a full configurability of the system.

## 3.6 High-speed connectivity subsystem

- Ethernet 10/100 MAC with MII interface (IEEE 802.3), with external PHY
  - RevMII (supporting 25 and 50 MHz clock frequencies)
  - IEEE 802.1-AS and 802.1-Qav for audio video (AV) traffic
- USB 2.0 (high-full-low speed) port with integrated PHY able to work as a host or device. The PHY is embedded.
  - One USB host controller compatible with USB 2.0 high-speed specification managing a single port. The peripheral has a dedicated channel to the multiport memory controller and a dedicated slave port for CPU programming (OHCI and EHCI).
  - One USB device compatible with USB 2.0 high-speed specifications. A dedicated channel connects the peripheral with the multiport memory controller and registers and an internal FIFO are accessible from the CPU through the main AHB bus. A USB plug detector block is also available to detect the presence of the VBUS voltage.

## 3.7 Low-speed connectivity subsystem

- Two independent UARTs supporting hardware flow control up to 460.8 Kbits/s
- Fast IrDA controller with a speed rate from 9.6 Kbits/s to 4 Mbits/s (SIR/MIR/FIR)
- One synchronous “Serial Port Interface” (SPI) controller capable of operating as a master or a slave (Motorola - Texas Instruments - National Semiconductor) with a speed (data) rate up to 20 Mbits/s
- One $I^2C$ (also known as a digital audio interface) controller capable of operating in master and slave mode and covering all the possible data rates (high, fast and low)
- JPEG codec accelerator (1 clock per pixel)
- 8 Kbytes of static RAM
- “Flexible Static Memory Controller” (FSMC) supporting:
  - Asynchronous parallel NAND and NOR Flash memories
  - Synchronous and asynchronous SRAM
- Two independent “Controller Area Network” (CAN) interfaces compliant with CAN protocol version 2.0 parts A and B (up to 1 Mbit/s).

## 3.8 Application subsystem

- Configurable hardware engine for multiple HomePlug PHY and real-time MAC layers processing supporting:
  - HomePlug AV and 1.0 standards
  - HomePlug Green PHY standard
- Integrated analog front-end:
  - Programmable gain amplifier: gain range -12 dB to 48 dB
  - ADC and DAC
  - 2.5 V, 150 mA voltage regulator
  - Zero crossing (ZC) comparator
- Cryptographic coprocessor channels (C3), DMA based programmable engine, with support for:
  - Advanced encryption standard (AES) cipher (128-, 192-, 256-bit keys) in ECB, CBC, CTR modes
  - Data encryption standard (DES) and triple DES cipher in ECB and CBC modes
  - SHA-1, HMAC-SHA-1, SHA-256, HMAC-SHA-256, MD5, HMAC-MD5 digests algorithms
- Configurable serial port (SPORT) interface for external DSP and audio codec (ADC and DAC in $I^2S$ mode)
- Transport stream (TS) interface
- Pulse generator and capture (PGC) (IR) for remote controls
- 4-channel $I^2S$ [“Digital Audio Interface” (DAI)]
- 24 application specific GPIOs:
  - Up to 4 GPIOs supporting PWM
  - Up to 4 GPIOs supporting double PWM.

## 3.9 Clock and reset system

- The system clocks are generated by:
  - Two fully programmable PLLs. One is used to generate a clock for CPU and AMBA AHB bus and the other is used in case the DDR clock has to be different (asynchronous) with respect to the CPU clock.
  - One “high precision” clock synthesizer with 4 outputs providing different frequencies for the various IPs
- Fully programmable control of the clock and reset signals for all the slave blocks allowing sophisticated power management.

# 4 Pin descriptions

From *Table 4* to *Table 15 on page 21* and *Table 16* in *Section 5 on page 29* describe the STreamPlug ST2100 pinouts.

## 4.1 Dedicated pins

**Table 4. Master clock RTC, RESET and 3.3 V comparator pin descriptions**

| Group | Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|---|
| Master clock | RCG_MCLK_A | AB18 | In | 24 MHz (typical) crystal in | Oscillator 2.5 V capable |
| | RCG_MCLK_ZO | AB19 | Out | 24 MHz (typical) crystal out | Oscillator 2.5 V capable |
| RTC | RTC_TST | G23 | In | POR test signal | Keep it at GND |
| | RTC_ZO | H22 | Out | 32 KHz crystal output | Oscillator 1.5 V capable |
| | RTC_A | H23 | In | 32 KHz crystal input | Oscillator 1.5 V capable |
| | RTC_SGN | J23 | In | POR signal | Keep it floating |
| RESET | MRESET | Y13 | In | Main reset | TTL Schmitt trigger input buffer 3.3 V tolerant with PU |
| 3.3 V comp. | COMP_3V3_ ANAREXT | A21 | Power | External resistor for 3.3 V I/Os compensation | Analog, 3.3 V capable |
| | COMP_3V3_ GNDBGCOMP | A22 | Power | Return for external resistor for 3.3 V I/Os compensation | |

**Table 5. Power supply pin descriptions**

| Group | Signal name | Ball | Value |
|---|---|---|---|
| DIGITAL GROUND | GND | A1, A23, D5, D20, J11, J13, K10,K11, K12, K13, K14,K22, L10, L11, L12, L13, L14, L21, M1, M4, M10, M11, M12, M13, M14, M20, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14, R11, R13, R22, AC1, AC23, AB23 | 0 V |
| | DVSS_USB | AB17 | |
| | GND_ADC | V21 | |
| | GND_DAC | T23 | |
| | GND_RCG_CLK_SYNTH | AA19 | |

**Table 5. Power supply pin descriptions (continued)**

| Group | Signal name | Ball | Value |
|---|---|---|---|
| ANALOG GROUND | GNDE_RTC | J22 | 0 V |
| | VSSA_USB | AC16 | |
| | VSSA_USB | AC13 | |
| | VSSAC_USB | AA15 | |
| | GNDAS_ADC | W21 | |
| | GNDA_ADC | W22 | |
| | GNDA1_DAC | V20 | |
| | GNDA2_DAC | T22 | |
| | GNDAS_DAC | U20 | |
| | DAC_MASS_QUIET | U22 | |
| | GNDE_DAC | W20 | |
| | GNDE_RCG_MCLK | AC19 | |
| | AGNDSUB_RCG_MCLK | Y17 | |
| | AGND_RCG_MCLK | AA17 | |
| | AGND_PLL1 | Y15 | |
| | AGND_PLL2 | W17 | |
| | GNDA_RCG_CLK_SYNTH | Y20 | |
| | GNDE_REG | AB22 | |
| | GNDE_PGA | AB21 | |
| | PCIE_P1_VSSR | K23 | |
| | PCIE_P1_VSSR | M23 | |
| | PCIE_P1_VSST | N23 | |
| | PCIE_VSS_PLL | P21 | |
| | PCIE_P1_VSST | R23 | |
| I/O | VDDE_3V3 | E5, E6, E7, E17, E18, E19, F5, F19, G5, G19, U5, U19, V5, V19, W5, W6, W7, W18, W19 | 3.3 V |
| CORE | VDD_1V2 | J9, J10, J12, J14, J15, K9, K15, L9, L15, M9, M15, N9, N15, P9, P15, R9, R10, R12, R14, R15, AA21 | 1.2 V |
| USB PHY | VDD_1V2_USB | AB15 | 1.2 V |
| | VDD_2V5_USB | AA16 | 2.5 V |
| | VDD_3V3_USB | AB16 | 3.3 V |

Table 5. Power supply pin descriptions (continued)

| Group | Signal name | Ball | Value |
|---|---|---|---|
| ANALOG GROUND | GNDE_RTC | J22 | 0 V |
| | VSSA_USB | AC16 | |
| | VSSA_USB | AC13 | |
| | VSSAC_USB | AA15 | |
| | GNDAS_ADC | W21 | |
| | GNDA_ADC | W22 | |
| | GNDA1_DAC | V20 | |
| | GNDA2_DAC | T22 | |
| | GNDAS_DAC | U20 | |
| | DAC_MASS_QUIET | U22 | |
| | GNDE_DAC | W20 | |
| | GNDE_RCG_MCLK | AC19 | |
| | AGNDSUB_RCG_MCLK | Y17 | |
| | AGND_RCG_MCLK | AA17 | |
| | AGND_PLL1 | Y15 | |
| | AGND_PLL2 | W17 | |
| | GNDA_RCG_CLK_SYNTH | Y20 | |
| | GNDE_REG | AB22 | |
| | GNDE_PGA | AB21 | |
| | PCIE_P1_VSSR | K23 | |
| | PCIE_P1_VSSR | M23 | |
| | PCIE_P1_VSST | N23 | |
| | PCIE_VSS_PLL | P21 | |
| | PCIE_P1_VSST | R23 | |
| I/O | VDDE_3V3 | E5, E6, E7, E17, E18, E19, F5, F19, G5, G19, U5, U19, V5, V19, W5, W6, W7, W18, W19 | 3.3 V |
| CORE | VDD_1V2 | J9, J10, J12, J14, J15, K9, K15, L9, L15, M9, M15, N9, N15, P9, P15, R9, R10, R12, R14, R15, AA21 | 1.2 V |
| USB PHY | VDD_1V2_USB | AB15 | 1.2 V |
| | VDD_2V5_USB | AA16 | 2.5 V |
| | VDD_3V3_USB | AB16 | 3.3 V |

**Table 5. Power supply pin descriptions (continued)**

| Group | Signal name | Ball | Value |
|---|---|---|---|
| PCIe PHY | PCIE_VDD_PLL | M21 | 1.2 V |
| | PCIE_P1_VDDR | M22 | 1.2 V |
| | PCIE_P1_VDDT1 | N21 | 1.2 V |
| | PCIE_P1_VDDT2 | N22 | 2.5 V |
| | PCIE_VDD2_PLL | R21 | 2.5 V |
| OSCI (master clock) | VDD_1V2_RCG_MCLK | AA18 | 1.2 V |
| | VDDE_2V5_RCG_MCLK | AC18 | 2.5 V |
| PLL 1 | AVDD_2V5_PLL1 | Y16 | 2.5 V |
| PLL 2 | AVDD_2V5_PLL2 | Y14 | 2.5 V |
| SYNTH | VDD_1V2_RCG_CLK_SYNTH | Y19 | 1.2 V |
| | VCCA_2V5_RCG_CLK_SYNTH | Y18 | 2.5 V |
| DDR | VDDE_DDR | A5, A11, A14, A20, C23, D6, D11, D14 | 1.8 V / 2.5 V |
| AFE_ADC | VDD_1V2_ADC | W23 | 1.2 V |
| | VCCAISO_2V5_ADC | Y21 | 2.5 V |
| | VCCA_2V5_ADC | Y23 | 2.5 V |
| AFE_DAC | VDD_1V2_DAC | T21 | 1.2 V |
| | VCCA1_2V5_DAC | U21 | 2.5 V |
| | VCCA2_2V5_DAC | T20 | 2.5 V |
| AFE_PGA | VDD_2V5_PGA | AB20 | 2.5 V |
| | VDDE_3V3_PGA | AC20 | 3.3 V |
| OSCI RTC | VDD_1V5_RTC | G22 | 1.5 V |
| Internal 2.5 V regulator | VDDE_2V5_REG (REG OUT) | Y22 | 2.5 V |
| | VDDE_3V3_REG (REG IN) | AA22 | 3.3 V |
| Reserved | Reserved | AA23, B23, D21, D22, D23, E20, E21, E22, E23, F20, F21, F22, F23, G20, G21, H20, H21, J20, J21, K20, K21, L20 | Keep it floating |
| Reserved | Reserved | B22 | Connect to GND |

**Table 6. Debug pin descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| Reserved | B4 | In | Reserved<br>Connect to GND | TTL input buffer, 3.3 V tolerant with PD |
| JTAG_TMS | C5 | In | Test mode select | TTL input buffer, 3.3 V tolerant with PU |
| JTAG_TCK | D4 | In | Test clock | TTL input buffer, 3.3 V tolerant with PU |
| JTAG_NTRST | E4 | In | Test reset input | TTL input buffer, 3.3 V tolerant with PU |
| JTAG_TDI | F4 | In | Test data input | TTL input buffer, 3.3 V tolerant with PU |
| JTAG_TDO | G4 | Out | Test data output | TTL output buffer, 3.3 V capable, 4 mA |
| ETM_TRACECLK | Y7 | Out | ETM clock (the other ETM signals are available on MFIOs) | TTL output buffer, 3.3 V capable, 4 mA |

**Table 7. Boot source descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| SOC_CFG_BOOT0 | C2 | In | Boot mode configuration | TTL input buffer, 3.3 V tolerant with PD |
| SOC_CFG_BOOT1 | B2 | In | Boot mode configuration | TTL input buffer, 3.3 V tolerant with PD |
| SOC_CFG_BOOT2 | C3 | In | Boot mode configuration | TTL input buffer, 3.3 V tolerant with PD |
| SOC_CFG_BOOT3 | B3 | In | Boot mode configuration | TTL input buffer, 3.3 V tolerant with PD |

**Table 8. Boot source selection**

| Boot source | SOC_CFG_BOOT3 | SOC_CFG_BOOT2 | SOC_CFG_BOOT1 | SOC_CFG_BOOT0 |
|---|---|---|---|---|
| SMI (3-byte addressing) | 0 | 0 | 0 | 0 |
| SMI (2-byte addressing) | 0 | 0 | 0 | 1 |
| FSMC/NAND 8-bit | 0 | 0 | 1 | 0 |
| FSMC/NAND 16-bit | 0 | 0 | 1 | 1 |
| UART1 (G20) | 0 | 1 | 0 | 0 |
| UART2(G21) | 0 | 1 | 0 | 1 |
| FSMC/NOR 8-bit | 0 | 1 | 1 | 0 |
| FSMC/NOR 16-bit | 0 | 1 | 1 | 1 |
| Reserved | 1 | X(1) | X(1) | X(1) |

1. An “X” may be a “1” or a “0”.

**Table 9. SMI pin descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| SMI_DIN | A2 | In | Serial Flash input data | TTL input buffer, 3.3 V tolerant with configurable PU/PD and HYST |
| SMI_DOUT | A3 | Out | Serial Flash output data | TTL output buffer, 3.3 V capable, 4 mA |
| SMI_CLK | A4 | I/O | Serial Flash clock | TTL output buffer, 3.3 V capable, 4 mA |
| SMI_NCS0 | B1 | Out | Serial Flash chip select | TTL output buffer, 3.3 V capable, 4 mA |
| SMI_NCS1 | C1 | Out | Serial Flash chip select | TTL output buffer, 3.3 V capable, 4 mA |
| SMI_NCS2 | D1 | Out | Serial Flash chip select | TTL output buffer, 3.3 V capable, 4 mA |

**Table 10. USB Pin descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| USB_VBUS | AA14 | I/O | USB device VBUS detect or USB host VBUS control | Bidirectional TTL pad, 3.3 V tolerant input with PD for device mode; output for host mode |
| USB_OVERCUR | AB13 | In | USB host overcurrent | TTL input buffer 3.3 V tolerant with PU (for host mode only) |
| USB_TXRTUNE | AB14 | Out | Reference resistor | Analog |
| USB_DP | AC14 | I/O | USB host or device D+ | Bidirectional analog buffer 5 V tolerant |
| USB_DM | AC15 | | USB host or device D- | Bidirectional analog buffer 5 V tolerant |
| Reserved | AC17 | Out | Do not connect test output | Analog |

**Table 11. PCIe / SATA pin descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| PCIE_P1_RXN | L22 | In | High frequency negative RX input signal | Analog |
| PCIE_P1_RXP | L23 | In | High frequency positive RX input signal | Analog |
| PCIE_XTAL2 | N20 | Out | Feedback of the crystal oscillator | Oscillator |
| PCIE_XTAL1 | P20 | In | Input of the crystal oscillator | Oscillator |
| PCIE_P1_TXP | P22 | Out | High frequency positive TX output signal | Analog |
| PCIE_P1_TXN | P23 | Out | High frequency negative TX output signal | Analog |
| PCIE_REFRES | R20 | Input | Reference resistor for the impedance compensation | Analog |

**Table 12. Internal AFE pin descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| DAC_IDAC | U23 | Out | HF DAC differential positive current “Out” | Analog |
| DAC_REXT | V22 | Out | External precision resistor | Analog |
| DAC_IDACB | V23 | Out | HF DAC differential negative current “Out” | Analog |
| PGA_IN_N | AC21 | In | PGA negative input | Analog |
| PGA_IN_P | AC22 | In | PGA positive input | Analog |

**Table 13. AC crossing pin descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| AC_CROSSING | C4 | In | Mains digital input, zero crossing | TTL input buffer, 3.3 V tolerant, with configurable PU/PD and HYST |
| ZC_IN | AA20 | In | Mains analog zero crossing | Analog |

**Table 14. External PLI pin description**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| EXTPLI_TXON | C22 | Out | Line driver enable | TTL output buffer, 3.3 V capable, 4 mA |

**Table 15. DDR pin descriptions**

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| DDR_ADDR_0 | D7 | Out | Address lines | Compatible with DDRI (SSTL2) and DDRII (SSTL18) |
| DDR_ADDR_1 | C7 | | | |
| DDR_ADDR_2 | B7 | | | |
| DDR_ADDR_3 | A8 | | | |
| DDR_ADDR_4 | B8 | | | |
| DDR_ADDR_5 | C8 | | | |
| DDR_ADDR_6 | D8 | | | |
| DDR_ADDR_7 | A9 | | | |
| DDR_ADDR_8 | B9 | | | |
| DDR_ADDR_9 | C9 | | | |
| DDR_ADDR_10 | D9 | | | |
| DDR_ADDR_11 | A10 | | | |
| DDR_ADDR_12 | B10 | | | |
| DDR_ADDR_13 | C10 | | | |
| DDR_ADDR_14 | D10 | | | |
| DDR_BA_0 | C11 | Out | Bank select | |
| DDR_BA_1 | D12 | | | |
| DDR_BA_2 | C12 | | | |
| DDR_RAS | B14 | Out | Row address strobe | |
| DDR_CAS | B13 | Out | Column address strobe | |
| DDR_WE | B11 | Out | Write enable | |
| DDR_CLKEN | B12 | Out | Clock enable | |
| DDR_CLK_P | A12 | Out | Differential clock | Differential Compatible with DDRI (SSTL2) and DDRII (SSTL18) |
| DDR_CLK_N | A13 | | | |

Table 15. DDR pin descriptions (continued)

| Signal name | Ball | Direction | Function | Pin type |
|---|---|---|---|---|
| DDR_CS_0 | C13 | Out | Chip select | Compatible with DDRI (SSTL2) and DDRII (SSTL18) |
| DDR_CS_1 | C14 | | | |
| DDR_ODT_1 | A6 | I/O | On-die termination enable lines | |
| DDR_ODT_0 | A7 | | | |
| DDR_DATA_0 | D15 | I/O | Data lines (lower byte) | |
| DDR_DATA_1 | C15 | | | |
| DDR_DATA_2 | D16 | | | |
| DDR_DATA_3 | C16 | | | |
| DDR_DATA_4 | C18 | | | |
| DDR_DATA_5 | D18 | | | |
| DDR_DATA_6 | C17 | | | |
| DDR_DATA_7 | D17 | | | |
| DDR_DQS_0 | A15 | Out | Lower data strobe | Differential Compatible with DDRI (SSTL2) and DDRII (SSTL18) |
| DDR_NDQS_0 | A16 | | | |
| DDR_DM_0 | B15 | Out | Lower data mask | Compatible with DDRI (SSTL2) and DDRII (SSTL18) |
| DDR_GATE_0 | A17 | I/O | Lower gate open | |
| DDR_DATA_8 | C21 | I/O | Data lines (upper byte) | |
| DDR_DATA_9 | B21 | | | |
| DDR_DATA_10 | C20 | | | |
| DDR_DATA_11 | B20 | | | |
| DDR_DATA_12 | D19 | | | |
| DDR_DATA_13 | C19 | | | |
| DDR_DATA_14 | B19 | | | |
| DDR_DATA_15 | B18 | | | |
| DDR_DQS_1 | A18 | Out | Upper data strobe | Differential Compatible with DDRI (SSTL2) and DDRII (SSTL18) |
| DDR_NDQS_1 | A19 | | | |
| DDR_DM_1 | B16 | Out | Upper data mask | Compatible with DDRI (SSTL2) and DDRII (SSTL18) |
| DDR_GATE_1 | B17 | I/O | Upper gate open | |
| VREF_DDR | D13 | In | Reference voltage | Analog 1.8 V |
| DDR2_EN | B5 | In | Configuration | TTL input buffer, 3.3 V tolerant, with PU |
| COMP_1V8_ANAREXT | B6 | Power | External resistor for 1.8 V I/Os compensation | Analog 1.8 V capable |
| COMP_1V8_GNDBGCOMP | C6 | Power | Return for external resistor for 1.8 V I/Os compensation | Power |

## 4.2 Shared I/O pins (MFIOs)

The 104 MFIOs can be configured in different modes. This allows the STreamPlug ST2100 to be tailored for various applications.

For the MFIO from 88 to 103, the signal specified in *Table 16* is also conditioned by an internal selection MUX that can choose among the specified signal and an internal basic subsystem general purpose IO (BS_GPIO), as specified in the STreamPlug ST2100 manual and shown in *Figure 2* and *Figure 3*.

**Figure 2. MIFO 0-87 muxing scheme**

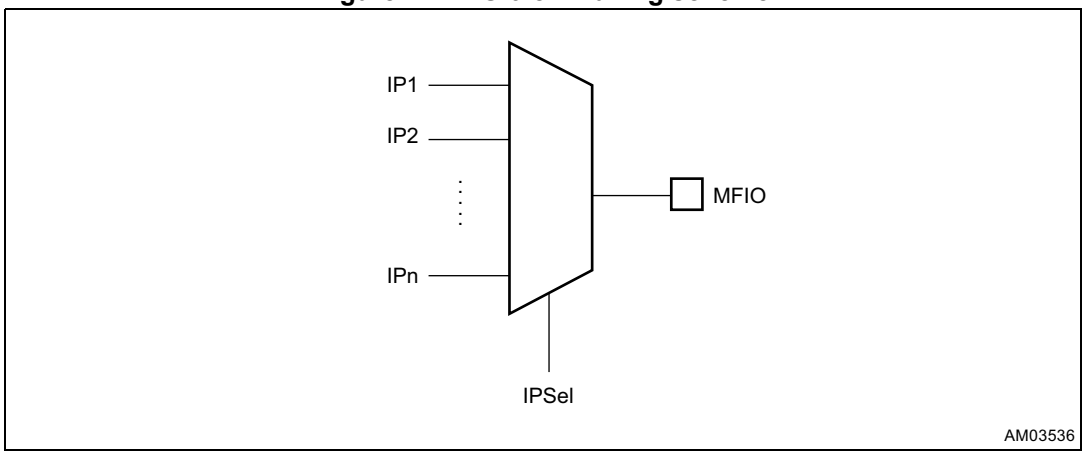



**Figure 3. MFIO 88-103 muxing scheme**

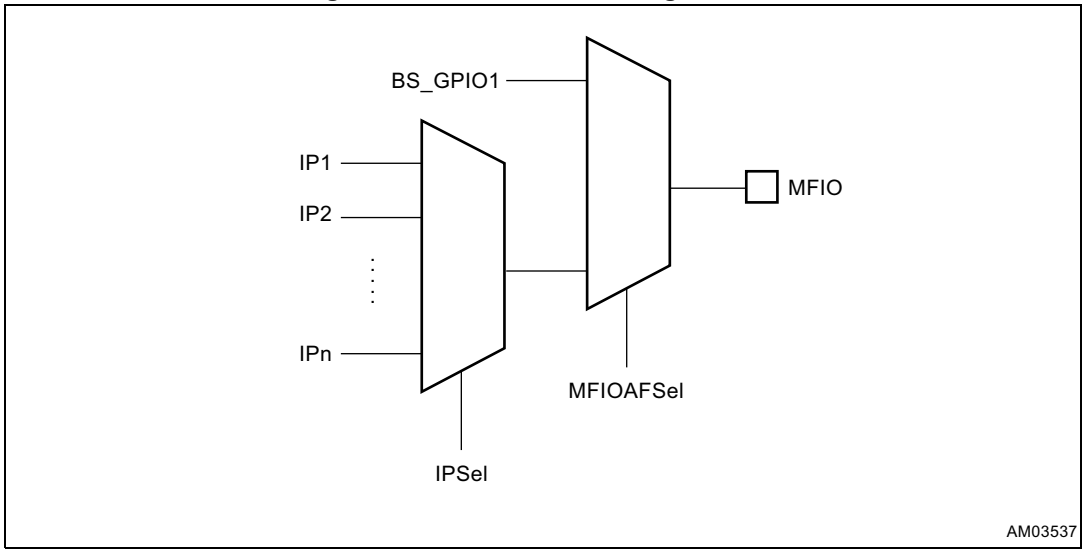


**Table 16. MFIO pin descriptions**

| Ball no. | Signal name | Muxing selection | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| AB9 | MFIO0 | eth_phy_int | FSMC_BLn0 | FSMC_PCSel0 | | | ETM_TRACEPKTA_0 |
| AA8 | MFIO1 | eth_clk | FSMC_BLn1 | FSMC_PCSel1 | | | ETM_TRACEPKTA_1 |
| AB6 | MFIO2 | MII_TXER | FSMC_PCOEn | FSMC_PCOEn | | | ETM_TRACEPKTA_2 |
| AA7 | MFIO3 | MII_TXEN | FSMC_PCWEn | FSMC_PCWEn | | | ETM_TRACEPKTA_3 |
| AA9 | MFIO4 | MII_TXD_3 | FSMC_Ebar0 | FSMC_PCIntRq_1 | | | ETM_TRACEPKTB_0 |
| AB7 | MFIO5 | MII_TXD_2 | FSMC_Ebar1 | FSMC_PCIntRq_2 | | | ETM_TRACEPKTB_1 |
| AA6 | MFIO6 | MII_TXD_1 | FSMC_Ebar2 | FSMC_PCAD16(CLE) | | | ETM_TRACEPKTB_2 |
| AB8 | MFIO7 | MII_TXD_0 | FSMC_Ebar3 | FSMC_PCAD17(ALE) | | | ETM_TRACEPKTB_3 |
| AB5 | MFIO8 | MII_TXCLK | FSMC_PCDa0 | | | | ETM_TRACE_SYNCA |
| AC8 | MFIO9 | MII_RXER | FSMC_PCDa1 | | | | ETM_PIPESTATA_0 |
| AC5 | MFIO10 | MII_RXDV | FSMC_PCDa2 | | | | ETM_PIPESTATA_1 |
| AC7 | MFIO11 | MII_RXD_3 | FSMC_PCDa3 | | | | ETM_PIPESTATA_2 |
| AB4 | MFIO12 | MII_RXD_2 | FSMC_PCDa4 | | | | ETM_TRACE_SYNCB |
| AC6 | MFIO13 | MII_RXD_1 | FSMC_PCDa5 | | | | ETM_PIPESTATB_0 |
| AA5 | MFIO14 | MII_RXD_0 | FSMC_PCDa6 | | | | ETM_PIPESTATB_1 |
| AC4 | MFIO15 | MII_RXCLK | FSMC_PCDa7 | | | | ETM_PIPESTATB_2 |
| AA4 | MFIO16 | MII_MDIO | FSMC_PCAD0 | | | | AS_GPIO8 |
| AC3 | MFIO17 | MII_MDC | FSMC_PCAD1 | | | | AS_GPIO9 |
| AB3 | MFIO18 | MII_CRS | FSMC_PCAD2 | | | | AS_GPIO10 |
| AC2 | MFIO19 | MII_COL | FSMC_PCAD3 | | | | AS_GPIO11 |
| Y3 | MFIO20 | UART2_CTS | FSMC_PCAD4 | | | | AS_GPIO12 |
| AB2 | MFIO21 | UART2_RTS | FSMC_PCAD5 | | | | AS_GPIO13 |

**Table 16. MFIO pin descriptions (continued)**

| Ball no. | Signal name | Muxing selection | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| Y4MFIO 22 | UART2_RXD | FSMC_PCAD6 | | | | AS_GPIO14 | |
| AA3 | MFIO23 | UART2_TXD | FSMC_PCAD7 | | | | AS_GPIO15 |
| Y5 | MFIO24 | UART1_CTS | FSMC_PCDa8 | | | | |
| AA1 | MFIO25 | UART1_RTS | FSMC_PCDa9 | | | | |
| Y6 | MFIO26 | UART1_RXD | FSMC_PCDa10 | | | | |
| AB1 | MFIO27 | UART1_TXD | FSMC_PCDa11 | | | | |
| W4 | MFIO28 | AS_GPIO4 | FSMC_PCDa12 | | | | |
| Y1 | MFIO29 | AS_GPIO5 | FSMC_PCDa13 | | | | |
| V3 | MFIO30 | AS_GPIO6 | FSMC_PCDa14 | | | | |
| V2 | MFIO31 | AS_GPIO7 | FSMC_PCDa15 | | | | |
| W3 | MFIO32 | AS_GPIO0 | FSMC_PCAD8 | | | | |
| Y2 | MFIO33 | AS_GPIO1 | FSMC_PCAD9 | | | | |
| U3 | MFIO34 | AS_GPIO2 | FSMC_PCAD10 | | | | |
| W2 | MFIO35 | AS_GPIO3 | FSMC_PCAD11 | | | | |
| V4 | MFIO36 | AS_GPIO8 | FSMC_PCAD12 | | | | |
| AA2 | MFIO37 | AS_GPIO9 | FSMC_PCAD13 | | | | |
| U2 | MFIO38 | AS_GPIO10 | FSMC_PCAD14 | | | | |
| W1 | MFIO39 | AS_GPIO11 | FSMC_PCAD15 | | | | |
| U4 | MFIO40 | AS_GPIO12 | | | | FSMC_PCAD16 | |
| V1 | MFIO41 | AS_GPIO13 | | | | FSMC_PCAD17 | |
| T3 | MFIO42 | AS_GPIO14 | PGC_IR_TX | FIrDA_RX | | FSMC_PCAD18 | |
| T1 | MFIO43 | AS_GPIO15 | PGC_IR_RX | FIrDA_TX | | FSMC_PCAD19 | |
| R4 | MFIO44 | SPORT_DRSEC2 | | | RxQuiet | FSMC_PCAD20 | |