Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

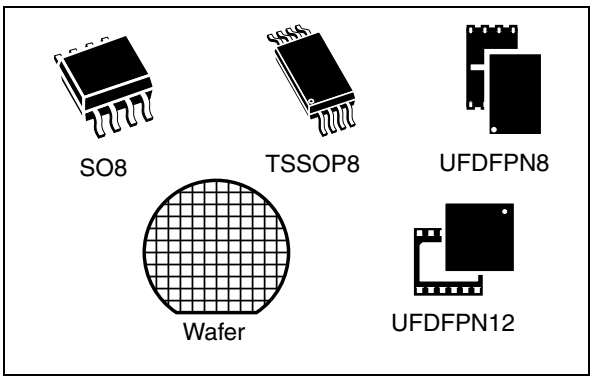
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ST25DVxxx

Dynamic NFC/RFID tag IC with 4-Kbit, 16-Kbit or 64-Kbit EEPROM, and Fast Transfer Mode capability

Datasheet - production data



Features

I²C interface

- Two-wire I²C serial interface supports 1MHz protocol
- Single supply voltage: 1.8V to 5.5V
- Multiple byte write programing (up to 256 bytes)

Contactless interface

- Based on ISO/IEC 15693 and NFC Forum Type 5 tag
- Supports all ISO/IEC 15693 modulations, coding, subcarrier modes and data rates
- Custom Fast read access up to 53 Kbit/s
- Single and multiple blocks read(1)
- Single and multiple blocks write(1) (up to 4)
- Internal tuning capacitance: 28.5 pF

Memory

- Up to 64-kbits of EEPROM (depending on version)
- I²C interface accesses bytes
- RF interface accesses blocks of 4 bytes
- Write time:
  - From I²C: typical 5ms for 1 byte
  - From RF: typical 5ms for 1 block
- Data retention: 40 years
- Write cycles endurance:
  - 1 million write cycles at 25 °C
  - 600k write cycles at 85 °C

Fast Transfer Mode

- Fast data transfer between I²C and RF interfaces
- Half-duplex 256-byte dedicated buffer

Energy harvesting

- Analog output pin to power external components

Data protection

- User memory: 1 to 4 configurable areas, protectable in read and/or write by three 64-bit passwords in RF and one 64-bit password in I²C
- System configuration: protected in write by a 64-bit password in RF and a 64-bit password in I²C

GPO

- Interruption pin configurable on multiple RF events (field change, memory write, activity, Fast Transfer end, user set/reset/pulse)
- Open Drain or CMOS output (depending on version)

Low power mode(2)

- Input pin to trigger low power mode

RF management

- RF command interpreter enabled/disabled from I²C host controller

Temperature range

- From - 40 to 85 °C

Package

- 8-pin and 12-pin packages
- ECOPACK2® (RoHS compliant)

Table 1. Device summary

Reference	Part number
ST25DVxxx	ST25DV04K ST25DV16K ST25DV64K

1. Same for Extended commands.

2. 12-pin package only.

Contents

List of tables

List of figures

1 Description

The ST25DVxxx device is a NFC RFID Tag offering 4 Kbit, 16 Kbit, and 64 Kbit of electrically erasable programmable memory (EEPROM). ST25DVxxx offers two interfaces. The first one is an I^2C serial link and can be operated from a DC power supply. The second one is a RF link activated when ST25DVxxx acts as a contactless memory powered by the received carrier electromagnetic wave.

In I^2C mode, the ST25DVxxx user memory contains up to 8192 bytes, which could be split in 4 flexible and protectable areas.

In RF mode, following ISO/IEC 15693 or NFC forum type 5 recommendations, ST25DVxxx user memory contains up to 2048 blocks of 4 bytes which could be split in 4 flexible and protectable areas.

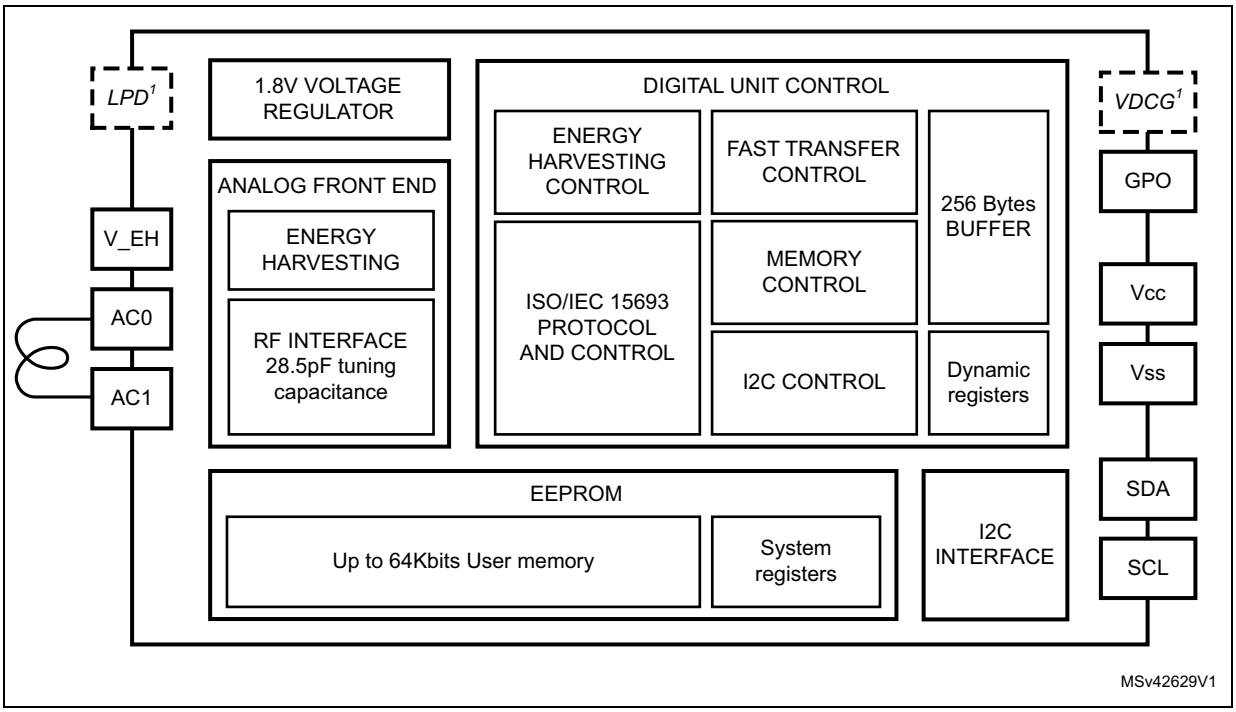
ST25DVxxx offers a fast transfer mode between the RF and contact worlds, thanks to a 256 bytes volatile buffer (also called Mailbox).

In addition, the GPO pin of the ST25DVxxx provides data informing the contact world about incoming events, like RF field detection, RF activity in progress or mailbox message availability.

An energy harvesting feature is also proposed when external conditions make it possible.

1.1 ST25DVxxx block diagram

Figure 1. ST25DVxxx block diagram



1. V_{DCG} and LPD are included in 12 pins package only

1.2 ST25DVxxx packaging

ST25DVxxx is provided in different packages:

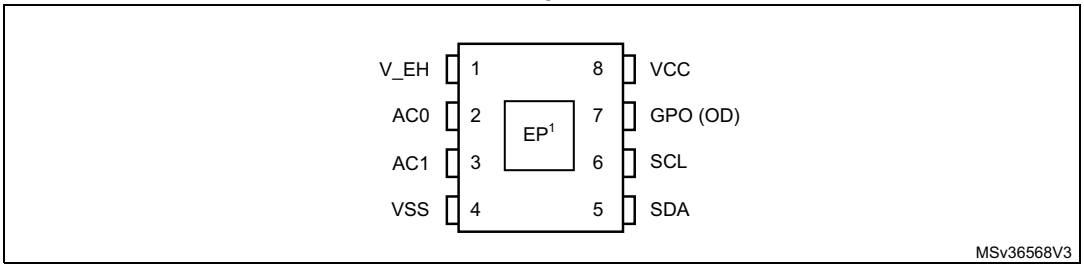
- 8 pins (S08 or TSSPOP8 or UFDFPN8) for the open drain version of Interrupt output
- 12 pins (UFDFPN12) for a CMOS interrupt output. This package includes an additional element that minimizes standby consumption.

Table 2. Signal names

Signal name	Function	Direction
V_EH	Energy Harvesting	Power output
GPO	Interrupt Output	Output
SDA	Serial Data	I/O
SCL	Serial Clock	Input
AC0, AC1	Antenna coils	
V_{CC}	Supply voltage	Power
V_{SS}	Ground	
LPD(1)	Low power down mode	Input
V_{DCG}(1)	Supply voltage for GPO driver	Power
NC	Not connected	Must be left floating
EP(2)	Exposed Pad	Must be left floating

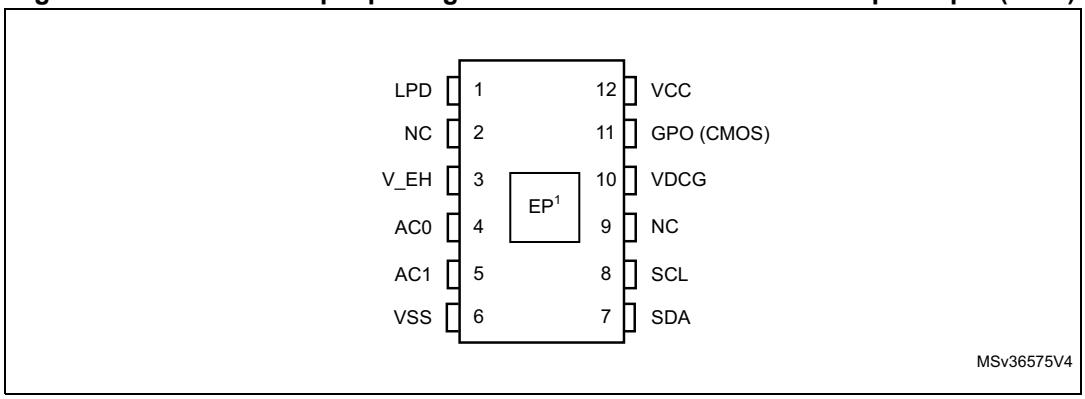
1. Available only on 12-pin package.
2. Available only on UFDPN8 and UFDFPN12 packages.

Figure 2. ST25DVxxx 8-pin packages connections with Open drain Interruption Output



1. Exposed Pad is only present on UFDFPN8 package.

Figure 3. ST25DVxxx 12-pin package connections with Cmos Interrupt Output (GPO)



1. Exposed Pad is only present on UFDFPN12 package.

2 Signal descriptions

2.1 Serial link (SCL, SDA)

2.1.1 Serial clock (SCL)

This input signal is used to strobe all data in and out of the ST25DVxxx. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. See *Section 9.2* to know how to calculate the value of this pull-up resistor

2.1.2 Serial data (SDA)

This bidirectional signal is used to transfer data in or out of the ST25DVxxx. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 75* indicates how the value of the pull-up resistor can be calculated).

2.2 Power control (V_{CC}, LPD,V_{SS})

2.2.1 Supply voltage (V_{CC})

This pin can be connected to an external DC supply voltage.

Note: An internal voltage regulator allows the external voltage applied on V_{CC} to supply the ST25DVxxx, while preventing the internal power supply (rectified RF waveforms) to output a DC voltage on the V_{CC} pin.

2.2.2 Low Power Down (LPD)

This input signal is used to control an internal 1.8 V regulator delivering ST25DVxxx internal supply. When LPD is high, this regulator is shut off and its consumption is reduced below 1µA. This regulator has a turn on time in range of 100us, to be added to the boot duration, before the device becomes fully operational. This feature is only available on the 12-pin ST25DVxxx package.

2.2.3 Ground (V_{SS})

V_{SS} is the reference for the V_{CC} and V_{DCG} supply voltages and V_EH analog output voltage.

2.3 RF link (AC0 AC1)

2.3.1 Antenna coil (AC0, AC1)

These inputs are used to connect the ST25DVxxx device to an external coil exclusively. It is advised not to connect any other DC or AC path to AC0 or AC1.

When correctly tuned, the coil is used to power and access the device using the ISO/IEC 15693 and ISO 18000-3 mode 1 protocols.

2.4 Process control (V_{DCG}, GPO)

2.4.1 Driver Supply voltage (V_{DCG})

This pin, available only with ST25DVxx-JF version, can be connected to an external DC supply voltage. It only supplies the GPO driver block. ST25DVxxx cannot be powered by V_{DCG}. If V_{DCG} is left floating, no information will be available on GPO pin.

2.4.2 General purpose output (GPO)

The ST25DVxxx features a configurable output GPO pin used to provide RF activity information to an external device. ST25DVxx-IE offers a GPO open drain. This GPO pin must be connected to an external pull-up resistor (> 4.7 KΩ) to operate.

The interrupt consists in pulling the state to a low level or outputting a low-level pulse on GPO pin.

ST25DVxx-JF offers a GPO CMOS output, which requires to connect V_{DCG} pin to an external power supply. The interrupt consists in setting the state to a high level or outputting a positive pulse on the GPO pin.

GPO pin is a configurable output signal, and can mix several Interruption modes. By default, the GPO register sets the interruption mode as a RF Field Change detector. It is able to raise various events like RF Activity, Memory Write completion, or fast transfer actions. It can authorize the RF side to directly drive GPO pin using the Manage GPO command to set the output state or emit a single pulse (for example, to wake up an application.). See *Section 5.2: GPO* for details.

2.5 Energy harvesting analog output (V_EH)

This analog output pin is used to deliver the analog voltage V_EH available when the Energy harvesting mode is enabled and if the RF field strength is sufficient. When the Energy harvesting mode is disabled or the RF field strength is not sufficient, V_EH pin is in High-Z state (See *Section 5.3: Energy Harvesting (EH)* for details).

3 Power management

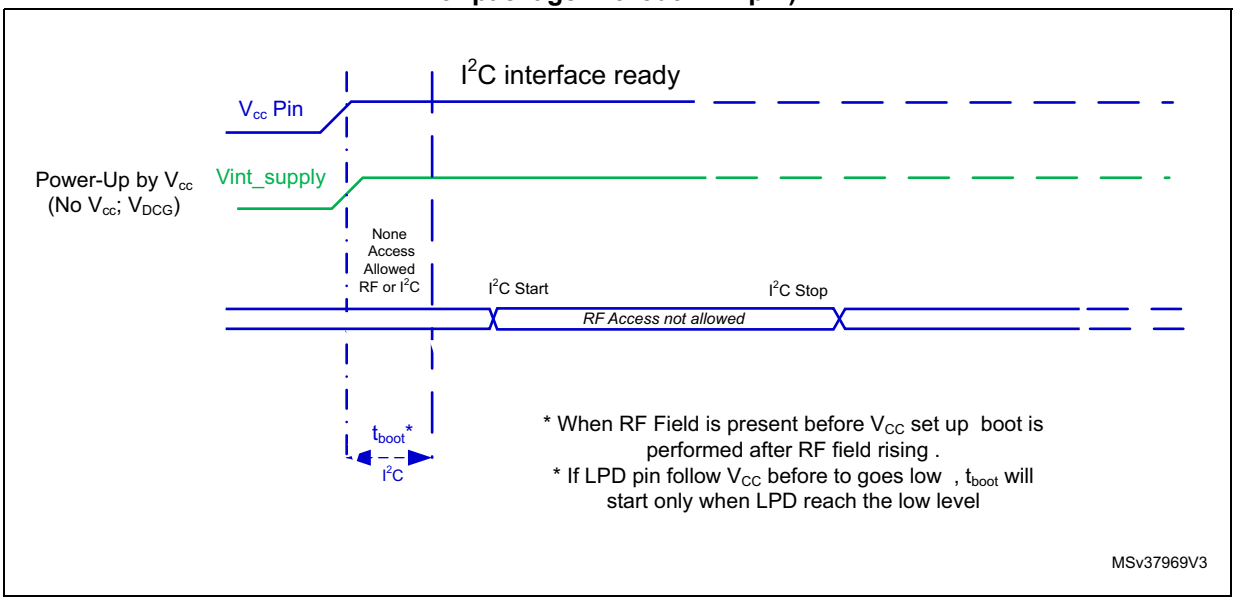
3.1 Wired interface

Operating supply voltage V_{CC}

In contact mode, prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 204: I²C operating conditions*). To maintain a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF and 100 pF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal I²C write cycle (t_W). Instructions are not taken into account until completion of ST25DVxxx's boot sequence (see *Figure 4*).

Figure 4. ST25DVxxx Power-Up sequence (No RF field, LPD pin tied to V_{ss} or package without LPD pin)



Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1V/µs.

Device reset in I²C mode

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the ST25DVxxx does not respond to any I²C instruction until V_{CC} has reached the power-on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 204: I²C operating conditions*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby power mode. However, the device must not be accessed until V_{CC} has reached a valid and stable V_{CC} voltage within the specified [$V_{CC(min)}$, $V_{CC(max)}$] range and

t_boot time necessary to ST25DVxxx set-up has passed. In the version supporting LPD pin, the boot will take place only when LPD goes low.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the device stops responding to any instruction sent to it, and I^2C address counter is reset.

Power-down mode

During power-down (continuous decay of V_{CC}), the device must be in Standby power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3.2 Contactless interface

Device set in RF mode

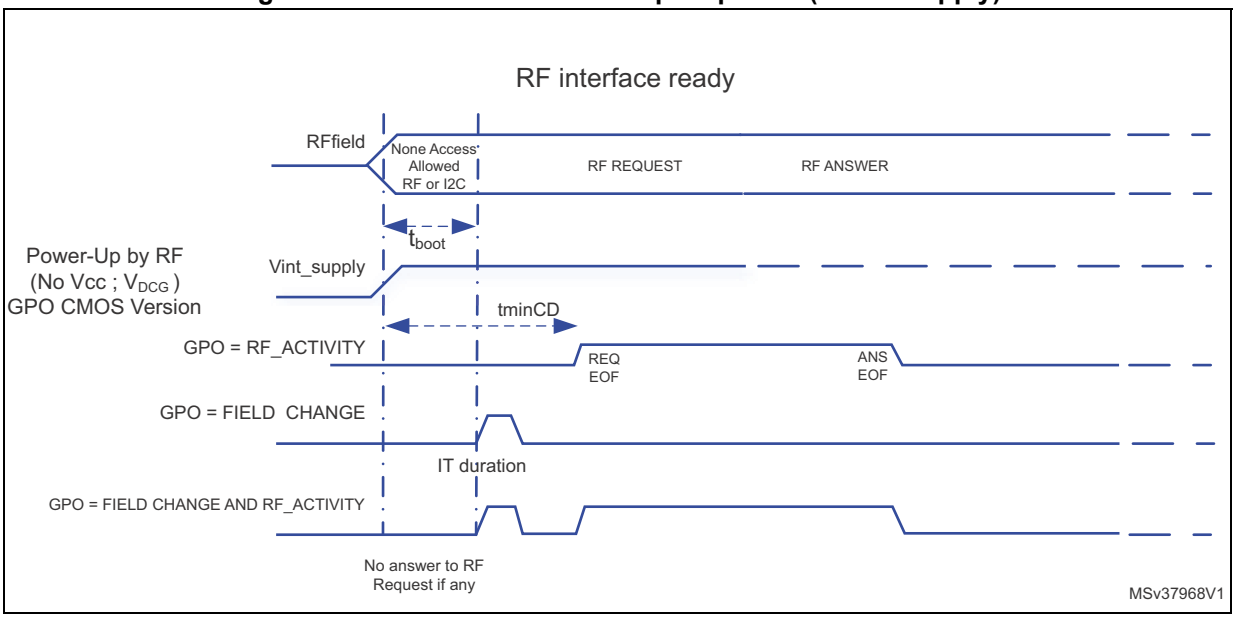
To ensure a proper boot of the RF circuitry, the RF field must be turned ON without any modulation for a minimum period of time t_{RF_ON}. Before this time, ST25DVxxx will ignore all received RF commands. (See *Figure 5: ST25DVxxx RF Power Up sequence (No DC supply)*).

Device reset in RF mode

To ensure a proper reset of the RF circuitry, the RF field must be turned off (100% modulation) for a minimum t_{RF_OFF} period of time.

The RF access can be temporarily or indefinitely disabled by setting the appropriate value in the RF disable register.

Figure 5. ST25DVxxx RF Power Up sequence (No DC supply)



4 Memory management

4.1 Memory organization overview

The ST25DVxxx memory is divided in four main memory areas:

- User memory
- Dynamic registers
- Fast Transfer Mode buffer
- System configuration area

The ST25DVxxx user memory can be divided into 4 flexible user areas. Each area can be individually read - and/or - write-protected with one out of three specific 64-bit password.

The ST25DVxxx dynamic registers are accessible by RF or I^2C host and provide dynamic activity status or allow temporary activation or deactivation of some ST25DVxxx features.

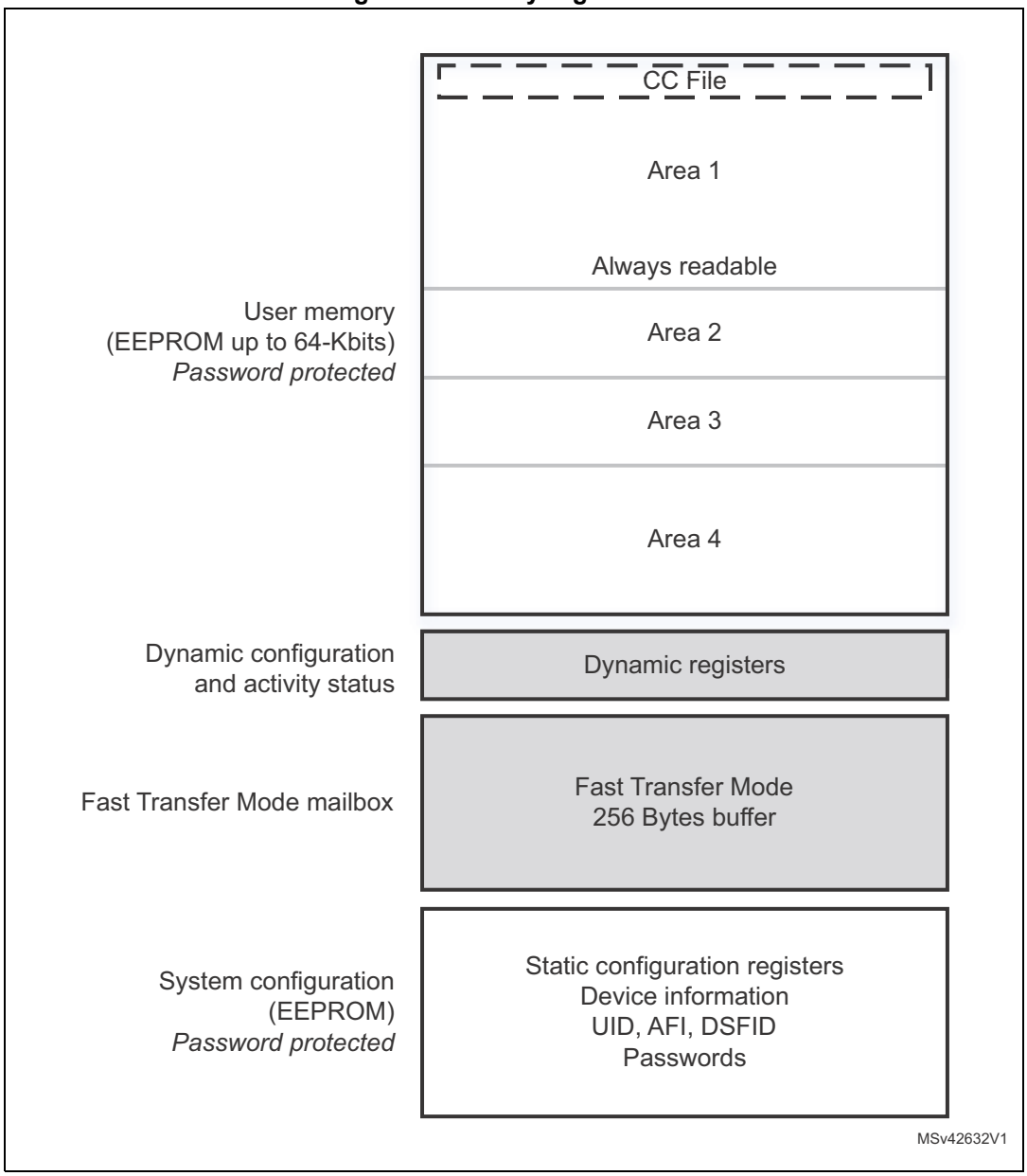
The ST25DVxxx also provides a 256 byte Fast Transfer Mode buffer, acting as a mailbox between RF and I^2C interface, allowing fast data transfer between contact and contactless worlds.

Finally, the ST25DVxxx system configuration area contains static registers to configure all ST25DVxxx features, which can be tuned by user. Its access is protected by a 64 bit configuration password.

This system configuration area also includes read only device information such as IC reference, memory size or IC revision, as well as a 64-bit block that is used to store the 64-bit unique identifier (UID), and the AFI (default 00h) and DSFID (default 00h) registers. The UID is compliant with the ISO 15693 description, and its value is used during the anticollision sequence (Inventory). The UID value is written by ST on the production line. The AFI register stores the application family identifier. The DSFID register stores the data storage family identifier used in the anticollision algorithm.

The system configuration area includes five additional 64-bit blocks that store an I^2C password plus three RF user area access passwords and a RF configuration password.

Figure 6. Memory organization



4.2 User memory

User memory is accessible from both RF contactless interface and I^2C wired interface.

From RF interface, user memory is addressed as Blocks of 4 bytes, starting at address 0. RF extended read and write commands can be used to address all ST25DVxxx memory blocks. Other read and write commands can only address up to block FFh.

From I^2C interface, user memory is addressed as Bytes, starting at address 0. Device select must set E2 = 0. User memory can be read in continuity. Unlike the RF interface, there is no roll-over when the requested address reaches the end of the memory capacity.