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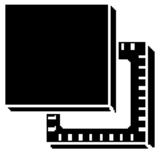
ST25R3910

Mid-range HF reader with 0.7 W supporting AAT

Datasheet - production data



QFN32

Features

- Close loop adjustment of ASK modulation for accurate control of modulation depth in case of ISO-14443B protocol
- Low power (3.5 µA) NFC target mode
- AM/PM demodulator
- Accurate RF envelope measurement (8-bit A/D converter)
- High output power at 3.3 V power supply:
  - Up to 700 mW in case regulator is externally shorted
  - Up to 500 mW in case of differential output when antenna trimming is used
  - Up to 125 mW in case of single ended output when antenna trimming is used
- Squelch for gain reduction, to compensate for noise generated by tag processing
- Automatic Antenna tuning (AAT)
- Transparent mode
- Amplitude and phase measurement
- Supporting 13.56 MHz and 27.12 MHz quartz oscillator with fast start-up
- Supply voltage range from 2.4 to 3.6 V
- Wide temperature range: -40 ºC to 85 ºC
- Package: 32-pin QFN (5x5mm)

Description

The ST25R3910 is a high performance 13.56 MHz RFID reader, with two differential, low impedance (1.5 Ohm) antenna drivers.

These drivers are unmatched, allowing the ST25R3910 to deliver up to eight times the output power of a standard HF reader IC using the same power supply voltage, and reducing in half the power consumption at the same output power.

The ST25R3910 can operate already at 2.4 V, with a low power operating mode of 5 mA, making it perfectly suited for portable or battery-powered applications.

For applications where high power is required the ST25R3910 can deliver up to 700 mW, thus avoiding the need for complex external booster circuitry.

The component count and complexity of the design is further reduced through automatic modulation depth adjustment.

The analog front end (AFE) is complemented by a highly integrated data framing engine for both ISO-14443 A and B. This includes data rates up to 848 kbit/s, with all framing and synchronization tasks on board. This enables to build a complete HF RFID reader using only a low end MCU.

The ST25R3910 supports reader to tag and Peer to Peer communication using the NFCIP-1 active communication mode with a 106 kbps data rate. Other standard and custom protocols, such as ISO-15693 or FeliCa™ can be implemented via transparent mode. The ST25R3910 features a SPI, which enables bi-directional communication with the external microcontroller.

The ST25R3910 also features the Automatic Antenna Tuning (AAT) technology, enabling the reader to re tune itself to deliver maximum output at 13.56 MHz, when the surroundings detune the antenna.

Contents

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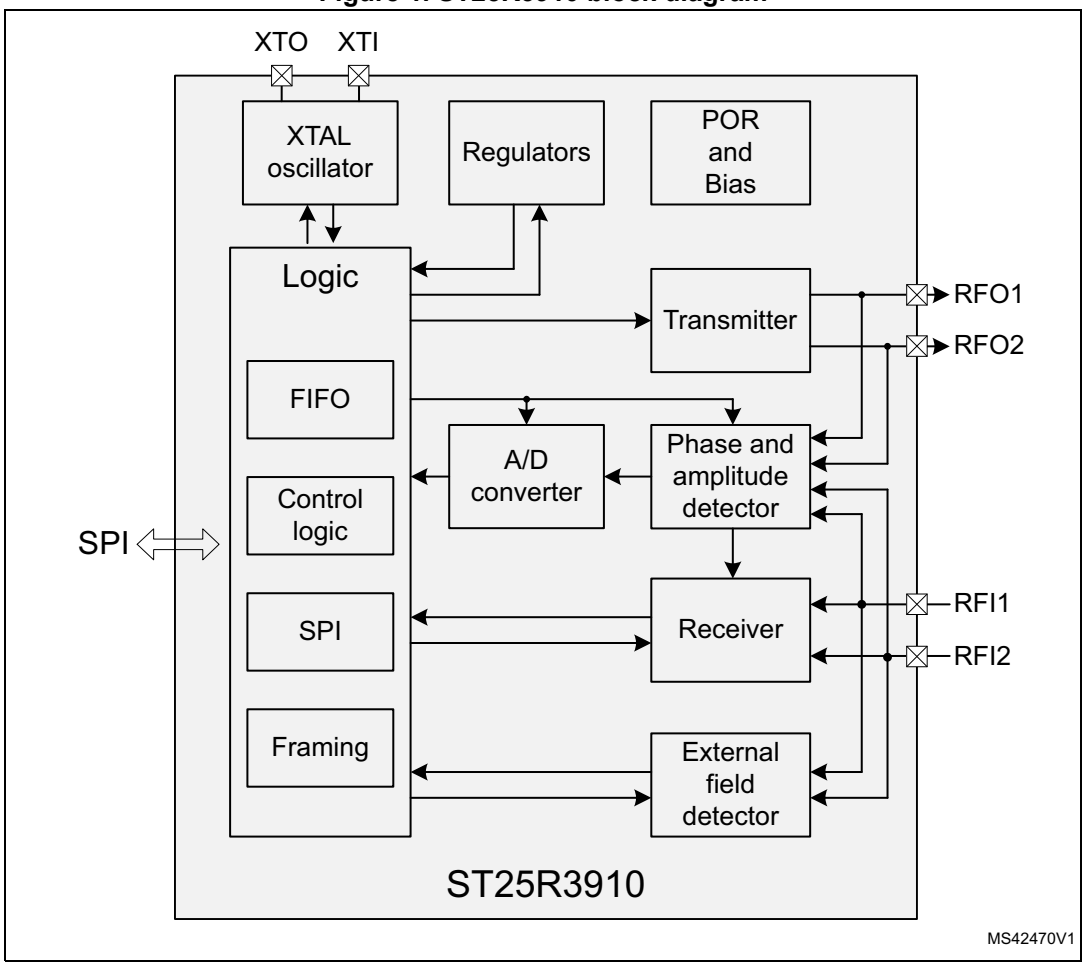
1 Functional overview

The ST25R3910 is suitable for applications where the reader antenna is directly driven (no 50 Ω cable). Several unique features make it especially suitable for low power and battery powered applications.

1.1 Block diagram

The block diagram is shown in *Figure 1*.

Figure 1. ST25R3910 block diagram



1.1.1 Transmitter

The transmitter incorporates drivers that drive external antenna through pins RFO1 and RFO2. Single sided and differential driving is possible. The transmitter block additionally contains a sub-block that modulates transmitted signal (OOK or configurable AM modulation).

The ST25R3910 transmitter is intended to directly drive antennas (without 50 Ω cable, usually antenna is on the same PCB). Operation with 50 Ω cable is also possible, but in that case some of the advanced features are not available.

1.1.2 Receiver

The receiver detects tag modulation superimposed on the 13.56 MHz carrier signal. The receiver contains two receive chains (one for AM and another for PM demodulation) composed of a peak detector followed by two gain and filtering stages and a final digitizer stage. The filter characteristics are adjusted to optimize performance for each mode and bit rate (sub-carrier frequencies from 212 kHz to 848 kHz are supported). The receiver chain inputs are the RFI1 and RFI2 pins. The receiver chain incorporates several features that enable reliable operation in challenging phase and noise conditions.

1.1.3 Phase and amplitude detector

The phase detector is observing the phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals (RFI1 and RFI2). The amplitude detector is observing the amplitude of the receiver input signals (RFI1 and RFI2) via self-mixing. The amplitude of the receiver input signals (RFI1 and RFI2) is directly proportional to the amplitude of the antenna LC tank signal.

The phase detector and the amplitude detector can be used for the following purposes:

- PM demodulation, by observing RFI1 and RFI2 phase variation
- Average phase difference between RFOx pins and RFIx pins is used to check and optimize antenna tuning and inductive wakeup via the MCU
- Amplitude of signal present on RFI1 and RFI2 pins is used to check and optimize antenna tuning

1.1.4 A/D converter

The ST25R3910 contains a built in Analog to Digital (A/D) converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude and phase, calibration of modulation depth…). The result of the A/D conversion is stored in a register and can be read via SPI.

1.1.5 External field detector

The External field detector is a low power block switched on in NFCIP target mode to detect the presence of the initiator field, and also used during the NFCIP Collision Avoidance procedure.

1.1.6 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve a fast start-up. The start-up time varies with crystal type, temperature and other parameters, hence the oscillator amplitude is observed and an interrupt is sent when stable oscillator operation is reached.

The oscillator block also provides a clock signal to the external microcontroller (MCU_CLK), according to the settings in the control register.

1.1.7 Power supply regulators

Integrated power supply regulators ensure a high power supply rejection ratio for the complete reader system. If the reader system PSRR has to be improved, the command Adjust Regulators is sent. As a result of this command, the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to assure a stable regulated supply. The resulting regulated voltage is stored in a register. It is also possible to define regulated voltage by writing a configuration register. To decouple any noise sources from different parts of the IC there are three regulators integrated with separated external blocking capacitors (the regulated voltage of all of them is the same). One regulator is for the analog blocks,the other is for the antenna drivers. Logic and digital I/O pads are supplied directly from V_{DD} (negative supply pin for logic and digital I/O is separated to avoid coupling of logic induced noise in the substrate).

This block additionally generates a reference voltage for the analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

1.1.8 POR and Bias

This block provides the bias current and the reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit that provides a reset at power-up and at low supply voltage levels.

1.1.9 ISO-14443 and NFCIP-1 framing

This block performs framing for receive and transmit according to the selected ISO mode and bit rate settings.

In reception it takes the demodulated sub-carrier signal from the receiver. It recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from the FIFO, generates parity and CRC bits, adds SOF and EOF and performs final encoding before passing the modulation signal to the transmitter.

In Transparent mode, the framing and FIFO are bypassed, the digitized sub-carrier signal (the receiver output), is directly sent to the SDATAO pin, and the signal applied to the SDATAI pin is directly used to modulate the transmitter.

1.1.10 FIFO

The ST25R3910 contains a 32-byte FIFO. Depending on the mode, it contains either data that has been received or data to be transmitted.

1.1.11 Control logic

The control logic contains I/O registers that define operation of device.

1.1.12 SPI

A 4-wire Serial Peripheral Interface (SPI) is used for communication between the external microcontroller and the ST25R3910.

1.2 Application information

The minimum configurations required to operate the ST25R3910 are shown in *Figure 2* and *Figure 3*.

Figure 2. Minimum configuration with single sided antenna driving (including EMC filter)

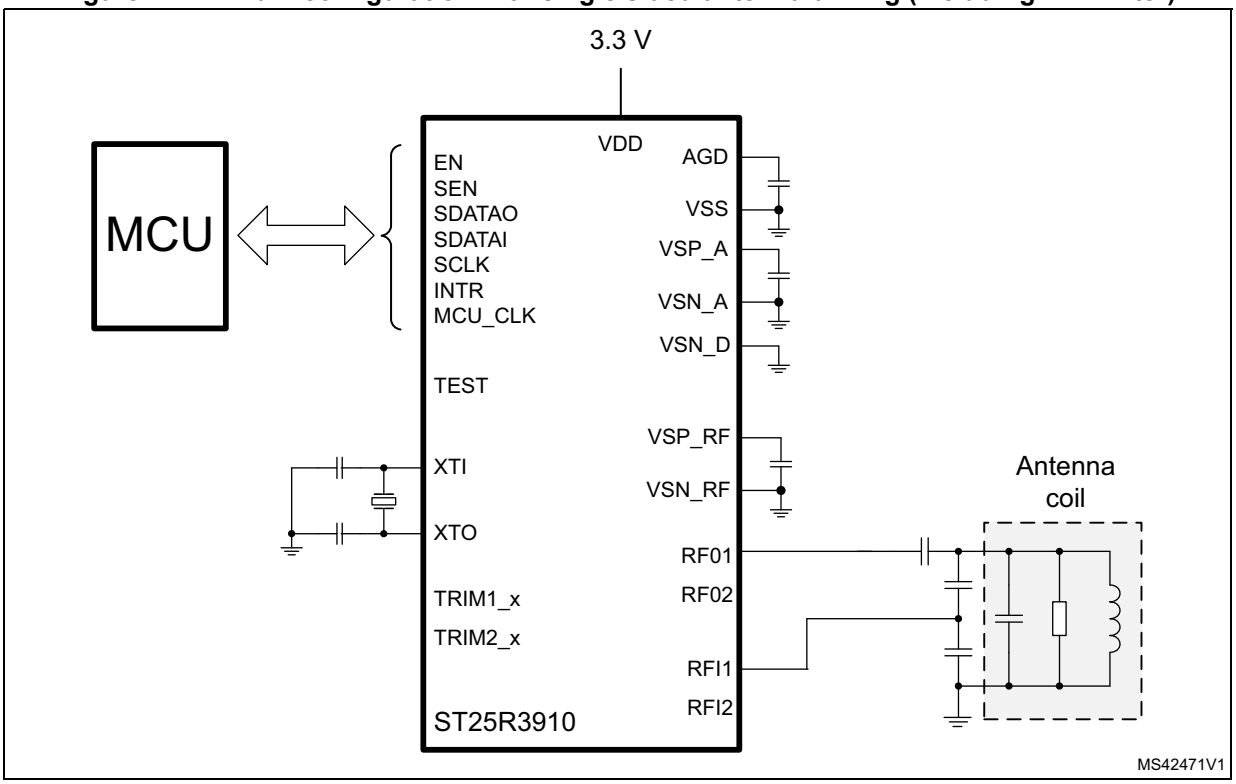
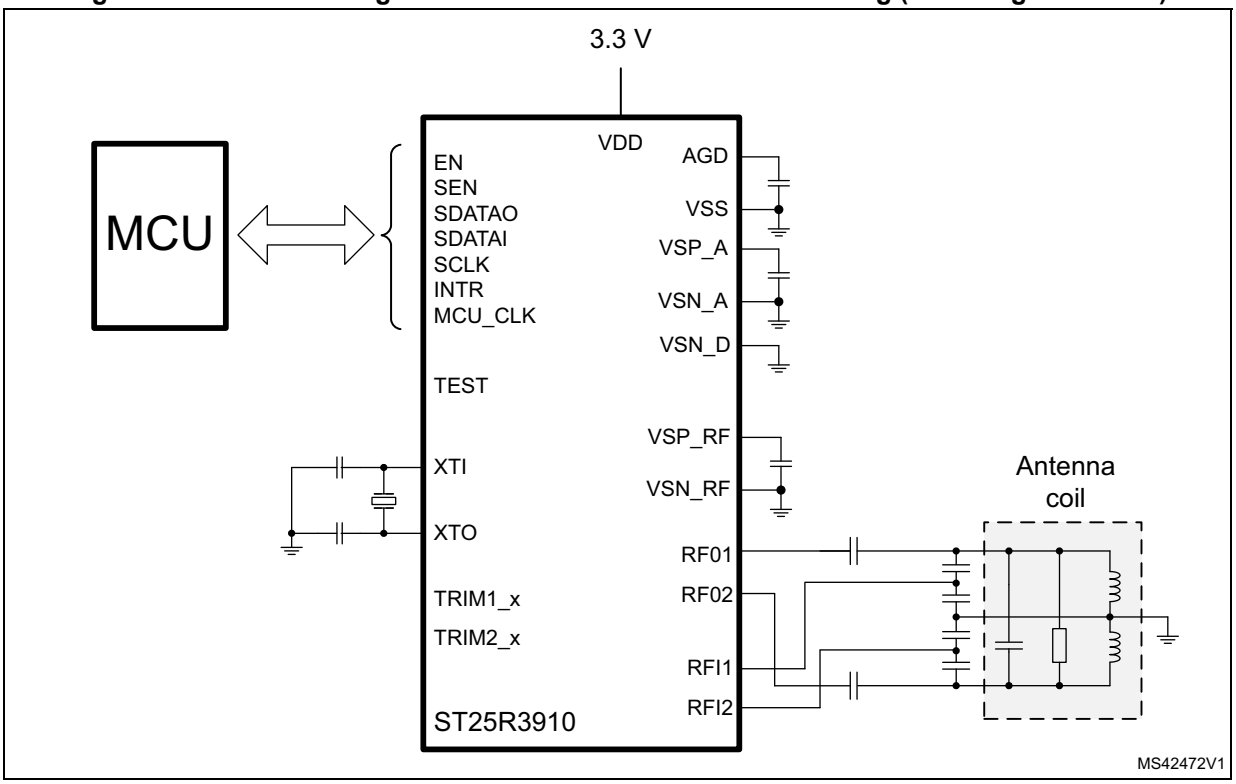


Figure 3. Minimum configuration with differential antenna driving (including EMC filter)



1.2.1 Operating modes

The ST25R3910 operating mode is defined by the contents of the *Operation Control Register*.

At power-up all bits of the *Operation Control Register* are set to 0, the ST25R3910 is in Power-down mode. In this mode AFE static power consumption is minimized, only the POR and part of the bias are active, while the regulators are transparent and are not operating. The SPI is still functional in this mode so all settings of ISO mode definition and configuration registers can be done.

Control bit en (bit 7 of the *Operation Control Register*) is controlling the quartz crystal oscillator and regulators. When this bit is set, the device enters in Ready mode. In this mode the quartz crystal oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable.

Enable of receiver and transmitter are separated so it is possible to operate one without switching on the other (control bits rx_en and tx_en). In some cases this may be useful, if the reader field has to be maintained and there is no tag response expected, the receiver can be switched-off to save current. Another example is the NFCIP-1 active communication receive mode in which the RF field is generated by the initiator and only the receiver operates.

The receiver also has a Low power mode in which its power consumption (and then its sensitivity) is reduced. This mode is entered in by setting control bit rx_lp.

The last control bit of the *Operation Control Register* is nfc_t bit. Setting of this bit is only allowed in case the NFC mode is set in the ISO mode definition register. Setting this bit to one, while all other bits are set to 0, puts the ST25R3910 into Initial NFC Target mode. In

this low power mode, only the Target Activation Detector, which will detect a presence of external RF field, is active. Once the presence of external RF field is detected, an interrupt is sent to the microcontroller, which will in turn switch on the oscillator and the receiver.

1.2.2 Transmitter

The transmitter contains two identical push-pull driver blocks connected to the pins RFO1 and RFO2. Each driver is composed of eight segments having binary weighted output resistance. The MSB segment typical ON resistance is 3 Ω, when all segments are turned on; the output resistance is typically 1.5 Ω. All segments are turned on to define the normal transmission (non-modulated) level. It is also possible to switch off certain segments when driving the non-modulated level to reduce the amplitude of the signal on the antenna and/or to reduce the antenna Q factor without making any hardware changes.

AM modulation and operation of the driver segments is controlled by writing AM modulation depth and antenna driver registers. *Antenna Driver Non-Modulated Level Definition Register* defines which segments will be used to define normal, non-modulated level. *Modulation Depth Definition Register* and *Antenna Driver AM Modulated Level Definition Register* are used to define how the AM modulated level is set-up. It can be set-up automatically by definition of modulation depth and the direct command Calibrate Modulation Depth or by a direct definition of segments which are turned off during AM modulation.

1.2.3 Receiver

The receiver performs demodulation of the tag sub-carrier modulation that is superimposed on the 13.56 MHz carrier frequency. It performs AM and/or PM demodulation, amplification, band-pass filtering and digitalization of sub-carrier signals (848, 424 and 212 kHz subcarrier frequencies are supported). Additionally it performs RSSI measurement, automatic gain control (AGC) and Squelch.

The receiver is switched on when *Operation Control Register* bit rx_en is set. The operation of the receiver is additionally controlled by the signal rx_on, set high when modulated signal is expected on the receiver input. This is automatically done after every Transmit command. Signal rx_on can be also forced high by sending direct command Unmask Receive Data. Signal rx_on is used to control features like RSSI and AGC.

AM demodulation is performed using a peak follower. Both the positive and negative peaks are tracked to suppress common mode signal. In case external demodulation is carried out the peak follower stage can be bypassed by setting bit envi in *Configuration Register 2*. In case of PM demodulation signal coming from the phase detector is replacing the output of peak follower.

Next stage in signal processing is the buffer amplifier followed by second order low pass filter with adjustable corner frequency. Final stage is a first order high pass filter with adjustable corner frequency. The digital signal representing tag subcarrier modulation is produced by a window comparator.

Filter setting is done automatically when ISO mode and data rate are chosen by writing *ISO Mode Definition Register*. Setting is displayed in the *Receiver Configuration Register* and can be changed by rewriting this register. In Transparent mode the *ISO Mode Definition Register* is not used and Filter selection has to be done by writing *Receiver Configuration Register*. By setting the *Operation Control Register* bit rx_lp receiver operates in Low power mode. In this mode, power consumption is lower but receiver sensitivity is reduced (see *Section 3: Electrical characteristics on page 58*).

Gain reduction, AGC and Squelch

The total gain of receiver chain is 160. In certain conditions it is desirable to reduce this gain. There are several features implemented in the Receiver to reduce this gain.

Automatic Gain Reduction (AGC)

The automatic gain control feature is useful in case the tag is close to the reader. In such conditions the receiver chain is in saturation and demodulation can be influenced by system noise and saturation of last gain stage. When AGC is switched on receiver gain is reduced so that the input to digitizer stage is not saturated. The AGC system comprises a window comparator with a window three times larger than the one of the digitalization window comparator. When the AGC function is enabled the gain is reduced until there are no transitions on its output. Such procedure ensures that the input to digitalization window comparator is less than three times larger than its window.

AGC operation is controlled by the *Receiver Configuration Register* bits agc_en and agc_m. Agc_en bit enables AGC operation, agc_m defines AGC operating mode. The AGC action is started 20 µs after the rising edge of signal rx_on. In case agc_m bit is 0 it will operate during a complete receive period, in case it is 1 it will operate on the first 8 subcarrier pulses. The AGC is reducing gain by 21 dB in 7 steps of 3 dB. When signal rx_on is low AGC is in reset.

Squelch

This feature is designed for operation of the receiver in noisy conditions. The noise can come from tags (caused by the processing of reader commands), or it can come from a noisy environment. This noise may be misinterpreted as start of tag response, resulting in decoding errors.

During execution of the Squelch procedure the output of the digitizing comparator is observed. In case there are more than two transitions on this output in a 50 µs time period, the receiver gain is reduced by 3 dB, and the output is observed during the next 50 µs. This procedure is repeated until the number of transitions in 50 µs is lower or equal to two, or until the maximum gain reduction is reached. This gain reduction can be cleared sending the direct command Clear Squelch.

During execution of the direct command Squelch the digital output of receiver (output of window comparator mentioned above) is observed. In case there are more than two transitions on this output in 50 µs time period, the gain is reduced by 3 dB and output is observed during next 50 µs. This procedure is repeated until the number of transitions in 50 µs is lower or equal to two, or until the maximum gain reduction (21 dB) is reached. This setting is cleared with direct command Clear Squelch.

Setting gain reduction

By setting bits rg2 to rg0 in *Receiver Configuration Register* receiver gain can also be reduced in seven steps of 3 dB.

Actual gain reduction is combination of all three gain reduction features mentioned above (AGC, Squelch and setting gain reduction in *Receiver Configuration Register*). Actual gain reduction state can also be observed by reading the *Receiver State Display Register* bits gr_2 to gr_0.

RSSI

The receiver also performs the RSSI (Received Signal Strength Indicator) measurement of the modulated signal that is superimposed on the 13.56 MHz carrier. The RSSI measurement is started after the rising edge of rx_on. It stays active as long as signal rx_on is high, it is frozen while rx_on is low. The RSSI is a peak hold system, and the value can only increase from the initial zero value. Every time the AGC reduces the gain the RSSI measurement is reset and starts from zero. Result of RSSI measurements is a 4-bit value that can be observed by reading the *Receiver State Display Register*. The LSB step is 2.15 dB.

Since the RSSI measurement is of peak hold type the RSSI measurement result does not follow any variations in the signal strength (the highest value will be kept). In order to follow RSSI variations it is possible to reset the RSSI bits and restart the measurement by sending the direct command Clear RSSI.

1.2.4 A/D converter

The ST25R3910 contains an 8-bit successive approximation A/D converter. Inputs to the A/D converter can be multiplexed from different sources to be used in several direct commands and adjustment procedures. The result of the last A/D conversion is stored in the *A/D Output Register*.

The A/D converter has two operating modes, absolute and relative.

- In absolute mode the low reference is 0 V and the high reference is 2 V. This means that A/D converter input range is from 0 to 2 V, 00h code means input is 0 V or lower, FFh means that input is 2 V - 1 LSB or higher (LSB is 7.8125 mV).
- In relative mode low reference is 1/6 of V_{SP_A} and high reference is 5/6 of V_{SP_A}, so the input range is from 1/6 to 5/6 V_{SP_A}.

Relative mode is only used in phase measurement (phase detector output is proportional to power supply). In all other cases absolute mode is used.

The A/D converter input can also be accessed externally. When the direct command AD Convert is sent, an A/D conversion of voltage present on pin AD_IN is performed in absolute mode, result is stored in *A/D Output Register*. AD_IN pin should be left non-connected in case A/D conversion is not needed in application.

1.2.5 Phase and amplitude detector

Phase detector

The phase detector is observing phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals RFI1 and RFI2, which are proportional to the signal on the antenna LC tank. These signals are first elaborated by digitizing comparators, then digitized signals are processed by a phase detector. Filter characteristics of the phase antenna are adapted to one of the two possible operation modes. For antenna tuning check, a strong low power filter is used to get average phase difference, for PM demodulation a low pass filter having 1 MHz corner frequency is used to pass the subcarrier frequency.

The phase detector output is inversely proportional to the phase difference between the two inputs. The 90° phase shift (ideal antenna LC tank tuning) results in $V_{SP}/2$ output voltage.

If the antenna LC tank is detuned, phase shift changes, resulting in a different phase detector output voltage. In case of command Check Antenna Resonance phase detector output is applied to A/ D converter in relative mode. Output of phase detector is also observed by comparator with reference signal $V_{SP}/2$. Output of this comparator is used in execution of direct command Calibrate Antenna.

The phase detector has low pass characteristics in case of PM demodulation. This is to enable phase demodulation of the 848 kHz subcarrier signal. The output is then fed to the Receiver.

Amplitude detector

Signals from pins RFI1 and RFI2 are used as inputs to the self-mixing stage. The output of this stage is a DC voltage proportional to amplitude of signal on pins RFI1 and RFI2. This signal is fed to the A/D converter when amplitude of signal on RFI inputs has to be measured (direct commands Measure RF and Calibrate Modulation Depth).

1.2.6 External field detector

The External Field Detector is used in NFC mode to detect the presence of an RF field. It is composed of two sub-blocks, Target Activation Detector and a RF Collision Avoidance Detector. Input to both blocks is the signal from the RFI1 pad. The thresholds of the two blocks can be independently set by writing the *NFCIP Field Detection Threshold Register*. The outputs of both detectors are fed to a logic OR gate, whose output is fed to the Control logic. A low to high transition of this logic or gate output triggers an interrupt (Interrupt due to NFC event).

Target Activation Detector

This block is turned on in NFC target mode to detect the presence of an interrogator field. It is enabled by setting the *Operation Control Register* bit nfc_t. It is a low power block with an adjustable threshold in the range from 145mVpp and 590mVpp. This block generates an interrupt when an external field is detected and also when it disappears. With such implementation it can also be used to detect the moment when the external field disappears. This is useful to detect the moment when external NFC device (it can either an interrogator or a target) has stopped emitting an RF field since a response can only be sent afterwards. Actual state of the Target Activation Detector can be checked by reading the bit rfp in the *Receiver State Display Register*. When this bit is set to logic one, there is a signal higher than the threshold present on the input of Target Activation Detector.

RF Collision Avoidance Detector

This block is activated during the RF Collision Avoidance sequence which is executed before every request or response in NFC active communication (Initial or Response RF Collision Avoidance). In case during the RF Collision Avoidance sequence the presence of an external field is detected, request/response is not sent, an interrupt is generated to inform the external controller about collision. During RF Collision Avoidance, the Target Activation Detector is disabled in order to have the correct threshold when detection is made. The threshold of the RF Collision Avoidance Detector can be adjusted in the range from 50 to 1080 mVpp.

1.2.7 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 and 27.12 MHz crystals. The oscillator is based on an inverter stage supplied by controlled current source. A feedback loop is controlling the bias current in order to regulate amplitude on XTI pin to 1 V_{pp}. This feedback ensures reliable operation even in case of low quality crystals, with R_s up to 50 Ω. To enable a fast reader start-up an interrupt is sent when the oscillator amplitude exceeds 750 mV_{pp}. The oscillator block always provides 13.56 MHz clock signal to the rest of the IC. In case of 27.12 MHz crystal clock signal is internally divided by two. Divider is controlled by *Configuration Register 2* bit osc. Division by two ensures that the 13.56 MHz signal has a duty cycle of 50%, which is better for the Transmitter performance (no PW distortion). Use of 27.12 MHz crystal is therefore recommended.

In case of 13.56 MHz crystal, the bias current of stage which is digitizing oscillator signal is increased to minimize the PW distortion. The oscillator output is also used to drive a clock signal output pin, which can be used by the external microcontroller (MCU_CLK). By setting *Configuration Register 2* the frequency can be chosen between 13.56, 6.78 and 3.39 MHz. Any microcontroller processing generates noise, which may be captured by the ST25R3910 receiver. Using MCU_CLK as the microcontroller clock source generates noise synchronous with the reader carrier frequency that is filtered out by the receiver, while using some other incoherent clock source produces noise which may generate some sideband signals captured by Receiver. It is then recommended to use MCU_CLK as microcontroller clock source.

1.2.8 Power supply, Regulators

The ST25R3910 includes two regulators that can be adjusted automatically to improve the reader PSRR. VDD is an external power supply pin, used to supply the logic and digital pins. One regulator is used to supply analog blocks (V_{SP_A}), another is reserved for the transmitter (V_{SP_RF}) in order to decouple transmitter current spikes from the rest of the IC. All negative power supply pins are externally connected to the same negative supply, the reason for separation is the need to decouple noise induced by voltage drops on the internal power supply lines. These pins are VSS (die substrate potential), VSN_D (negative supply of logic and digital pads), VSN_A (negative supply of analog blocks) and VSN_RF (negative supply of transmitter).

An additional regulator block provides AGD voltage (1.5 V), which is used as reference potential for analog processing (analog ground). Blocking capacitors have to be connected externally to regulator outputs and AGD pins. For pins VSP_A and VSP_RF recommended blocking capacitors are 2.2 µF in parallel with 10 nF, for pin AGD 1 µF in parallel with 10 nF is suggested.

The regulated voltage ranges from 2.4 to 3.4 V, with 100 mV step. Both regulators are set to the same voltage. V_{SP_A} regulator maximum capability is 20 mA while maximum capability of V_{SP_RF} regulator is 300 mA. V_{SP_RF} regulator also has a built-in protection limiting current to 300 mA in normal operation and to 500 mA in case of a short. The regulators are operating when either the *Operation Control Register* bit en is set or pin EN is high.

In Power-down mode the regulators are not operating, V_{SP_A} and V_{SP_RF} are connected to V_{DD} through 1 kΩ resistors, to ensure smooth power-up of the system and a smooth transitions from Stand-by mode to other operating modes. In case regulators were regulating or were transparent at power-up a large current would be pulled from V_{DD} supply to charge blocking capacitors of regulated outputs, a problematic situation for battery powered systems.

At power-up the regulated voltage is set to its maximum, i.e. 3.4 V.

The regulator voltage can then be set automatically or “manually”. The automatic procedure is started by sending the direct command Adjust Regulators. In this procedure regulated voltage is set 250 mV below V_{DD}. This procedure ensures that reader operates with maximum possible power while still achieving a good PSRR.

Regulator operation can be controlled and observed by writing and reading two Regulator registers. *Regulator Display Register* is a read only register that displays actual regulated voltage when regulator is operating. In Power-down mode its content is forced to 00.

By writing *Regulated Voltage Definition Register* the user chooses between automatic and “manual” adjustment of regulated voltage. Automatic mode is chosen when bit reg_s is 0 (default and also recommended state). When bit reg_s is asserted to 1 regulated voltage is defined by bits rege_3 to rege_0 of the same register.

1.2.9 Communication with an external microcontroller

The ST25R3910 is a slave devices and the external microcontroller initiates all communication. Communication is performed by a 4-wire Serial Peripheral Interface (SPI). The ST25R3910 sends an interrupt request (pin INTR) to the microcontroller, which can use clock signal available on pin MCU_CLK when the oscillator is running. The microcontroller can also drive pin EN. Putting this pin high has the same function as setting the *Operation Control Register* bit en (entry in Ready mode).

Serial Peripheral Interface (SPI)

While signal SEN is low the SPI interface is in reset, while it is high the SPI is enabled. It is recommended to keep SEN low whenever the SPI is not in use. SDATAI is sampled at the falling edge of SCLK. All communication is done in blocks of 8 bits (bytes). First two bits of first byte transmitted after low to high transition of SEN define SPI operation mode.

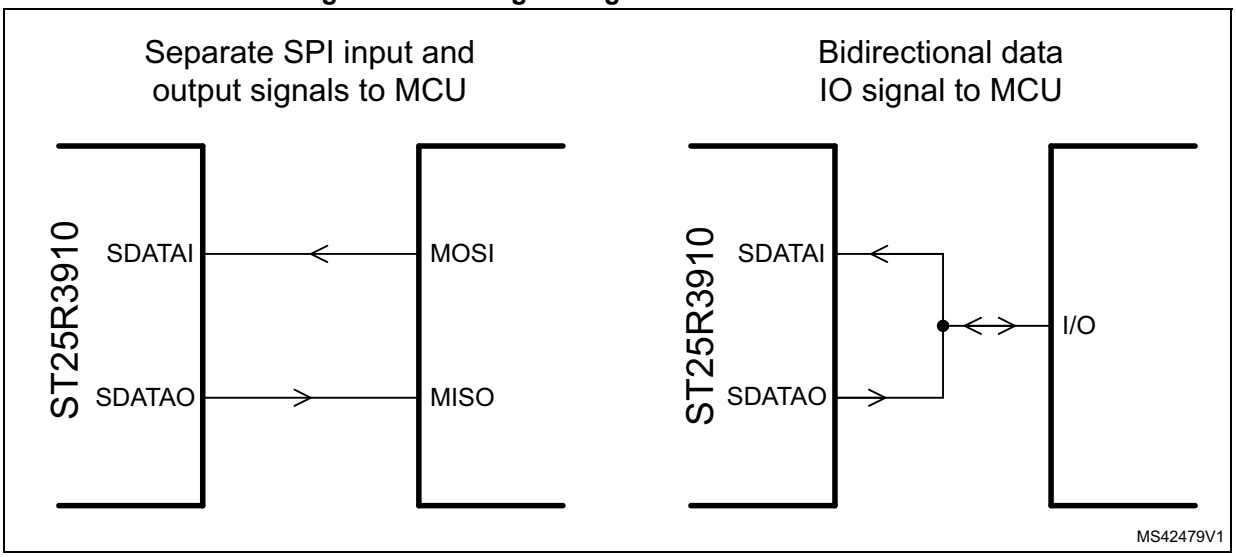
Table 1. Serial data interface (4-wire interface) signal lines

Name	Signal	Signal level	Description
SEN	Digital input	CMOS	SPI Enable (active low)
SDATAI	Digital input		Serial data input
SDATAO	Digital output with tristate		Serial data output
SCLK	Digital input		Clock for serial communication

MSB bit is always transmitted first (valid for address and data).

Read and Write modes support address auto-incrementing. This means that if some additional data bytes are sent/read after the address and first data byte, they are written to/read from addresses incremented by ‘1’. *Figure 4* defines possible modes.

Figure 4. Exchange of signals with microcontroller



When signal SEN is low, the SPI interface is in reset and SDATAO is in tristate; when it is high, SPI interface is enabled. It is recommended to keep signal SEN low whenever the SPI interface is not in use. SDATAI is sampled at the falling edge of SCLK. All communication is done in blocks of 8 bits (bytes). The first two bits of the first byte transmitted after low to high transition of SEN define the SPI operation mode. *Table 2* defines the possible modes.

Table 2. SPI operation patterns

Mode	Mode pattern (communication bits)								Mode related data							
	Mode		Register address						Register data							
	M1	M0	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Write	0	0	A5	A4	A3	A2	A1	A0	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
Read	0	1	A5	A4	A3	A2	A1	A0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
FIFO load	1	0	0	0	0	0	0	0	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
FIFO read	1	0	1	1	1	1	1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Command	1	1	C5	C4	C3	C2	C1	C0	-	-	-	-	-	-	-	-

Writing data to addressable registers (Write mode)

Figure 5 and *Figure 6* show cases of writing a single byte and writing multiple bytes with auto-incrementing address. SDATAI is sampled at the falling edge of SCLK. A SEN low pulse indicates the end of the Write command after register has been written. Auto incrementing address is supported, this means that if after the address and first data byte some additional data bytes are sent, they are written to addresses incremented by 1. If the command is terminated by putting SEN low before a packet of 8 bits composing one byte is sent, writing of this register is not performed. In case the register on the defined address does not exist or it is a read only register, no write is performed.

Figure 5. SPI communication: writing a single byte

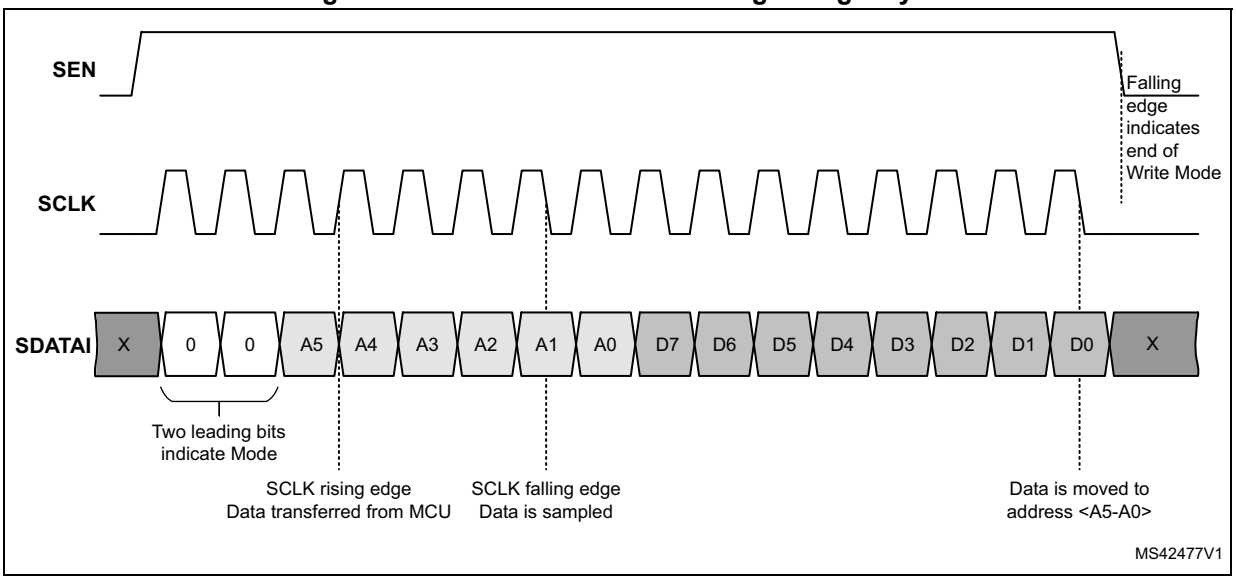
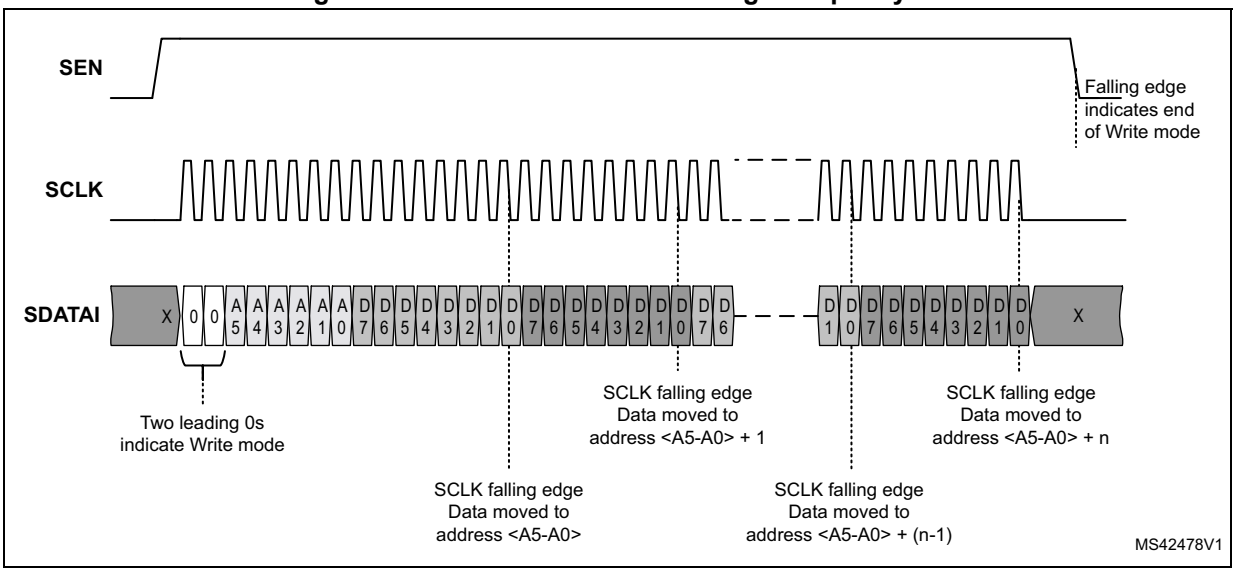


Figure 6. SPI communication: writing multiple bytes



Reading data from addressable registers (Read mode)

The command control byte for a read command consists of a command code and an address. After the command code, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from the MSB to the LSB. As in case of write, the read command supports auto-incrementing address. To transfer bytes from consecutive addresses, SPI master has to keep the SEN signal high and the SCLK has to be active as long as data need to be read from the slave.

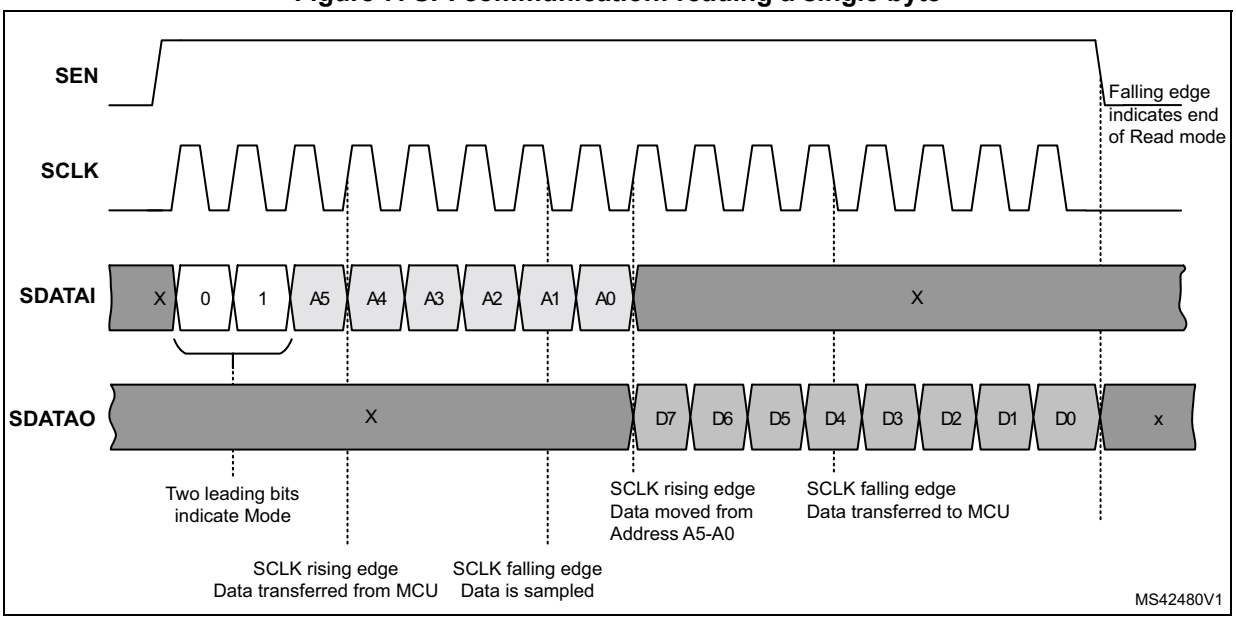
SDATAI is sampled at the falling edge of SCLK, data to be read from the ST25R3910 internal register is driven to SDATAO pin on rising edge of SCLK and is sampled by the MCU at the falling edge of SCLK.

A SEN low pulse has to be sent after register data has been transferred in order to indicate the end of the Read command and to prepare the Interface to the next command control byte.

In case the register on defined address does not exist all 0 data is sent to SDATAO.

Figure 7 is an example for reading of single byte.

Figure 7. SPI communication: reading a single byte

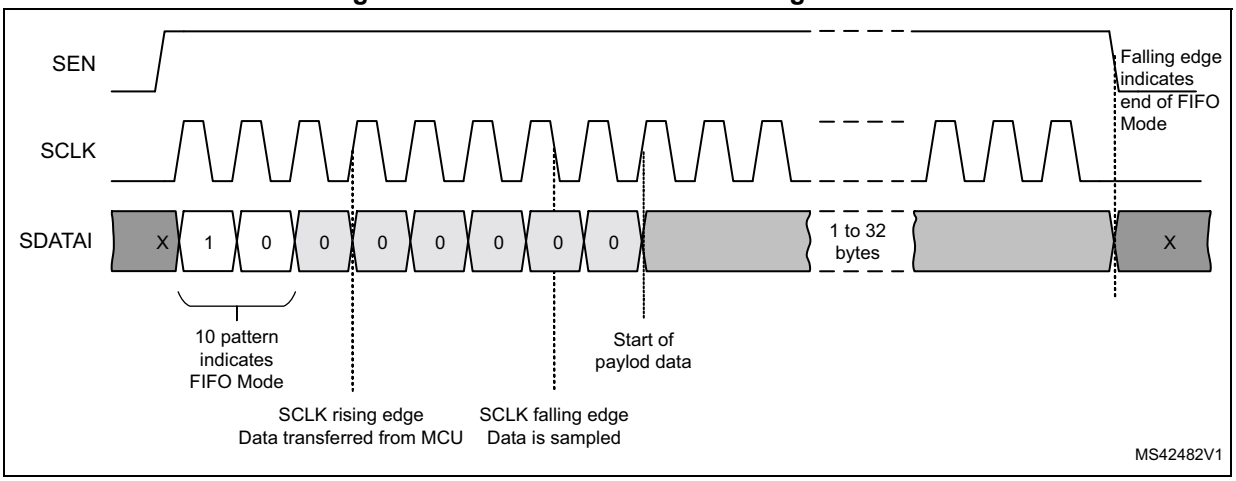


Loading transmitting data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. Difference is that in case of loading more bytes all bytes go to the FIFO. SPI operation mode bits 10 indicate FIFO operations. In case of loading transmitting data into FIFO all bits <C5 – C0> are set to 0. Then a bit-stream, the data to be sent (1 to 32 bytes), can be transferred. In case the command is terminated by putting SEN low before a packet of 8 bits (one byte) is sent, writing of that particular byte in FIFO is not performed.

Figure 8 shows how to load the Transmitting Data into the FIFO.

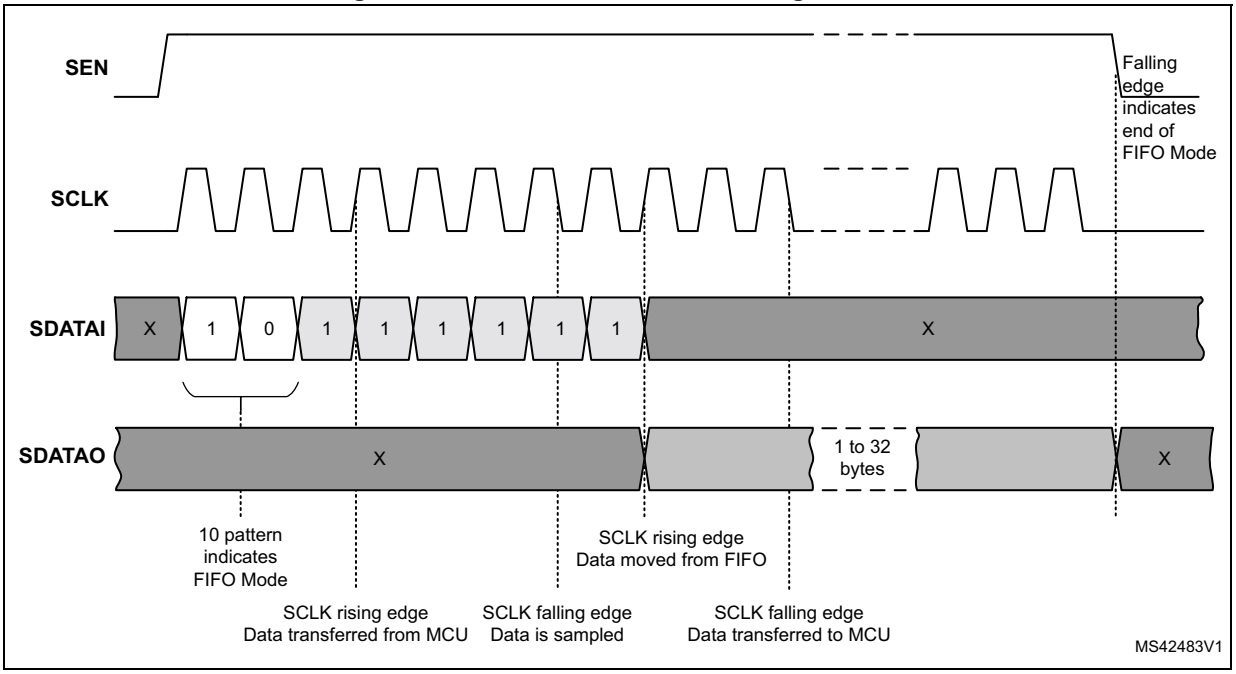
Figure 8. SPI communication: loading of FIFO



Reading received data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. Difference is that in case of reading more bytes they all come from the FIFO. SPI operation mode bits 10 indicate FIFO operations. In case of reading the received data from the FIFO all bits <C5 – C0> are set to 1. On the following SCLK rising edges the data from FIFO appears as in case of read data from addressable registers. If the command is terminated by putting SEN low before a packet of 8 bits (one byte) is read, that particular byte is considered unread and will be the first one read in next FIFO read operation.

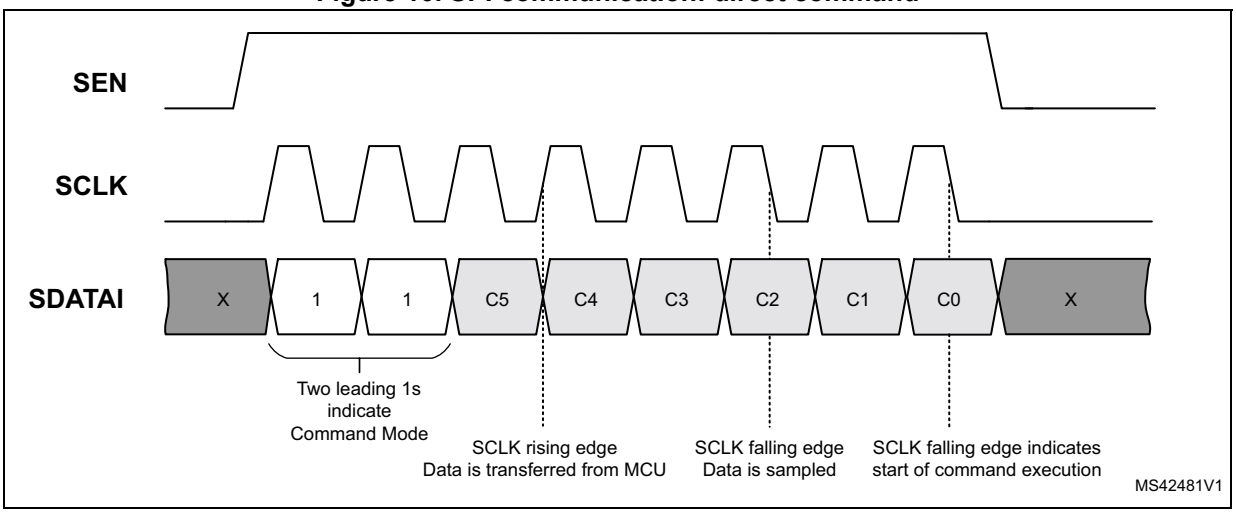
Figure 9. SPI communication: reading of FIFO



Direct Command Mode

Direct Command Mode has no arguments, so a single byte is sent. SPI operation mode bits 11 indicate Direct Command Mode. The following six bits define command code, sent MSB to LSB. The command is executed on falling edge of last clock (see *Figure 10*).

Figure 10. SPI communication: direct command



Interrupt interface

When an interrupt condition is met the source of interrupt bit is set in the *Interrupt Register* and the INTR pin transitions to high.

Table 3. INTR output

Name	Signal	Signal level	Description
INTR	Digital output	CMOS	Interrupt output pin

The microcontroller then reads the *Interrupt Register* to distinguish between different interrupt sources. After the *Interrupt Register* is read its content is reset to 0 and INTR pin signal transitions to low.

Note: There may be more than one interrupt bit set in case the microcontroller does not immediately read the Interrupt Register after the INTR signal has been set and another event causing interrupt has occurred.

If an interrupt from a certain source is not required, it can be disabled by setting corresponding bit in the *Mask Interrupt Register*. When masking a given interrupt source the interrupt is not produced, but the source of interrupt bit is still set in *Interrupt Register*.

After reading the *Interrupt Register* the 13.56 MHz clock coming from the oscillator is used to produce a reset signal that clears it and resets INTR signal. Practically in all interrupt cases the oscillator is running when an interrupt is produced. The only exception is the interrupt in the Initial NFC Target mode where only the Target Activation Detector is operating. In this case the interrupt is cleared with first SCLK rising edge following reading of the *Interrupt Register* (an extra dummy CLK pulse during reading of the *Interrupt Register* or the first SCLK pulse of the next SPI command will do the job).

FIFO water level and FIFO status registers

The ST25R3910 contains a 32 byte FIFO. In case of transmitting the Control logic shifts the data that was previously loaded by the external microcontroller to the Framing Block and further to the transmitter. During reception, the demodulated data is stored in the FIFO and the external microcontroller can download received data at a later moment.

Transmit and receive capabilities of the ST25R3910 are not limited by the FIFO size due to a FIFO water level interrupt system. During transmission an interrupt is sent (*INTR* due to FIFO water level in the *Interrupt Register*) when the content of data in the FIFO still to be sent is lower than the FIFO water level for receive. The external microcontroller can now add more data in the FIFO. The same stands for the reception: when the number of received bytes exceeds the FIFO water level for receive an interrupt is sent to inform the external controller that data has to be downloaded from FIFO.

The external controller has to serve the FIFO faster than data is transmitted or received. Using SCLK frequency that is at least double than the actual receive or transmit bit rate is recommended.

There are two settings of the FIFO water level available for receive and transmit in the *Configuration Register 5*.

After data are received the external microcontroller needs to know how long the received data string was before downloading data from the FIFO: This information is available in the *FIFO Status Register*, which displays number of bytes in the FIFO that were not read out.

The *FIFO Status Register* also contains a FIFO overflow bit, set when during reception the external processor did not react on time and more than 32 bytes were written in FIFO (the received data are lost in this case).

1.2.10 Direct commands

Table 4. Direct commands

Code	Command	Comments
000001	Set default	Puts the ST25R3910 in default state (same as after power-up)
000010	Clear	Stops all activities and clears FIFO
000100	Transmit with CRC	Starts a transmit sequence using automatic CRC generation
000101	Transmit without CRC	Starts a transmit sequence without automatic CRC generation
000110	Transmit REQA	Transmits REQA command (ISO-14443A mode only
000111	Transmit WUPA	Transmits WUPA command (ISO-14443A mode only)
001000	NFC transmit with Initial RF Collision Avoidance	Equivalent to Transmit with CRC with additional RF Collision Avoidance
001001	NFC transmit with Response RF Collision Avoidance	
001010	NFC transmit with Response RF Collision Avoidance with n=0	
010000	Mask receive data	Receive after this command is ignored

Table 4. Direct commands (continued)

Code	Command	Comments
010001	Unmask receive data	Received data following this command are normally processed (this command has priority over internal mask receive timer)
010010	AD convert	A/D conversion of signal on AD_IN pin is performed, result is stored in *A/D Output Register*
010011	Measure RF	RF amplitude is measured, result is stored in *A/D Output Register*
010100	Squelch	Performs gain reduction based on the current noise level.
010101	Clear Squelch	Resumes gain settings in place before sending Squelch command
010110	Adjust regulators	Adjusts supply regulators according to the current supply voltage level
010111	Calibrate modulation depth	Starts sequence which activates the TX, measures the modulation depth and adapts it to comply with the specified modulation depth
011000	Calibrate antenna	Starts the sequence to adjust parallel capacitances connected to TRIMx_y pins so that the antenna LC is in resonance.
011001	Check antenna resonance	Measurement of antenna LC tank resonance to determine whether calibration is needed.
011010	Clear RSSI	Clears RSSI bits and restarts the measurement
011100	Transparent mode	Enters in Transparent mode

Set Default

This direct command puts the ST25R3910 in the same state as power-up initialization. All registers are initialized to the default state.

Note: Results of different calibration and adjust commands are also lost.

This direct command is accepted in all operating modes.

Clear

This direct command stops all current activities (transmission or reception) and clears FIFO. It also clears collision and interrupt registers. This command has to be sent first in a sequence preparing a transmission (except in case of direct commands Transmit REQA and Transmit WUPA).

Transmit commands

All Transmit commands (Transmit With CRC, Transmit Without CRC, Transmit REQA and Transmit WUPA) are accepted only in case the transmitter is enabled (bit tx_en is set).

NFC transmit commands

The NFC transmit commands (NFC transmit with Initial RF Collision Avoidance, NFC transmit with Response RF Collision Avoidance, NFC transmit with Response RF Collision Avoidance with n=0) are used to transmit requests and responses in the NFC mode. Before actual transmission the RF Collision avoidance with Collision avoidance threshold defined in the *NFCIP Field Detection Threshold Register* is performed.

In the command NFC transmit with Response RF Collision Avoidance n is randomly set in a range from 0 to 3, while in the command NFC transmit with Response RF Collision Avoidance with n=0 it is set to 0. In case collision is detected during the RF Collision Avoidance the transmission is not done and an interrupt is sent with flag INTR due to NFC event.

The NFC transmit commands switch on and off the transmission block, setting the *Operation Control Register* bit tx_en in the NFC mode is not allowed.

Timing of the NFC transmit commands (see *Table 5*) is according to the ISO/IEC 18092 standard, which specifies a range for some of them.

Table 5. NFC P2P timings implemented in ST25R3910

Symbol	Parameter	Value	Unit	Comments
T_{IDT}	Initial delay time	302	µs	Initial RF Collision Avoidance
T_{RWF}	RF waiting time	37.76		-
T_{IRFG}	Initial guard time	5.11	ms	Initial RF Collision Avoidance
T_{ADT}	Active delay time	151	µs	Response RF Collision Avoidance
T_{ARFG}	Active guard time	84		
T_{GAS}	Guard time after sending response or request	65		Time during which RF field stays switched on after sending a response or a request. Not specified in the ISO/IEC 18092.

An interrupt due to end of transmission is sent when RF field is switched off.

All NFC Transmit commands are only authorized in case the ISO mode configuration bit nfc is set and the oscillator and regulators are running.

Mask Receive Data and Unmask Receive Data

After the direct command Mask Receive Data the signal rx_on that enables the RSSI and AGC operation of the receiver (see *Section 1.1.2: Receiver*) is forced to low, processing of the receiver output by the receive data framing block is disabled. This command is useful to mask receiver and receive framing from processing the data when there is actually no input and only a noise would be processed..

The direct command Unmask Receive Data is enabling normal processing of the received data (signal rx_on is set high to enable the RSSI and AGC operation), the receive data framing block is enabled. A common use of this command is to enable again the receiver operation after it was masked by the command Mask Receive Data.

The command Unmask Receive Data has to be used in the NFC target mode. The sequence implemented in the ST25R3910 supposes that every action is started with a transmit command, after sending the transmit data, the receive mode is automatically entered to process the response. Such a sequence is always in place in case of the