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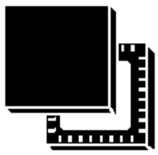
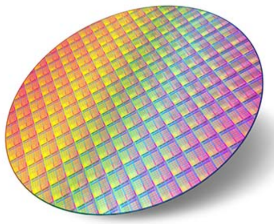
ST25R3911B

High performance HF reader / NFC initiator with 1.4 W supporting VHBR and AAT

Datasheet - production data


QFN32


Wafer

Features

- ISO 18092 (NFCIP-1) Active P2P
- ISO14443A, ISO14443B and FeliCa™
- Supports VHBR (3.4 Mbit/s PICC to PCD framing, 6.8 Mbit/s AFE and PCD to PICC framing)
- Capacitive sensing - Wake-up
- Automatic antenna tuning system providing tuning of antenna LC tank
- Automatic modulation index adjustment
- AM and PM (I/Q) demodulator channels with automatic selection
- DPO (Dynamic Power Output)
- Up to 1.4 W in case of differential output
- User selectable and automatic gain control
- Transparent and Stream modes to implement MIFARE™ Classic compliant or other custom protocols
- Possibility of driving two antennas in single ended mode
- Oscillator input capable of operating with 13.56 MHz or 27.12 MHz crystal with fast start-up
- 6 Mbit/s SPI with 96 bytes FIFO
- Wide supply voltage range from 2.4 V to 5.5 V
- Wide temperature range: -40 °C to 125 °C
- QFN32, 5 mm x 5 mm package

Description

The ST25R3911B is a highly integrated NFC Initiator / HF Reader IC, including the analog front end (AFE) and a highly integrated data framing system for ISO 18092 (NFCIP-1) initiator, ISO 18092 (NFCIP-1) active target, ISO 14443A and B reader (including high bit rates) and FeliCa™ reader. Implementation of other standard and custom protocols like MIFARE™ Classic is possible using the AFE and implementing framing in the external microcontroller (Stream and Transparent modes).

The ST25R3911B is positioned perfectly for the infrastructure side of the NFC system, where users need optimal RF performance and flexibility combined with low power.

Thanks to automatic antenna tuning (AAT) technology, the device is optimized for applications with directly driven antennas. The ST25R3911B is alone in the domain of HF reader ICs as it contains two differential low impedance (1 Ohm) antenna drivers.

The ST25R3911B includes several features that make it very suited for low power applications. It contains a low power capacitive sensor that can be used to detect the presence of a card without switching on the reader field. The presence of a card can also be detected by performing a measurement of amplitude or phase of signal on antenna LC tank, and comparing it to the stored reference. It also contains a low power RC oscillator and wake-up timer that can be used to wake up the system after a defined time period, and to check for the presence of a tag using one or more low power detection techniques (capacitive, phase or amplitude).

The ST25R3911B is designed to operate from a wide (2.4 V to 5.5 V) power supply range; peripheral interface IO pins support power supply range from 1.65 V to 5.5 V.

This is information on a product in full production.

Contents

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1 Functional overview

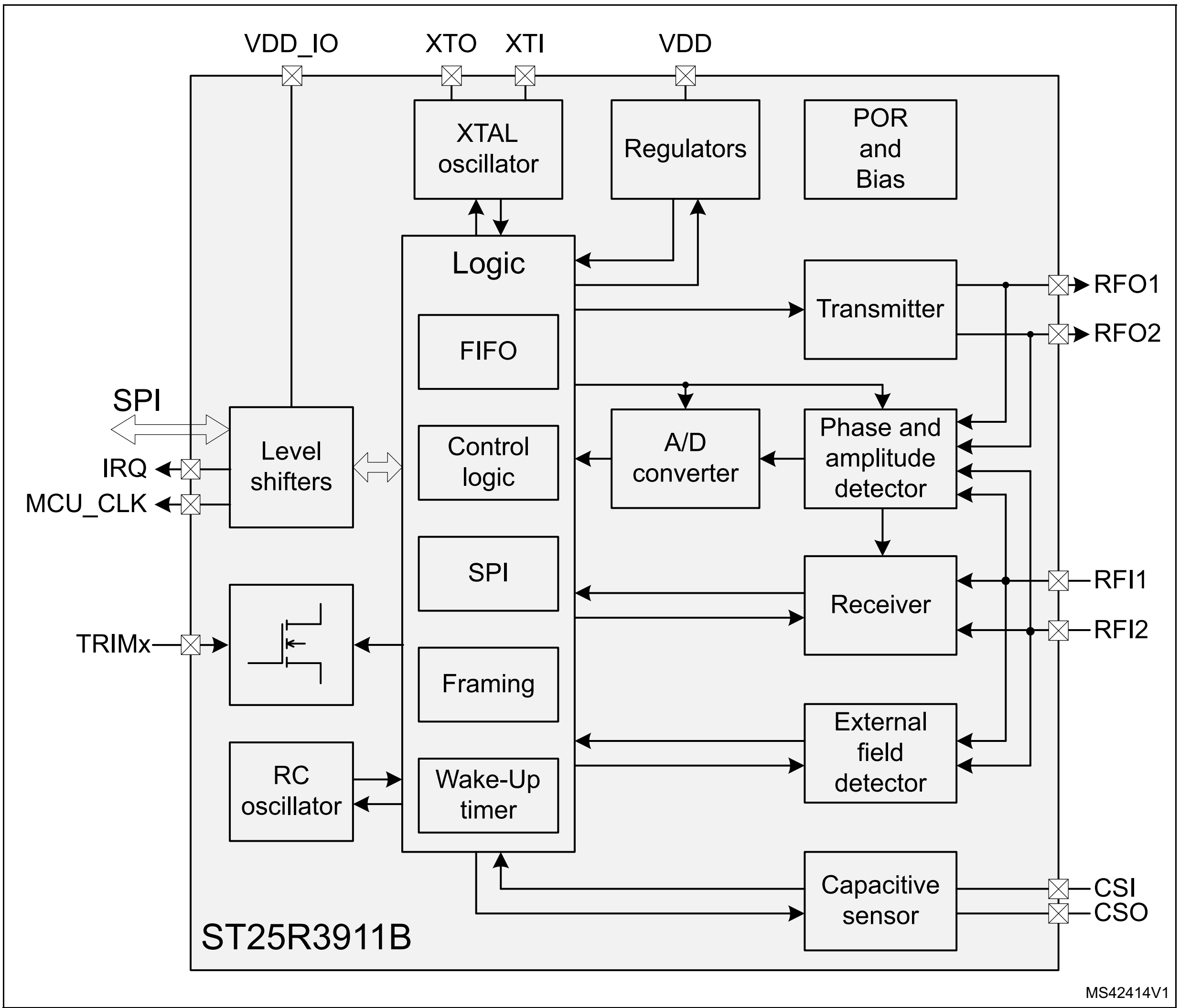
The ST25R3911B is suitable for a wide range of applications, among them

- EMV payment
- E-government
- Access control
- NFC infrastructure
- Ticketing

1.1 Block diagram

The block diagram is shown in *Figure 1*.

Figure 1. ST25R3911B block diagram



1.1.1 Transmitter

The transmitter incorporates drivers that drive external antenna through pins RFO1 and RFO2. Single sided and differential driving is possible. The transmitter block additionally contains a sub-block that modulates transmitted signal (OOK or configurable AM modulation).

The ST25R3911B transmitter is intended to directly drive antennas (without 50 Ω cable, usually antenna is on the same PCB). Operation with 50 Ω cable is also possible, but in that case some of the advanced features are not available.

1.1.2 Receiver

The receiver detects transponder modulation superimposed on the 13.56 MHz carrier signal. The receiver contains two receive chains (one for AM and another for PM demodulation) composed of a peak detector followed by two gain and filtering stages and a final digitizer stage. The filter characteristics are adjusted to optimize performance for each mode and bit rate (sub-carrier frequencies from 212 kHz to 6.8 MHz are supported). The receiver chain inputs are the RFI1 and RFI2 pins. The receiver chain incorporates several features that enable reliable operation in challenging phase and noise conditions.

1.1.3 Phase and amplitude detector

The phase detector is observing the phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals (RFI1 and RFI2). The amplitude detector is observing the amplitude of the receiver input signals (RFI1 and RFI2) via self-mixing. The amplitude of the receiver input signals (RFI1 and RFI2) is directly proportional to the amplitude of the antenna LC tank signal.

The phase detector and the amplitude detector can be used for the following purposes:

- PM demodulation by observing RFI1 and RFI2 phase variation
- Average phase difference between RFOx pins and RFIx pins is used to check and optimize antenna tuning
- Amplitude of signal present on RFI1 and RFI2 pins is used to check and optimize antenna tuning

1.1.4 A/D converter

The ST25R3911B contains a built in Analog to Digital (A/D) converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude and phase, calibration of modulation depth…). The result of the A/D conversion is stored in the *A/D Converter Output Register* and can be read via SPI.

1.1.5 Capacitive sensor

The capacitive sensor is used to implement low power detection of transponder presence, it measures the capacitance between two copper patches connected to the CSI and CSO pins. The capacitance changes with the presence of an object (card, hand). During calibration the reference capacitance (representing parasitic capacitance of the environment) is stored. In normal operation the capacitance is periodically measured and compared to the stored reference value, if the measured capacitance differs from the stored reference value by more than a register defined threshold, then an interrupt is sent to the external controller.

1.1.6 External field detector

The External field detector is a low power block used in NFC mode to detect the presence of an external RF field. It supports two different detection thresholds, Peer Detection Threshold and Collision Avoidance Threshold. The Peer Detection Threshold is used in the NFCIP-1 target mode to detect the presence of an initiator field, and is also used in active communication initiator mode to detect the activation of the target field. The Collision Avoidance Threshold is used to detect the presence of an RF field during the NFCIP-1 RF Collision Avoidance procedure.

1.1.7 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve a fast start-up. The start-up time varies with crystal type, temperature and other parameters, hence the oscillator amplitude is observed and an interrupt is sent when stable oscillator operation is reached. The use of a 27.12 MHz crystal is mandatory for VHBR operation.

The oscillator block also provides a clock signal to the external microcontroller (MCU_CLK), according to the settings in the *IO Configuration Register 1*.

1.1.8 Power supply regulators

Integrated power supply regulators ensure a high power supply rejection ratio for the complete reader system. If the reader system PSRR has to be improved, the command Adjust Regulators is sent. As a result of this command, the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to assure a stable regulated supply. The resulting regulated voltage is stored in the *Regulator and Timer Display Register*. It is also possible to define regulated voltage by writing to the *Regulator Voltage Control Register*. To decouple any noise sources from different parts of the IC there are three regulators integrated with separated external blocking capacitors (the regulated voltage of all of them is the same in 3.3 V supply mode). One regulator is for the analog blocks, one for the digital blocks, and one for the antenna drivers.

This block additionally generates a reference voltage for the analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

1.1.9 POR and Bias

This block provides the bias current and the reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit that provides a reset at power-up and at low supply voltage levels.

1.1.10 RC oscillator and Wake-Up timer

The ST25R3911B includes several possibilities of low power detection of card presence (capacitive sensor, phase measurement, amplitude measurement). The RC oscillator and the register configurable Wake-Up timer are used to schedule the periodic card presence detection.

1.1.11 ISO-14443 and NFCIP-1 framing

This block performs framing for receive and transmit according to the selected ISO mode and bit rate settings.

In reception it takes the demodulated sub-carrier signal from the receiver. It recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from the FIFO, generates parity and CRC bits, adds SOF and EOF and performs final encoding before passing the modulation signal to the transmitter.

In Transparent mode, the framing and FIFO are bypassed, the digitized sub-carrier signal (the receiver output), is directly sent to the MISO pin, and the signal applied to the MOSI pin is directly used to modulate the transmitter.

1.1.12 FIFO

The ST25R3911B contains a 96-byte FIFO. Depending on the mode, it contains either data that has been received or data to be transmitted.

1.1.13 Control logic

The control logic contains I/O registers that define operation of device.

1.1.14 SPI

A 4-wire Serial Peripheral Interface (SPI) is used for communication between the external microcontroller and the ST25R3911B.

1.2 Application information

The minimum configurations required to operate the ST25R3911B are shown in *Figure 2* and *Figure 3*.

Figure 2. Minimum configuration with single sided antenna driving (including EMC filter)

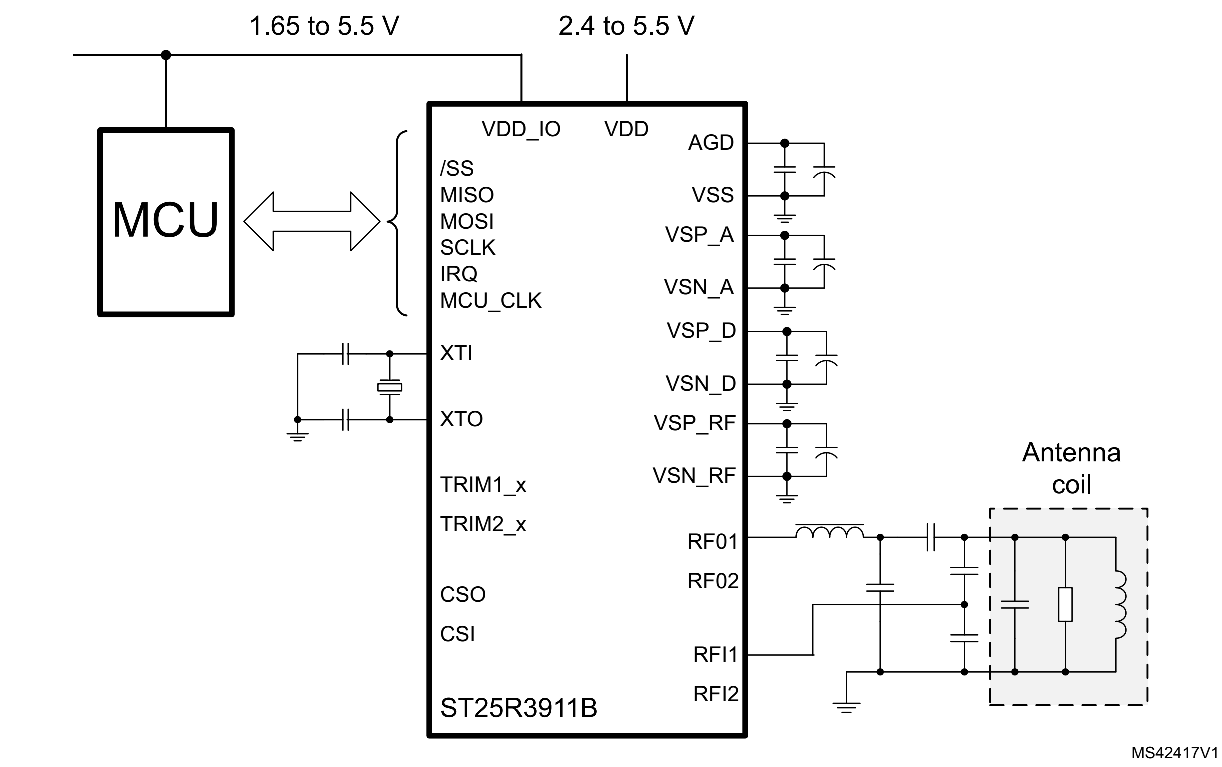
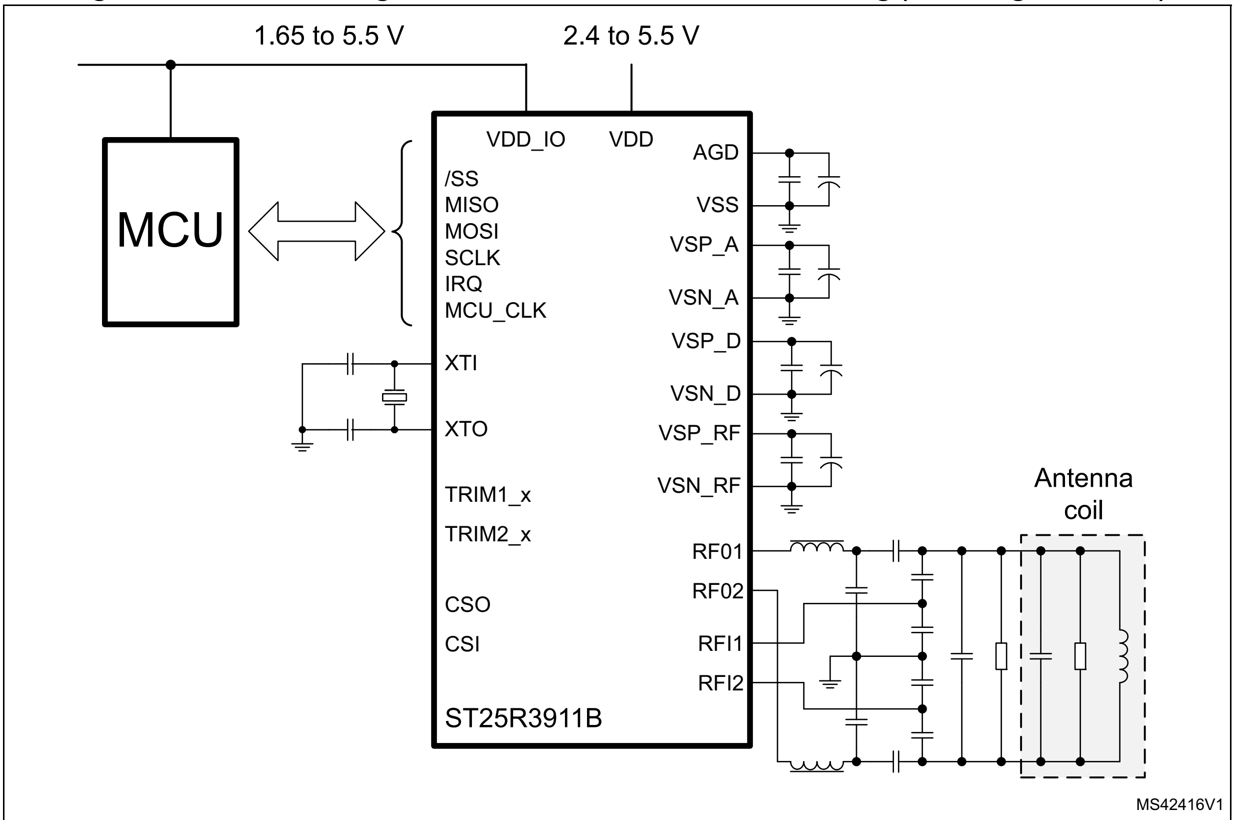


Figure 3. Minimum configuration with differential antenna driving (including EMC filter)



1.2.1 Operating modes

The ST25R3911B operating mode is defined by the contents of the *Operation Control Register*.

At power-up all bits of the *Operation Control Register* are set to 0, the ST25R3911B is in Power-down mode. In this mode AFE static power consumption is minimized, only the POR and part of the bias are active, while the regulators are transparent and are not operating. The SPI is still functional in this mode so all settings of ISO mode definition and configuration registers can be done.

Control bit en (bit 7 of the *Operation Control Register*) is controlling the quartz crystal oscillator and regulators. When this bit is set, the device enters in Ready mode. In this mode the quartz crystal oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable.

Enable of receiver and transmitter are separated so it is possible to operate one without switching on the other (control bits rx_en and tx_en). In some cases this may be useful, if the reader field has to be maintained and there is no transponder response expected, the receiver can be switched-off to save current. Another example is the NFCIP-1 active communication receive mode in which the RF field is generated by the initiator and only the receiver operates.

Asserting the *Operation Control Register* bit wu while the other bits are set to 0 puts the ST25R3911B into the Wake-Up mode that is used to perform low power detection of card presence. In this mode the low power RC oscillator and register configurable Wake-Up timer are used to schedule periodic measurement(s). When a difference of the measured value vs. the predefined reference is detected an interrupt is sent to wake-up the microcontroller.

1.2.2 Transmitter

The transmitter contains two identical push-pull driver blocks connected to the pins RFO1 and RFO2. These drivers are differentially driving the external antenna LC tank. It is also possible to operate only one of the two drivers by setting the *IO Configuration Register 1* bit single to 1. Each driver is composed of eight segments having binary weighted output resistance. The MSB segment typical ON resistance is 2 Ω, when all segments are turned on; the output resistance is typically 1 Ω. All segments are turned on to define the normal transmission (non-modulated) level. It is also possible to switch off certain segments when driving the non-modulated level to reduce the amplitude of the signal on the antenna and/or to reduce the antenna Q factor without making any hardware changes. The *RFO Normal Level Definition Register* defines which segments are turned on to define the normal transmission (non-modulated) level. Default setting is that all segments are turned on.

Using the single driver mode the number of the antenna LC tank components (and therefore the cost) is halved, but also the output power is reduced. In single mode it is possible to connect two antenna LC tanks to the two RFO outputs and multiplex between them by controlling the *IO Configuration Register 1* bit rfo2.

In order to transmit the data the transmitter output level needs to be modulated. Both AM and OOK modulation are supported. The type of modulation is defined by setting the bit tr_am in the *Auxiliary Definition Register*.

During the OOK modulation (for example ISO14443A) the transmitter drivers stop driving the carrier frequency. As consequence the amplitude of the antenna LC tank oscillation decays, the time constant of the decay is defined with the LC tank Q factor. The decay time in case of OOK modulation can be shortened by asserting the *Auxiliary Definition Register* bit ook_hr. When this bit is set to logic one the drivers are put in tristate during the OOK modulation.

AM modulation (for example ISO14443B) is done by increasing the output driver impedance during the modulation time. This is done by reducing the number of driver segments that are turned on. The AM modulated level can be automatically adjusted to the target modulation depth by defining the target modulation depth in the *AM Modulation Depth Control Register* and sending the Calibrate Modulation Depth direct command. Refer to *Section 1.2.20: AM modulation depth: definition and calibration* for further details.

Slow transmitter ramping

When the transmitter is enabled it starts to drive the antenna LC tank with full power, the ramping of the field emitted by antenna is defined by antenna LC tank Q factor.

However there are some reader systems where the reader field has to ramp up with a longer transition time when it is enabled. The STIF (Syndicat des transports d'Ile de France) specification requires a transition time from 10% to 90% of field longer than or equal to 10 µs.The ST25R3911B supports that feature. It is realized by collapsing VSP_RF regulated voltage when transmitter is disabled and ramping it when transmitter is enabled. Typical transition time is 15 µs at 3 V supply and 20 µs at 5 V supply.

Procedure to implement the slow transition:

1. When transmitter is disabled set *IO Configuration Register 2* bit slow_up to 1. Keep this state for at least 2 ms to allow discharge of VSP_RF.
2. Enable transmitter, its output will ramp slowly.
3. Before sending any command set the bit slow_up back to 0.

1.2.3 Receiver

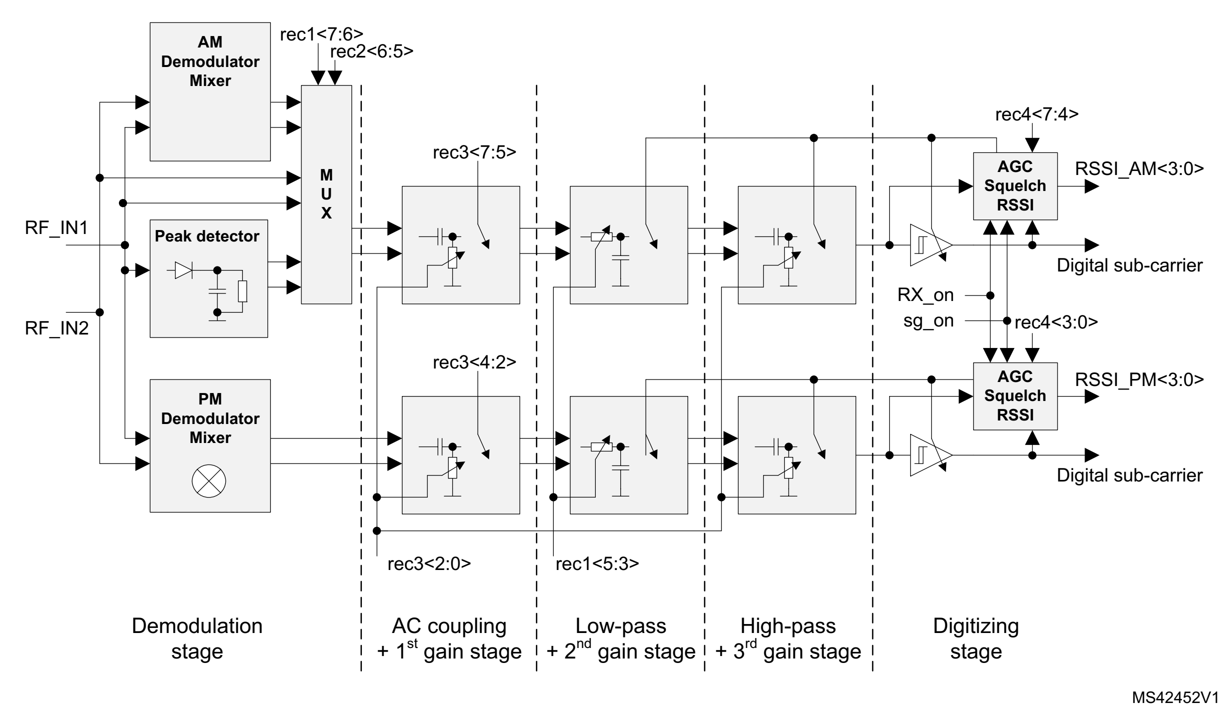
The receiver performs demodulation of the transponder sub-carrier modulation that is superimposed on the 13.56 MHz carrier frequency. It performs AM and/or PM demodulation, amplification, band-pass filtering and digitalization of sub-carrier signals. Additionally it performs RSSI measurement, automatic gain control (AGC) and Squelch.

In typical applications the receiver inputs RFI1 and RFI2 are outputs of capacitor dividers connected directly to the terminals of the antenna coil. This concept ensures that the two input signals are in phase with the voltage on the antenna coil. The design of the capacitive divider must ensure that the RFI1 and RFI2 input signal peak values do not exceed the V_{SP_A} supply voltage level.

The receiver comprises two complete receive channels, one for the AM demodulation and another one for the PM demodulation. In case both channels are active the selection of the channel used for reception framing is done automatically by the receive framing logic. The receiver is switched on when *Operation Control Register* bit rx_en is set to one. Additionally the *Operation Control Register* contains bits rx_chn and rx_man; rx_chn defines whether both, AM and PM, demodulation channels will be active or only one of them, while bit rx_man defines the channel selection mode in case both channels are active (automatic or manual). Operation of the receiver is controlled by four receiver configuration registers.

The operation of the receiver is additionally controlled by the signal rx_on that is set high when a modulated signal is expected on the receiver input. This signal is used to control RSSI and AGC and also enables processing of the receiver output by the framing logic. Signal rx_on is automatically set to high after the Mask Receive Timer expires. Signal rx_on can also be directly controlled by the controller by sending direct commands Mask Receive Data and Unmask Receive Data. *Figure 4* details the receiver block diagram.

Figure 4. Receiver block diagram



Demodulation stage

The first stage performs demodulation of the transponder sub-carrier signal, superimposed on the HF field carrier. Two different blocks are implemented for AM demodulation:

- Peak detector
- AM demodulator mixer.

The choice of the used demodulator is made by the *Receiver Configuration Register 1* bit amd_sel.

The peak detector performs AM demodulation using a peak follower. Both the positive and negative peaks are tracked to suppress any common mode signal. The peak detector is limited in speed; it can operate for sub-carrier frequencies up to fc/8 (1700 kHz). Its demodulation gain is G = 0.7. Its input is taken from one demodulator input only (usually RFI1).

The AM demodulator mixer uses synchronous rectification of both receiver inputs (RFI1 and RFI2). Its gain is G = 0.55. The mixer demodulator is optimized for VHBR sub-carrier frequencies (fc/8 and higher). For sub-carrier frequency fc/8 (1700 kHz) both peak follower and mixer demodulator can be used, while for fc/4 and fc/2 only the mixer demodulator can be used.

PM demodulation is also done by a mixer. The PM demodulator mixer has differential outputs with 60 mV differential signal for 1% phase change (16.67 mV / °). Its operation is optimized for sub-carrier frequencies up to fc/8 (1700 kHz).

In case the demodulation is done externally, it is possible to multiplex the LF signals applied to pins RFI1 and RFI2 directly to the gain and filtering stage by selecting the *Receiver Configuration Register 2* bit lf_en.

Filtering and gain stages

The receiver chain has band pass filtering characteristics. Filtering is optimized to pass sub-carrier frequencies while rejecting carrier frequency and low frequency noise and DC component. Filtering and gain is implemented in three stages, where the first and the last stage have first order high pass characteristics, and the second stage has second order low pass characteristic.

Gain and filtering characteristics can be optimized by writing the *Receiver Configuration Register 1* (filtering), the *Receiver Configuration Register 3* (gain in first stage) and the *Receiver Configuration Register 4* (gain in second and third stage).

The gain of the first stage is about 20 dB and can be reduced in six 2.5 dB steps. There is also a special boost mode available, which boosts the maximum gain by additional 5.5 dB. In case of VHBR (fc/8 and fc/4) the gain is lower. The first stage gain can only be modified by writing *Receiver Configuration Register 3*. The default setting of this register is the minimum gain. The default first stage zero is set at 60 kHz, it can also be lowered to 40 kHz or to 12 kHz by writing option bits in the *Receiver Configuration Register 1*. The control of the first and third stage zeros is done with common control bits (see *Table 1*).

Table 1. First and third stage zero setting

rec1<2> h200	rec1<1> h80	rec1<0> z12k	First stage zero	Third stage zero
0	0	0	60 kHz	400 kHz
1	0	0	60 kHz	200 kHz
0	1	0	40 kHz	80 kHz
0	0	1	12 kHz	200 kHz
0	1	1	12 kHz	80 kHz
1	0	1	12 kHz	200 kHz
Others			Not used	

The gain in the second and third stage is 23 dB and can be reduced in six 3 dB steps. The gain of these two stages is included in the AGC and Squelch loops. It can also be manually set in *Receiver Configuration Register 4*. Sending of direct command Reset Rx Gain is necessary to reset the AGC, Squelch and RSSI block. Sending this command clears the current Squelch setting and loads the gain reduction configuration from *Receiver Configuration Register 4* into the internal shadow registers of the AGC and Squelch block. The second stage has a second order low pass filtering characteristic, the pass band is adjusted according to the sub-carrier frequency using the bits lp2 to lp0 of the *Receiver Configuration Register 1*.

See *Table 2* for -1 dB cut-off frequency for different settings.

Table 2. Low pass control

rec1<5> lp2	rec1<4> lp1	rec1<3> lp0	-1 dB point
0	0	0	1200 kHz
0	0	1	600 kHz
0	1	1	300 kHz
1	0	0	2 MHz
1	0	1	7 MHz
Others			Not used

Table 3 provides information on the recommended filter settings. For all supported operation modes and receive bit rates there is an automatic preset defined, additionally some alternatives are listed. Automatic preset is done by sending direct command Analog Preset. There is no automatic preset for Stream and Transparent modes. Since the selection of the filter characteristics also modifies gain, the gain range for different filter settings is also listed.

Table 3. Receiver filter selection and gain range

rec1<5:3>lp<2:0>	rec1<2>h200	rec1<1>h80	rec1<0>z12k	Gain (dB)					Comments
				Max all	Min1 Max23	Max1 Min23	Min all	With boost	
000	0	0	0	43.4	28.0	26.4	11.0	49.8	Automatic preset for ISO14443A fc/128 and NFC Forum Type 1 Tag
000	1	0	0	44.0	29.0	27.5	12.0	49.7	Automatic preset for ISO14443B fc/128 ISO14443 fc/64
001	1	0	0	44.3	29	27.0	11.7	49.8	Recommended for 424/484 kHz sub-carrier
000	0	1	0	41.1	25.8	23.6	8.3	46.8	Alternative choice for ISO14443 fc/32 and fc/16
100	0	1	0	32.0	17.0	17.2	2.0	37.6	Automatic preset for ISO14443 fc/32 and fc/16 Alternative choice for fc/8 (1.7 kb/s)
100	0	0	0	32.0	17.0	17.2	2.0	37.6	Alternative choice for fc/8 (1.7 kb/s)
000	0	1	1	41.1	25.8	23.6	8.3	46.8	Automatic preset FeliCa™ (fc/64, fc/32) Alternative choice for ISO14443 fc/32 and fc/16
101	0	1	0	30.0	20.0	12.0	2.0	34.0	Alternative choice for fc/8 and fc/4
101	1	0	0	30.0	20.0	12.0	2.0	34.0	Automatic preset for fc/8 and fc/4
000	1	0	1	36.5	21.5	24.9	9.9	41.5	Automatic preset for NFCIP-1 (initiator and target)

Digitizing stage

The digitizing stage produces a digital representation of the sub-carrier signal coming from the receiver. This digital signal is then processed by the receiver framing logic. The digitizing stage consists of a window comparator with adjustable digitizing window (five possible settings, 3 dB steps, adjustment range from ±33 mV to ±120 mV). Adjustment of the digitizing window is included in the AGC and Squelch loops. In addition, the digitizing window can also be set manually in the *Receiver Configuration Register 4*.

AGC, Squelch and RSSI

As mentioned above, the second and third gain stage gain and the digitizing stage window are included in the AGC and Squelch loops. Eleven settings are available. The default state features minimum digitizer window and maximum gain. The first four steps increase the digitizer window in 3 dB steps, the next six steps additionally reduce the gain in the second and third gain stage, again in 3 dB steps. The initial setting with whom Squelch and AGC start is defined in *Receiver Configuration Register 4*. The *Gain Reduction State Register* displays the actual state of gain that results from Squelch, AGC and initial settings in *Receiver Configuration Register 4*. During bit anticollision like Type A, the AGC should be disabled.

Squelch

This feature is designed for operation of the receiver in noisy conditions. The noise can come from tags (caused by the processing of reader commands), or it can come from a noisy environment. This noise may be misinterpreted as start of transponder response, resulting in decoding errors.

During execution of the Squelch procedure the output of the digitizing comparator is observed. In case there are more than two transitions on this output in a 50 µs time period, the receiver gain is reduced by 3 dB, and the output is observed during the next 50 µs. This procedure is repeated until the number of transitions in 50 µs is lower or equal to two, or until the maximum gain reduction is reached. This gain reduction can be cleared sending the direct command Reset Rx Gain.

There are two possibilities of performing squelch: automatic mode and using the direct command Squelch.

1. Automatic mode is enabled in case bit sqm_dyn in the *Receiver Configuration Register 2* is set. It is activated automatically 18.88 µs after end of Tx and is terminated when the Mask Receive timer expires. This mode is primarily intended to suppress noise generated by tag processing during the time when a tag response is not expected (covered by Mask Receive timer).
2. Command Squelch is accepted in case it is sent when signal rx_on is low. It can be used when the time window in which noise is present is known by the controller.

AGC

AGC (Automatic Gain Control) is used to reduce gain to keep the receiver chain out of saturation. With gain properly adjusted the demodulation process is also less influenced by system noise.

AGC action starts when signal rx_on is asserted high and is reset when it is reset to low. At the high to low transitions of the rx_on signal the state of the receiver gain is stored in the *Gain Reduction State Register*. Reading this register at a later stage gives information on the gain setting used during last reception.

When AGC is switched on the receiver gain is reduced so that the input to the digitizer stage is not saturated. The AGC system comprises a comparator with a window 3.5 times larger than that of the digitizing window comparator. When the AGC function is enabled the gain is reduced until there are no transitions on the output of its window comparator. This procedure ensures that the input to the digitizing window comparator is less than 3.5 times larger than its threshold.

AGC operation is controlled by the control bits agc_en, agc_m and agc_fast in the *Receiver Configuration Register 2*. Bit agc_en enables the AGC operation, bit agc_m defines the AGC mode, and bit agc_alg defines the AGC algorithm.

Two AGC modes are available. The AGC can operate during the complete Rx process (as long as signal rx_on is high), or it can be enabled only during the first eight sub-carrier pulses.

Two AGC algorithms are available. The AGC can either start by presetting code 4h (max digitizer window, max gain) or by resetting the code to 0h (min digitizer window, max gain).

The algorithm with preset code is faster, therefore it is recommended for protocols with short SOF (like ISO14443A fc/128).

Default AGC settings are:

- AGC is enabled
- AGC operates during complete Rx process
- algorithm with preset is used.

RSSI

The receiver also performs the RSSI (Received Signal Strength Indicator) measurement for both channels. The RSSI measurement is started after the rising edge of rx_on. It stays active as long as signal rx_on is high, it is frozen while rx_on is low. The RSSI is a peak hold system, and the value can only increase from the initial zero value. Every time the AGC reduces the gain the RSSI measurement is reset and starts from zero. Result of RSSI measurements is a 4-bit value that can be observed by reading the *RSSI Display Register*. The LSB step is 2.8 dB, and the maximum code is Dh (13d).

Since the RSSI measurement is of peak hold type the RSSI measurement result does not follow any variations in the signal strength (the highest value will be kept). In order to follow RSSI variations it is possible to reset the RSSI bits and restart the measurement by sending the direct command Clear RSSI.

Receiver in NFCIP-1 active communication mode

There are several features built into the receiver to enable reliable reception of active NFCIP-1 communication. All these settings are automatically preset by sending the direct command Analog Preset after the NFCIP-1 mode has been configured. In addition to the filtering options, there are two NFCIP-1 active communication mode specific configuration bits stored in the *Receiver Configuration Register 3*.

Bit lim enables clipping circuits that are positioned after the first and second gain stages. The function of the clipping circuits is to limit the signal level for the following filtering stage (when the NFCIP-1 peer is close the input signal level can be quite high).

Bit rg_nfc forces gain reduction of second and third filtering stage to -6 dB while keeping the digitizer comparator window at maximum level.

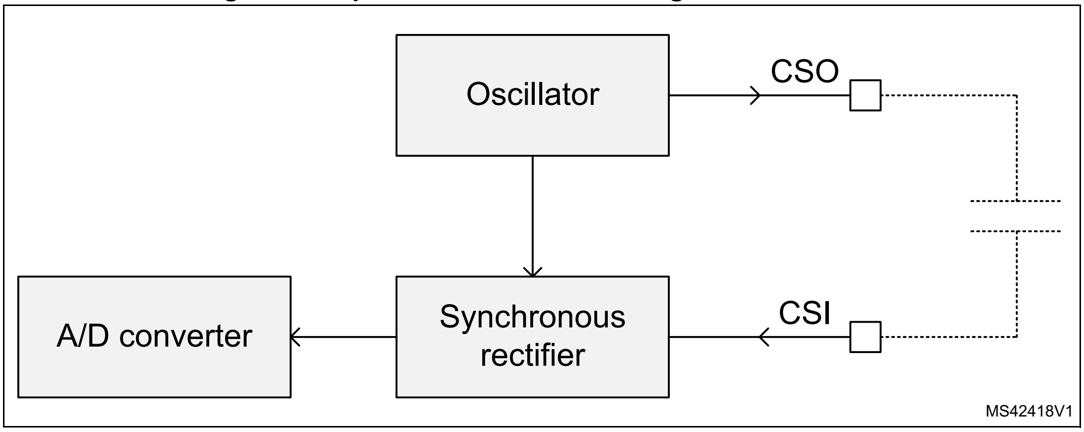
1.2.4 Capacitive sensor

The Capacitive sensor block (*Figure 5*) gives the possibility of low power detection of tag presence.

The capacitive measurement system comprises two electrodes. One is the excitation electrode emitting an electrical field of a fixed frequency in the range of a few hundred kHz (CSO) and the second one is the sensing electrode (CSI). The amount of charge generated in the sensing electrode represents the capacitance between the two electrodes. The capacitive sensor electrodes are tolerant to parasitic capacitance to ground (up to 25 pF) and to input leakage (up to 1 MΩ).

Since the charge on the sensing electrode is generated with the frequency of the excitation electrode, a synchronous rectifier is used to detect it. This ensures good rejection of interference and high tolerance to parasitic capacitances (to all nodes except the excitation electrode). The synchronous rectifier output is a DC voltage linearly proportional to the capacitance between the excitation and sensing electrode. The output DC voltage is converted by the A/D converter in absolute mode. The result is stored in the *A/D Converter Output Register* (see also *Section 1.2.8: A/D converter*).

Figure 5. Capacitive sensor block diagram



Any conductive object (human hand or tag antenna windings) approaching the two electrodes changes the capacitance between the excitation and sensing electrode as it 'shortens' the distance between the two by providing conductance on the part of the path between the two electrodes.

The capacitance measurement is started by sending the direct command Measure Capacitance. The ST25R3911B can also be configured to automatically wake-up and perform periodic capacitance measurements. The result is compared to a stored reference or to an average of previous measurements and in case the difference is greater than a predefined value an IRQ is triggered to wake-up the controller (see also *Section 1.2.5: Wake-Up mode*).

The capacitive sensor gain can be adjusted in *Capacitive Sensor Control Register*. The default gain is 2.8 V/pF (typical value), the maximum gain is 6.5 V/pF (typical value). Since the LSB of the A/D converter corresponds to approximately 7.8 mV, the default gain results in a sensitivity of 2.8 fF/LSB (1.2 fF/LSB in case of maximum gain).

The duration of the capacitance measurement is 200 µs, and the current consumption during the measurement is 1.1 mA (typical value). As an example, if the capacitive measurement is performed every 100 ms in Wake-Up mode, then the resulting average current consumption is 5.8 µA (3.6 µA is the standby consumption in Wake-Up mode).

Capacitor sensor calibration

The capacitive sensor comprises a calibration unit that internally compensates the parasitic capacitances between CSI and CSO, thus leaving full measurement range for information about capacitance variation. Five bits are used to control the calibration. The minimum calibration step and the available calibration range are, respectively, 0.1 pF and 3.1 pF. The calibration can be done manually by writing to the *Capacitive Sensor Control Register* or automatically by sending the direct command Calibrate Capacitive Sensor. The status of the Calibrate Capacitive Sensor command and the resulting calibration value are stored in the *Capacitive Sensor Display Register*.

In order to avoid interference of the capacitive sensor with the Xtal oscillator and the reader magnetic field and to assure repetitive results it is strongly recommended to perform capacitance measurement and calibration in Power-down mode only.

1.2.5 Wake-Up mode

Asserting the *Operation Control Register* bit wu while the other bits are set to 0 puts the ST25R3911B in Wake-Up mode, used to perform low power detection of card presence. The ST25R3911B includes several possibilities of low power detection of a card presence (capacitive sensor, phase measurement, amplitude measurement). An integrated low power 32 kHz RC oscillator and a register configurable Wake-Up timer are used to schedule periodic detection.

Usually the presence of a card is detected by a so-called polling loop. In this process the reader field is periodically turned on and the controller checks whether a card is present using RF commands. This procedure consumes a lot of energy since the reader field has to be turned on for 5 ms before a command can be issued.

Low power detection of card presence is performed by detecting a change in the reader environment, produced by a card. When a change is detected, an interrupt is sent to the controller. As a result, the controller can perform a regular polling loop.

In the Wake-Up mode the ST25R3911B periodically performs the configured reader environment measurements and sends an IRQ to the controller when a difference to the configured reference value is detected.

Detection of card presence can be done by performing phase,amplitude and capacitive sensor measurements.

Presence of a card close to the reader antenna coil produces a change of the antenna LC tank signal phase and amplitude. The reader field activation time needed to perform the phase or the amplitude measurement is extremely short (~20 µs) compared to the activation time needed to send a protocol activation command.

Additionally the power level during the measurement can be lower than the power level during normal operation since the card does not have to be powered to produce a coupling effect. The emitted power can be reduced by changing the *RFO Normal Level Definition Register*.

The capacitive sensor detects a change of the parasitic capacitance between the two excitation electrodes. This change in capacitance can be caused by a card antenna or a hand holding the card. See *Section 1.1.5: Capacitive sensor* for a detailed information on the capacitive sensor.

The registers on locations from 31h to 3Dh are dedicated to Wake-Up timer configuration and display. The *Wake-Up Timer Control Register* is the main Wake-Up mode configuration register. The timeout period between the successive detections and the measurements are selected in this register. Timeouts in the range from 10 to 800 ms are available, 100 ms is the default value. Any combination of available measurements can be selected (one, two or all of them).

The next twelve registers (32h to 3Dh) are configuring the three possible detection measurements and storing the results, four registers are used for each measurement.

An IRQ is sent when the difference between a measured value and the reference value is larger than the configured threshold value. There are two possible definitions for the reference value:

1. The ST25R3911B can calculate the reference based on previous measurements (auto-averaging)
2. The controller determines the reference and stores it in a register

The first register in the series of four is the *Amplitude Measurement Configuration Register*. The difference to the reference value that triggers the IRQ, the method of reference value definition and the weight of the last measurement result in case of auto-averaging are defined in this register. The next register is storing the reference value in case the reference is defined by the controller. The following two registers are display registers. The first one stores the auto-averaging reference, and the second one stores the result of the last measurement.

The Wake-Up mode configuration registers have to be configured before the Wake-Up mode is entered. Any modification of the Wake-Up mode configuration while it is active may result in unpredictable behavior.

Auto-averaging

In case of auto-averaging the reference value is recalculated after every measurement as

NewAverage = OldAverage + (MeasuredValue - OldAverage) / Weight

The calculation is done on 13 bits to have sufficient precision.The auto-averaging process is initialized when the Wake-Up mode is entered for the first time after initialization (at power-up or after Set Default command). The initial value is taken from the measurement display registers (for example *Amplitude Measurement Display Register*) until the content of this register is not zero.

Every Measurement Configuration register contains a bit that defines whether the measurement that causes an interrupt is taken in account for the average value calculation (for example bit am_aam of the *Amplitude Measurement Configuration Register*).

1.2.6 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. The operation of quartz crystal oscillator is enabled when the *Operation Control Register* bit en is set to one. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable (see *Section 1.3.24: Main Interrupt Register*).

The status of oscillator can be observed by observing the *Auxiliary Display Register* bit osc_ok. This bit is set to ‘1’ when oscillator frequency is stable.

The oscillator is based on an inverter stage supplied by a controlled current source. A feedback loop is controlling the bias current in order to regulate amplitude on XTI pin to 1 V_{pp}.

To enable a fast reader start-up an interrupt is sent when the oscillator amplitude exceeds 750 mV_{pp}.

Division by two ensures that 13.56 MHz signal has a duty cycle of 50%, which is better for the transmitter performance (no PW distortion). Use of 27.12 MHz crystal is therefore recommended for better performance.

In case of 13.56 MHz crystal, the bias current of stage that is digitizing oscillator signal is increased to assure as low PW distortion as possible.

Note: In case of VHBR reception (bit rates fc/8 and above) it is mandatory to use the 27.12 MHz crystal since high frequency clock is needed for receive framing.

The oscillator output is also used to drive a clock signal output pin MCU_CLK) that can be used by the external microcontroller. The MCU_CLK pin is configured in the *IO Configuration Register 2*.

1.2.7 Timers

The ST25R3911B contains several timers that eliminate the need to run counters in the controller, thus reducing the effort of the controller code implementation and improve portability of code to different controllers.

Every timer has one or more associated configuration registers in which the timeout duration and different operating modes are defined. These configuration registers have to be set while the corresponding timer is not running. Any modification of timer configuration while the timer is active may result in unpredictable behavior.

All timers except the Wake-Up timer are stopped by direct command Clear.

Note: In case bit nrt_emv in the General Purpose and No-Response Timer Control Register is set to one, the No-Response timer is not stopped

Mask Receive timer and No-Response timer

Mask Receive timer and No-Response timer are both automatically started at the end of transmission (at the end of EOF).

Mask Receive timer

The Mask Receive timer is blocking the receiver and reception process in framing logic by keeping the rx_on signal low after the end of Tx during the time the tag reply is not expected.

While the Mask Receive timer is running, the Squelch is automatically turned on (if enabled). Mask Receive timer does not produce an IRQ.

The Mask Receive timer timeout is configured in the *Mask Receive Timer Register*.

In the NFCIP-1 active communication mode the Mask Receive timer is started when the peer NFC device (a device with whom communication is going on) switches on its field.

The Mask Receive timer has a special use in the low power Initial NFC Target Mode. After the initiator field has been detected the controller turns on the oscillator, regulator and receiver. Mask Receive timer is started by sending direct command Start Mask Receive Timer. After the Mask Receive Timer expires the receiver output starts to be observed to detect start of the initiator message. In this mode the Mask Receive timer clock is additionally divided by eight it (one count is 512/fc) to cover range up to about 9.6 ms.