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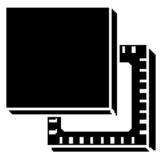
ST25RU3993

UHF RFID single chip reader EPC Class1 Gen2 compatible

Datasheet - production data



QFN48

Features

- Supply voltage range 3.0 to 3.6 V
  - Limited operation possible down to 2.7 V
  - Maximum PA supply voltage 4.3 V
  - Peripheral I/O supply range 1.65 to 5.5 V
- Protocol support for:
  - ISO 18000-6C (EPC Class1 Gen2)
  - ISO 29143 (Air interface for mobile RFID)
  - ISO 18000-6A/B through direct mode
- DRM: 250 kHz and 320 kHz filters for M4 and M8
- Integrated supply regulators
- Frequency hopping support
- ASK or PR-ASK modulation
- Automatic I/Q selection
- Phase bit for tag tracking with 8-bit linear RSSI
- Temperature range: -40 °C to 85 °C
- 48-pin QFN (7x7x0.9 mm) package

Description

The ST25RU3993 is an EPC Class 1 Gen 2 RFID reader IC that implements all the relevant protocols, including ISO 18000-6C, the ISO 29143 air-interface protocol for mobile RFID interrogators, and ISO 18000-6A/B for operation in direct mode. It includes an on-chip VCO and a power amplifier, and offers a complete set of RFID features including Dense Reader Mode (DRM) functionality and support for frequency-hopping, low-level transmission coding, low-level decode, data framing and CRC checking.

The ST25RU3993 operates at very low-power, making it suitable for use in portable and battery-powered equipment such as mobile phones.

Packaged in a 7x7 mm QFN, the ST25RU3993 is able to deliver very high sensitivity and provides high immunity against the effects of antenna reflection and self-jamming. This is critical in mobile and embedded applications, in which antenna design is often compromised by cost or size constraints. High sensitivity enables the end-products to achieve their required read range while using a simpler and cheaper antenna, thus reducing overall system cost.

Thanks to its high level of integration, the ST25RU3993 requires only an external 8-bit microcontroller to create a complete RFID reader system, thus eliminating the need for a complex RFID co-processor.

Contents

List of tables

List of figures

1 Description

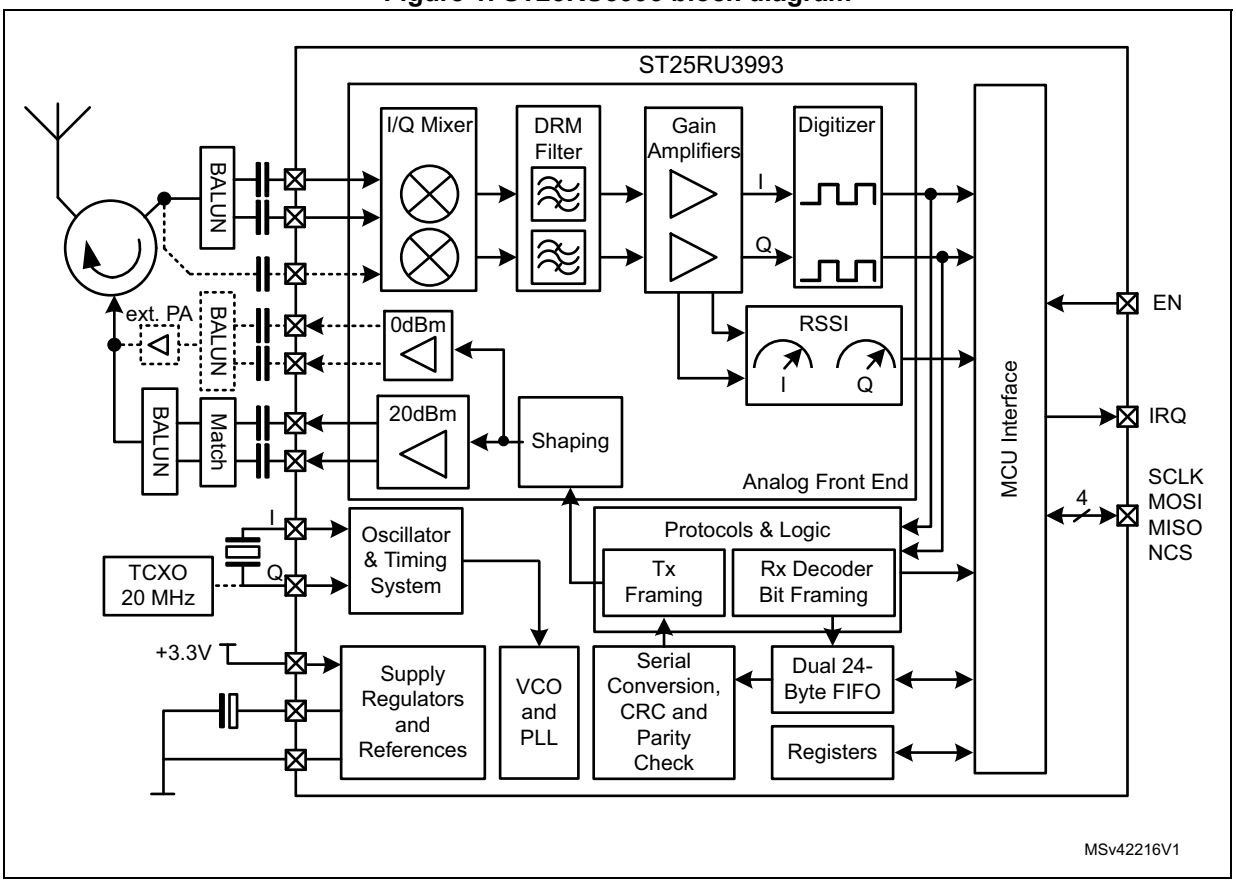
The ST25RU3993 device is ideally suited for:

- Embedded consumer/industrial applications with cost constraints such as beverage dispensing
- Hand-held readers
- Mobile UHF RFID readers
- Battery-powered stationary readers

1.1 Block diagram

The block diagram is shown in *Figure 1*.

Figure 1. ST25RU3993 block diagram

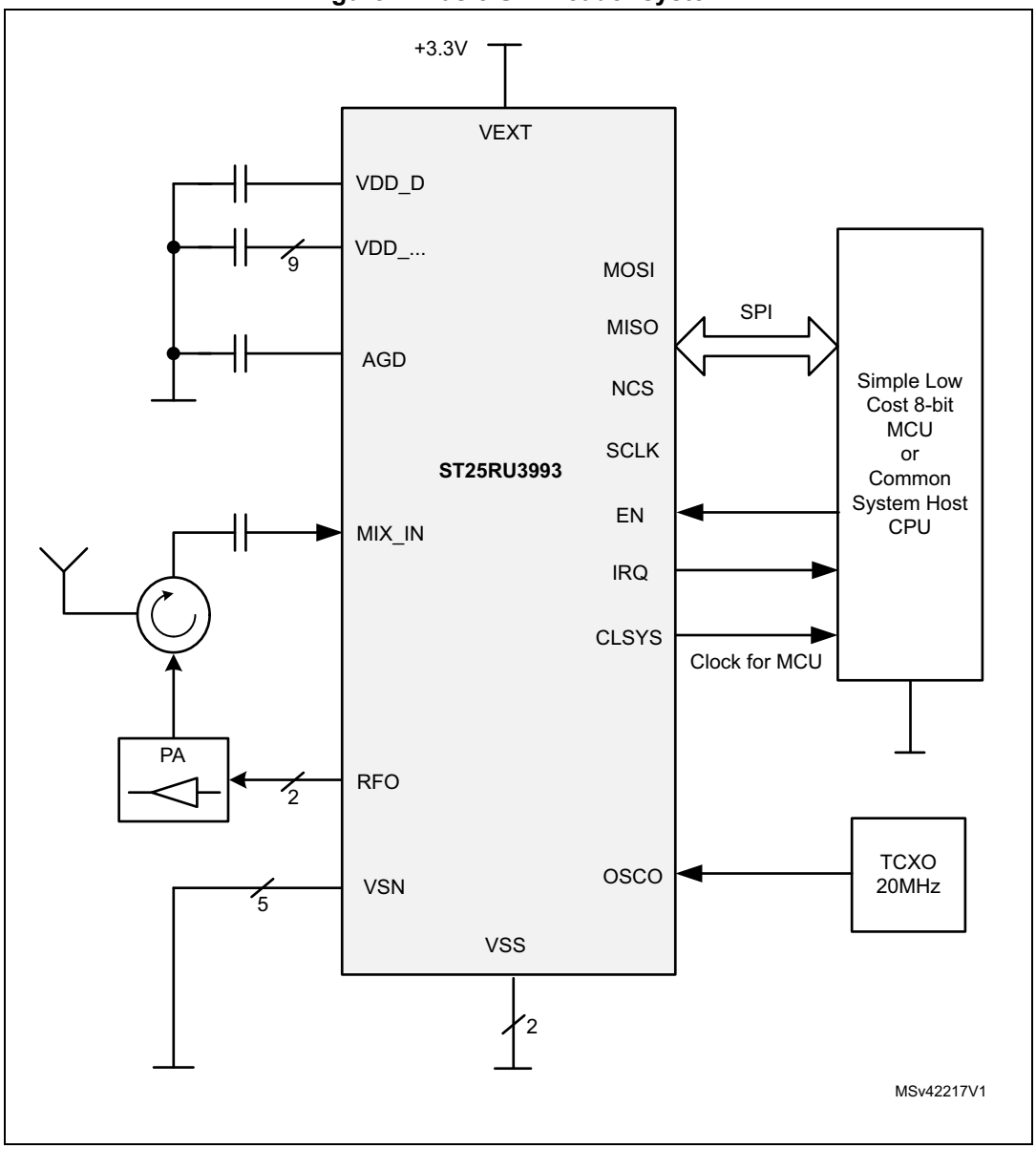


2 Functional overview

The ST25RU3993 UHF reader device is an integrated analog front end and protocol handling system for UHF RFID readers. The chip works on 3.3 V supply voltage and is therefore perfectly suited for low voltage, low-power applications.

It supports operation on DRM link frequencies used in ETSI and FCC regions (see *Section 2.9.4: Rx filter* for supported link modes). It complies with EPC Class1 Gen2 protocol (ISO 18000-6C) in normal mode and ISO 18000-6A/B in direct mode.

Figure 2. Basic UHF reader system



The RFID reader device features complete analog and digital functionality for the reader operation, including transmitter and receiver section with full EPC Class1 Gen2 (ISO18000-6C) digital protocol support.

The reader is enabled by setting the EN pin of the device to a positive logic level. A four-wire serial peripheral interface (SPI) is used for communication between the host system (MCU) and the reader device. The MCU is notified to service an IRQ by a logic high level on the IRQ pin. The device configuration and fine tuning of the reader performance is achieved through direct access to all control registers. The baseband data is transferred via a dual 24-byte FIFO buffer register to and from the reader device. The transmission system comprises a parallel/serial data conversion, low level data encoding and automatic generation of FrameSync, Preamble, and cyclic redundancy check (CRC).

Two transmitter output ports are available:

- One differential low-power, high linearity 0 dBm output that drives its power into a single ended 50 Ω load.
- One differential high power output that is amplified by the internal PA. The high power output delivers up to 20 dBm and requires a single ended 50 Ω load.

Both outputs are capable of amplitude shift keying (ASK) or phase reversal amplitude shift keying (PR-ASK) shaped modulation. The integrated supply voltage regulators ensure supply ripple rejection of the complete reader system.

The receiver system ensures both AM and PM demodulation, and comprises a proprietary automatic gain control system.

Selectable gain stages and signal bandwidth cover a wide range of input link frequencies and bit rate options. The signal strength of AM and PM modulation is measured and can be accessed through the *RSSI display register* (2Bh). The receiver output is selectable between digitized sub-carrier signals and internal sub-carrier decoder output. The internal decoder output delivers a bit stream and a data clock.

The receiver system comprises a framing system for the baseband data. It performs a CRC check and organizes the data in bytes that are then accessible to the host system through a 24-byte FIFO register.

To minimize the bill of materials (BOM), it also comprises an on-board PLL section with an integrated voltage controlled oscillator (VCO), partially integrated loop filter, supply section, ADC section and host interface section. To cover a wide range of applications the reader device has several possible configurations. The register section configures the operation and the behavior of all blocks.

The device needs to be supplied via VEXT and VEXT_PA pins. The power supply connection is described in *Power supply*. At device power-up, the configuration registers are preset with their default values. The default values are described in the configuration register tables along with all option bits. The communication between the reader device and the transponder(s) follows the reader-talk-first method. After device power-up and register configuration, the host system (MCU) can start a communication with the transponder by turning the RF field ON and transmitting the first protocol command. Transmission and reception is possible in two modes:

- Normal mode
- Direct mode

In normal mode the base band data is transferred through the double FIFO buffer and all protocol data processing is done internally. In the direct mode the encoders and decoders are bypassed for transmission and reception and the data processing must be done by the MCU. In the direct mode the MCU can service the analog front-end in real time.

2.1 Power supply

The device has its own power supply system to minimize the influence of external power supply noise and interferences and improves decoupling between different internal building blocks.

The positive supply pins are VEXT and VEXT_PA. The negative supply pins are all VSN and VSS pins, including the exposed die pad. For optimal power supply rejection and device performance the supply voltage should be at least 3.3 V. A power supply voltage above 3.0 V enables operation with reduced power supply rejection. With lower supply voltages (down to 2.7 V) reduced device performance should be expected.

2.1.1 Main regulators

A set of adjustable regulators is used to supply the different internal building blocks of the device. The common input pin for most regulators is VEXT. The regulator outputs are the VDD_A, VDD_LF, VDD_D, VDD_MIX and VDD_B pins. Each regulator output requires shunt capacitors to ground. Typical values are 2.2 µF and 100 pF, ceramic capacitors of (at least) X5R class are recommended. VDD_LFI and VDD_TXPAB are supply input pins and should be connected to VDD_MIX.

The regulated output voltage can be set in the range from 2.7 V up to 3.4 V in 0.1 V steps using option bits rvs[2:0] in the *Regulator and PA bias register* (0Bh). It is also possible to adjust the regulated output voltage automatically to approximately 300 mV below the supply voltage V_{EXT} using the direct command Automatic Power Supply Level Setting (A2h).

2.1.2 Internal PA supply regulator

The internal power amplifier has a dedicated voltage regulator. The input pin is VEXT_PA, output is VDD_PA. The regulator has an internal compensation circuit that requires a small external capacitance on VDD_PA (typical 1 nF). Operation of this voltage regulator is allowed only in a loaded condition.

The regulated output voltage can be set in the range from 2.7 V up to 3.4 V in 0.1 V steps using option bits rvs_rf[2:0] in the *Regulator and PA bias register* (0Bh). It is also possible to adjust the regulated output voltage automatically to approximately 300 mV below the supply voltage V_{EXT} using the direct command Automatic Power Supply Level Setting (A2h).

As the rvs_rf[2:0] settings and the automatic power supply level adjustment generally can have different values, the system is designed to automatically select the lowest voltage level for the VDD_PA.

2.1.3 Periphery communication supply

The logic levels used for communication with the host system (MCU) can vary within a wide voltage range. The VDD_IO input pin is used to define these logic levels between 1.65 V and 5.5 V. It is recommended to connect VDD_IO to the host system power supply in order to avoid any voltage mismatch.

2.1.4 Automatic power supply level setting

The power supply section comprises a system that automatically adjusts the regulators to approximately 300 mV below the V_{EXT} supply voltage, required to achieve good power supply rejection in the regulators.

The direct command Automatic Power Supply Level Setting (A2h) activates the system. To switch back to manual power supply level adjustment, the direct command Manual Power Supply Level Setting (A3h) should be sent.

Before the direct command (A2h) is issued it is necessary to set and lock the PLL within the allowed target frequency (840 MHz to 960 MHz).

At the beginning of the automatic adjustment, the device sets the regulators to 3.4 V and enables the RF field to simulate a normal power supply load. During the procedure the device decreases the regulated voltage in 100 mV steps, each 300 µs long. The lowest voltage that the regulator can set is 2.7 V.

The procedure stops when the difference between the V_{EXT} and the regulated voltages is at least 300 mV, or reaches the last step. The device then disables the RF field and sends an IRQ request with Irq_cmd bit (register 36h) set to high.

2.1.5 Power modes

The device has four main power modes:

- Power down mode
- Standby mode
- Normal mode – RF OFF
- Normal mode – RF ON

Power down mode

By driving the EN pin to a logic low level the device enters the power-down mode. In this mode, the circuit is disabled.

Standby mode

The Standby mode is entered from normal mode by setting the option bit stby high (register 00h). In the Standby mode the voltage regulators, the reference voltage system and the crystal oscillator are operating in a low-power mode. The PLL, transmitter output stages and the receivers are switched off. All register settings are maintained while switching between Standby and Normal mode. The bias and reference voltages after stby = 0 typically stabilize within 12 ms. By then the device is ready to switch ON the RF field and start data transmission.

Normal mode - RF OFF

Setting the EN pin to a logic high level activates the normal mode. In this mode the following internal blocks are enabled:

- All supply regulators
- Reference voltage and bias system
- Crystal oscillator
- RF oscillator and PLL

When the EN pin is set to a logic high level the bias and reference voltages become stable after 12 ms (typical value). From then on the device is ready for interaction with the internal registers. After the reference frequency source stabilizes and the CLSYS clock becomes active, the device is ready to operate according to the configuration of its internal registers. If the crystal oscillator is used, the time the crystal stabilizes depends on the crystal type used. A typical time is 1.5 ms to 3 ms. By reading the *AGC and internal status display*

register (2Ah), the MCU can check the crystal status. The status bit osc_ok = 1 in this register indicates that the crystal oscillation is stable and that the device is ready to operate.

If a continuously running TCXO is used the settling of the internal clock is faster, as only the OSCO pin DC level needs to be set. The same test with the osc_ok status bit as described above can be used.

After additional 500 ms (typ.) the device is ready to switch on the RF field and the transmission of inventory commands for transponder communication.

Normal mode - RF ON

By setting the rf_on option bit in the *Device status control register* (00h) the device immediately starts with the field ramp-up. The ramp-up time and shape are defined by trfon[1:0] and lin_mod option bits in the *Modulator control register 3* (15h). When the RF field ramp-up is finished the rf_ok status bit (register 2Ah) is set to high. In addition an IRQ is generated, which is indicated by Irq_ana status bit set to high (register 38h).

Setting the option bit rf_on to low starts the field ramp-down. The RF field is decreased according to trfon[1:0] and lin_mod bits (register 15h). When this step is completed, the rf_ok status bit in *AGC and internal status display register* (2Ah) is set to low, and an IRQ is sent with the Irq_ana status bit high.

Table 1 summarizes the available power modes and the transitions times between them.

Table 1. Power modes overview

Mode	EN pin	Stby option bit	rf_on option bit	Current consumption	Time to enter the mode	Time from mode to active RF field
Power down	L	-	-	1 µA	Immediately from normal mode	12 - 17 ms (Crystal or TCXO start + bias start)
Standby	H	H	L	3 mA	Immediately from normal mode	12 - 17 ms (Crystal or TCXO start + bias start)
Normal	H	L	L	24 mA	12 - 17 ms (Crystal or TCXO start + bias start)	12.5 µs (Field ramp-up)
Normal with RF field on	H	L	H	75 mA	12.5 µs (Field ramp-up)	NA

2.2 Host communication

A standard 4-wire serial interface (SPI) together with an interrupt request line (IRQ pin) is used to communicate with the device. An additional line (CLSYS) can be used as a system clock source for the MCU.

Table 2. Serial data interface (SPI interface) signal lines

Name	SIgnal	Signal level	Description
NCS	Digital input	CMOS	SPI enable (active low)
SCLK	Digital input	CMOS	Serial clock
MOSI	Digital input	CMOS	Serial data input

Table 2. Serial data interface (SPI interface) signal lines (continued)

Name	SIgnal	Signal level	Description
MISO	Digital output with tri-state	CMOS	Serial data output
IRQ	Digital output	CMOS	Interrupt request output
CLSYS	Digital output	CMOS	MCU clock output

By setting the NCS pin low the SPI interface is enabled. While NCS is high the SPI interface is deactivated. It is recommended to keep signal NCS high whenever the SPI interface is not used. MOSI is sampled at the falling edge of SCLK. The SPI communication is done in bytes. The first two bits of the first byte on the MOSI line (after NCS high-to-low) define the SPI operation mode. MSB bit is always transmitted first (valid for address and data).

The read and write modes support address auto incrementing for multi byte transfers. Only the first address needs to be sent and internally the address is incremented for consecutive reads or writes.

The MISO output is usually in tri-state and it is only driven when output data are available. This allows to short-circuit the MOSI and the MISO lines externally to create a bi-directional signal (see *Figure 3*).

During the time the MISO output is in high impedance it is possible to activate a 50 kΩ pull-down resistor by setting option bits miso_pd1 and miso_pd2 in *Miscellaneous register 1* (0Dh).

Figure 3 shows the possible SPI interconnection options.

Figure 3. Possible SPI configurations

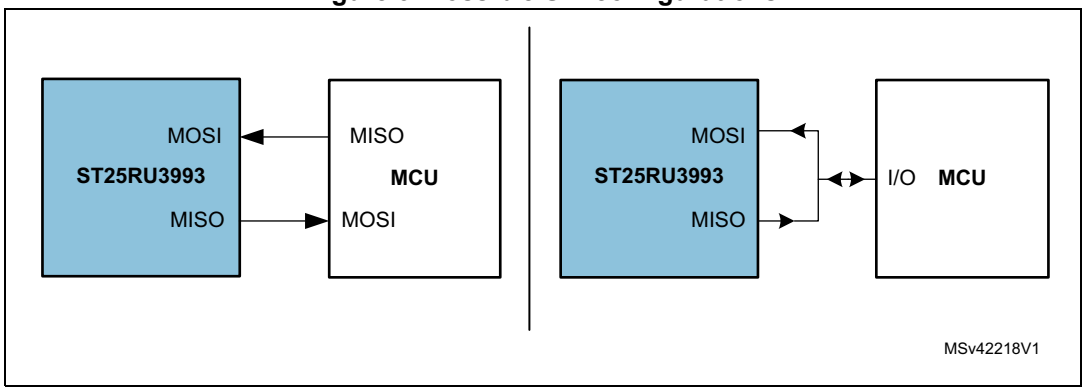


Table 3. SPI operation modes

Command type	Mode pattern (MSB to LSB)								Mode related data
	Mode		Register address / command ID						
	M1	M2	X5	X4	X3	X2	X1	X0	
Write	0	0	A5	A4	A3	A2	A1	A0	Data byte (or more bytes if of autoincrementing)
Read	0	1	A5	A4	A3	A2	A1	A0	Data byte (or more bytes if of autoincrementing)
Direct command	1	0	C5	C4	C3	C2	C1	C0	-
RFU	1	1	x	x	x	x	x	x	-

2.2.1 Writing to registers

Figure 4 show typical SPI Write communication examples for a single byte and for multiple bytes using address auto-incrementing. Following the SPI operation mode bits (M1 and M2) the address bits (A5: A1) of the target register are sent. Then one or more data bytes are sent depending on using auto-incrementing or not. The communication is terminated by putting NCS back to high. If this happens before a packet of 8 bits (one byte) is sent, writing to this register is not performed. If the register at the defined address does not exist or is a read only register the write command does not succeed either.

Figure 4 shows an example of a SPI write command signaling for a single byte.

Figure 4. Writing a single byte

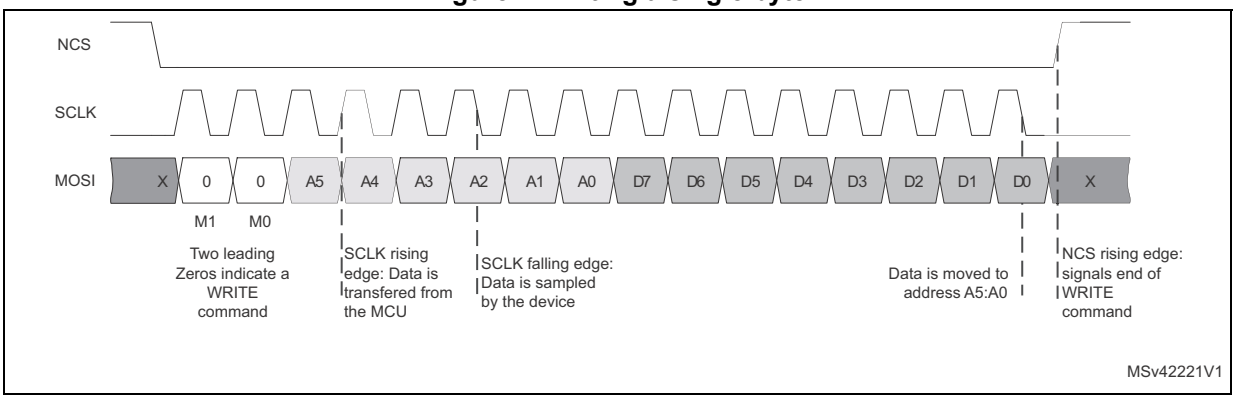
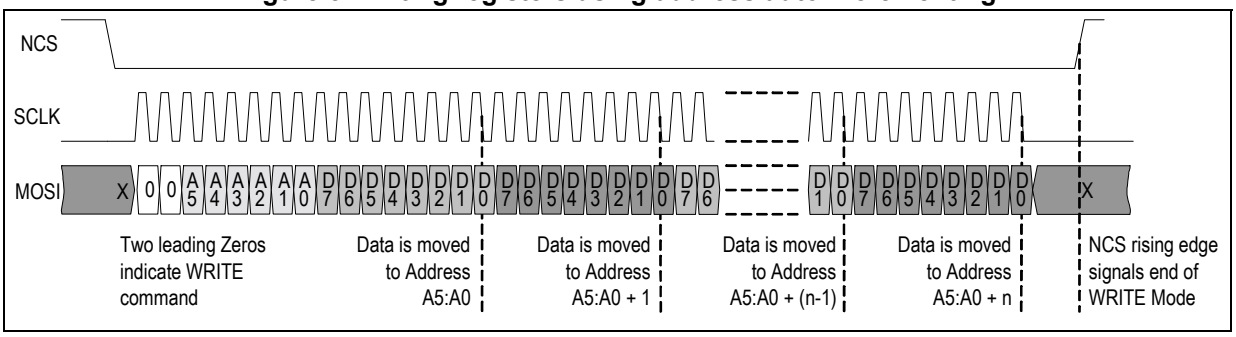


Figure 5 an example of a SPI write command signaling for multiple bytes.

Figure 5. Writing registers using address auto-incrementing



2.2.2 Reading from registers

After the SPI operation mode bits (M1 and M0) the target address is sent. Then one or more data bytes are transferred to the MISO output. MOSI is sampled at the falling edge of SCLK. Data to be read from the internal registers are transferred to the MISO pin on rising edge of SCLK and should be sampled by the MCU on the falling edge. If the register address does not exist all 0 data are sent to MISO.

Figure 6 shows an example for a typical SPI Read command for a single byte.

Figure 6. Reading a single byte

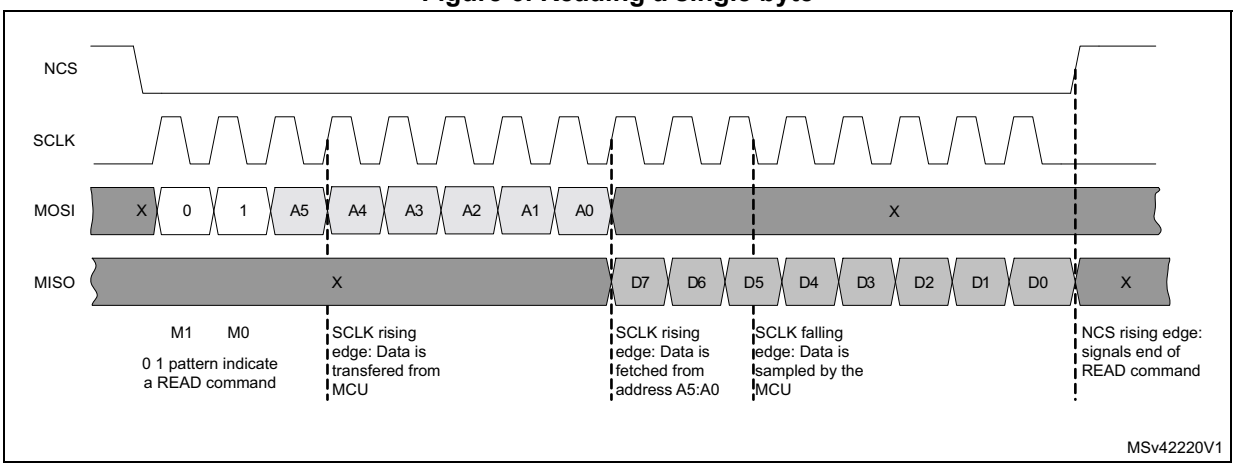
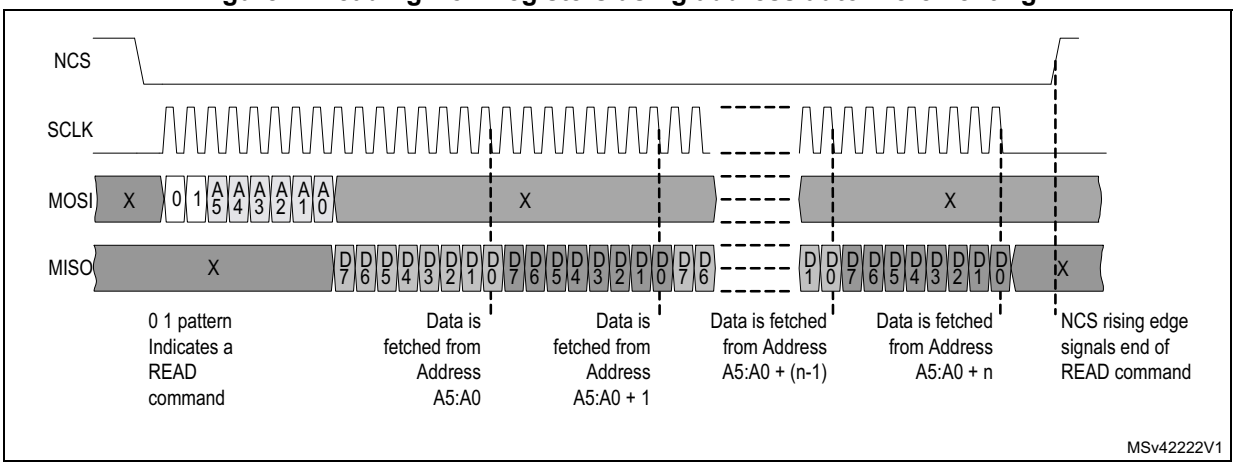


Figure 7 shows an example of an SPI read command signaling for multiple bytes.

Figure 7. Reading from registers using address auto-incrementing



2.2.3 Direct commands

Direct commands have no parameters, so only a single byte needs to be sent. The only exception is the Query command, which requires two parameter bytes (stored in FIFO) following the command byte. SPI operation mode bits M1 = 1 and M0 = 0 define a direct command. The following six bits define the direct command ID. The direct command is executed at the last falling edge of SCLK. Some direct commands are executed immediately while others start a process with certain duration (calibration, measurements…).

Caution: During execution of such commands it is not recommended to start another activity on the SPI interface.

After the execution of a direct command an IRQ request with Irq_cmd bit high (register 38h) is sent.

Table 4. List of direct commands

Code (HEX)	Command	Direct execution
80h	Idle	Yes
81h	Direct Mode	Yes
83h	Soft Init	Yes
84h	Hop to Main Frequency	Yes
85h	Hop to Auxiliary Frequency	Yes
87h	Trigger AD Conversion	No
88h	Trigger Rx Filter Calibration	No
89h	Decrease Rx Filter Calibration Data	Yes
8Ah	Increase Rx Filter Calibration Data	Yes
90h	Transmission with CRC	Yes
91h	Transmission with CRC Expecting Header Bit	Yes
92h	Transmission without CRC	Yes
96h	Block Rx	Yes
97h	Enable Rx	Yes
98h	Query	Yes
99h	QueryRep	Yes
9Ah	QueryAdjustUp	Yes
9Bh	QueryAdjustNic	Yes
9Ch	QueryAdjustDown	Yes
9Dh	ACK	Yes
9Fh	ReqRN	Yes
A2h	Automatic power supply level setting	No
A3h	Manual power supply level setting	Yes
A4h	Automatic VCO range selection	No
A5h	Manual VCO range selection	Yes
A6h	AGL On	Yes
A7h	AGL Off	Yes
A8h	Store RSSI	Yes
A9h	Clear RSSI	Yes
AAh	Interrogator anti-collision support enable	Yes
ABh	Interrogator anti-collision support disable	Yes

Direct command description

The direct commands supported by the ST25RU3993 are detailed below. Values in parentheses show the related command byte.

- **Direct mode** (81h): device enters the direct mode.
- **Soft init** (83h): this command resets the configuration registers to their default values and terminates all functions that were triggered before.
- **Hop to main frequency** (84h): this command forces the PLL to use the frequency defined in the PLL Main Registers 1 - 3. The PLL main registers are used per default.
- **Hop to auxiliary frequency** (85h): This command forces the PLL to use the frequency setting defined in the *PLL auxiliary register 1*, *PLL auxiliary register 2* and *PLL auxiliary register 3*.
- **Trigger A/D conversion** (87h): this command triggers the analog to digital conversion using the internal 8-bit A/D converter. For further information, refer to the A/D Converter description.
- **Trigger Rx filter calibration** (88h): this command triggers the Rx filter calibration procedure. For further information, refer to the Rx filter calibration description.
- **Decrease Rx filter calibration data** (89h), Increase Rx filter calibration data (8Ah): these commands adjust the automatically acquired Rx filter calibration data. For further information, refer to the Rx filter calibration description.
- **Transmission with CRC** (90h): transmission commands are used to transmit data from the reader to transponders. First, the Tx length registers (3Dh, 3Eh) need to be set with the number of complete bytes for transmission, including the number of bits for the incomplete byte. Then transmission data can be loaded in the FIFO register (3Fh). Transmission starts when the first byte is loaded. CRC-16 is included in the transmitted sequence.
  The optimal way to load all transmission data is to use the Continuous Write mode, starting with the address 3Dh.
  Example Using Address Auto-Incrementing:
  SPI data (MOSI): 90h - 3Dh - 00h - 30h - AAh - BBh - CCh operates as follows:
  - 90h:Transmission with CRC
  - Write 00h to 3Dh
  - Write 30h to 3Eh (three bytes are going to be transmitted)
  - Write AAh, BBh, CCh to address 3Fh (FIFO data which will be transmitted).
- **Transmission with CRC expecting header bit** (91h): same as the previous command, but it also informs Rx decoding logic that an header bit is expected in the response.
- **Transmission without CRC** (92h): same as direct command ‘Transmission with CRC’, but the CRC part is omitted.
- **Block Rx** (96h): the Block Rx command deactivates the digital part of receiver (bit decoder and framer). Turning OFF the receiver is useful if the system operates in a noisy environment, causing a constant switching of the sub-carrier input of the Rx digital part. The active receiver will try to detect a Preamble and if the noise pattern matches the expected signal pattern, an interrupt is generated. A constant flow of interrupt requests can be a problem for the MCU, Such situation can be avoided by deactivating the receive decoder using the Block RX command. The receiver is automatically reactivated at the end of any data transmission after the Rx wait time elapses. To set the Rx wait time refer to the Rx Wait Timer section. A second possibility to stop Block Rx is to send the Enable Rx (97h) command.
- **Enable Rx** (97h): this command prepares analog and digital part of the receiver for reception. This command should be sent to trigger the reception manually. This

command should not be sent if reception is automatically triggered by a data transmission command.

- **Query** (98h): the Query command issues the EPC Query, which starts the inventory round. The Query command requires additional two data bytes which should be written to the FIFO (3Fh):
  The two bytes in the FIFO should contain: “00”, DR, M, TRext, Sel, Session, Target, Q
  Since this adds-up to 15 applicable bits, the LSB bit is disregarded.
  The transmitter in the end sends:
  – Preamble
  – Command ID
  – Tx data (two bytes from FIFO)
  – CRC-5.

  The received RN16 is stored in the internal RN16 register for further communication steps (ACK, ReqRN). RN16 is also stored in the FIFO.
- **QueryRep** (99h): the QueryRep command issues the EPC Gen2 QueryRep command followed by two session bits. The session bits are taken from *Tx setting register* (3Ch). The received RN16 is stored in the internal RN16 register for further communications (ACK, ReqRN). RN16 is also accessible in the FIFO.
- **QueryAdjustUp** (9Ah): the QueryAdjustUp direct command issues the EPC Gen2 QueryAdjust command followed by two session bits and ‘up’ parameter (increasing the number of available slots). The session bits are taken from *Tx setting register* (3Ch). The received RN16 is stored in the internal RN16 register for further communications (ACK, ReqRN). RN16 is also accessible in the FIFO.
- **QueryAdjustNic** (9Bh): the QueryAdjustNic command issues the EPC Gen2 QueryAdjust command followed by two session bits and ‘no change’ parameter. The session bits are taken from *Tx setting register* (3Ch). The received RN16 is stored in the internal RN16 register for further communications (ACK, ReqRN). RN16 is also accessible in the FIFO.
- **QueryAdjustDown** (9Ch): the QueryAdjustUp command issues the EPC Gen2 QueryAdjust followed by two session bits and ‘down’ parameter (decreasing the number of available slots). The session bits are taken from *Tx setting register*(3Ch). The received RN16 is stored in the internal RN16 register for further communications (ACK, ReqRN). RN16 is also accessible in the FIFO.
- **ACK** (9Dh): the ACK command issues the EPC ACK followed by RN16 stored in the internal RN16 register during last successful Query command.
- **NAK** (9Eh): the NAK command issues the EPC Gen2 NAK command to tags.
- **ReqRN** (9Fh): the ReqRN command issues the EPC Request RN to the tag. The last received RN is used as a parameter and the received new RN16 (handle) is stored in the internal RN16 register for further communications (ACK, ReqRN). New RN16 is also stored in the FIFO.
- **Automatic power supply level setting** (A2h), **manual power supply level setting** (A3h): these commands trigger the automatic adjustment of the on-board voltage

regulators, and switch back to the manual selection. See Periphery Communication Supply description for more details.

- **Automatic VCO range selection** (A4h), **manual VCO range selection** (A5h): these commands trigger the automatic VCO range selection and switch back to manual VCO range selection. See PLL and VCO description for more details.
- **AGL on** (A6h), **AGL off** (A7h): these commands trigger and disable the AGL action. See AGL description for more details.
- **Store RSSI** (A8h), **Clear RSSI** (A9h): these commands store and clear the received signal strength indicator (RSSI) data that can be used for IQ decision circuitry. See IQ Selection description for more details.
- **Interrogator anti-collision support enable** (AAh), **interrogator anti-collision support disable** (ABh): these commands enable or disable the interrogator anti-collision support defined in ISO 29143.

Direct command chaining

Direct commands with immediate execution can be followed by another SPI commands like Read or Write without deactivating the NCS signal in between.

2.2.4 SPI interface timing

Table 5. SPI timing parameters

Symbol	Parameter	Note/Condition	Min	Typ	Max	Unit
General (VDD_IO > 3 V, CLOAD < 50 pF, hs_output = 1)						
BR_{SPI}	Bit rate	-	-	-	5	Mbps
t_{SCLKH}	Clock high time	-	70	-	-	ns
t_{SCLKL}	Clock low time	-	70	-	-	ns
t_{NCSL}	NCS setup time	Time between NCS high-low transition to first SCLK high transition	10	-	-	ns
t_{DIS}	Data-in setup time	-	10	-	-	ns
t_{DIH}	Data-in hold time	-	10	-	-	ns
t_{NCSH}	NCS hold time Read / Write	Time between last SCLK falling edge and NCS low-high transition after a Read or Write	10	-	-	ns
t_{NCSH}	NCS hold time direct command	Time between last SCLK falling edge and NCS low-high transition after a direct command	70	-	-	ns

Table 5. SPI timing parameters (continued)

Symbol	Parameter	Note/Condition	Min	Typ	Max	Unit
Read timing						
t_{DOD}	Data out delay	$V_{DD\_IO} \geq 3$ V, $C_{LOAD} = 50$ pF, hs_output = 1	-	30	-	ns
t_{DOD}	Data out delay	$V_{DD\_IO} \geq 1.65$ V, $C_{LOAD} = 50$ pF, hs_output = 1	-	60	-	ns
t_{DOD}	Data out delay	$V_{DD\_IO} \geq 3$ V, $C_{LOAD} = 50$ pF, hs_output = 0	-	90	-	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the MISO line	-	40	-	ns

Figure 8 shows the corresponding timing waveforms and parameters for the SPI write command.

Figure 8. SPI Write timing

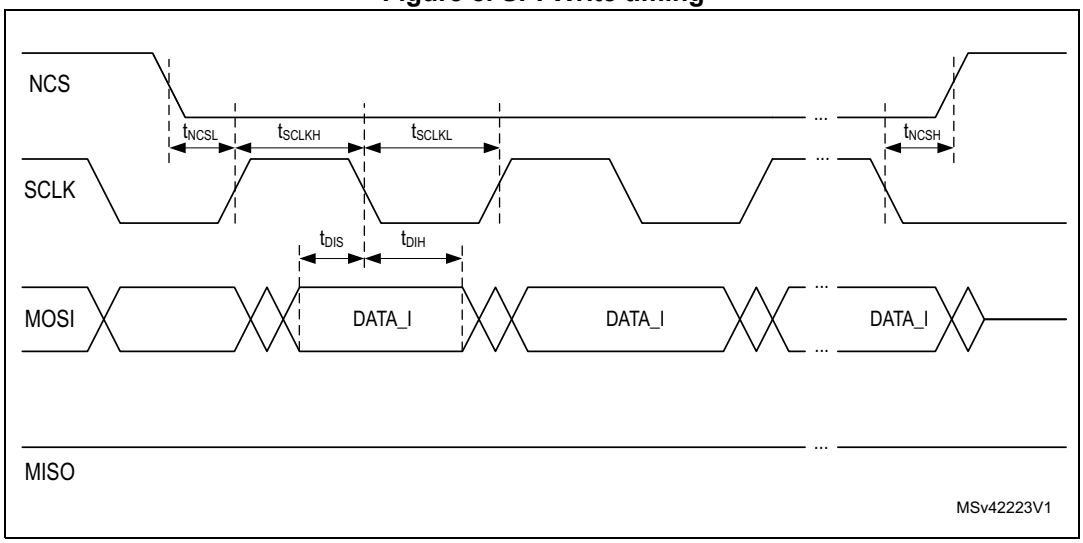
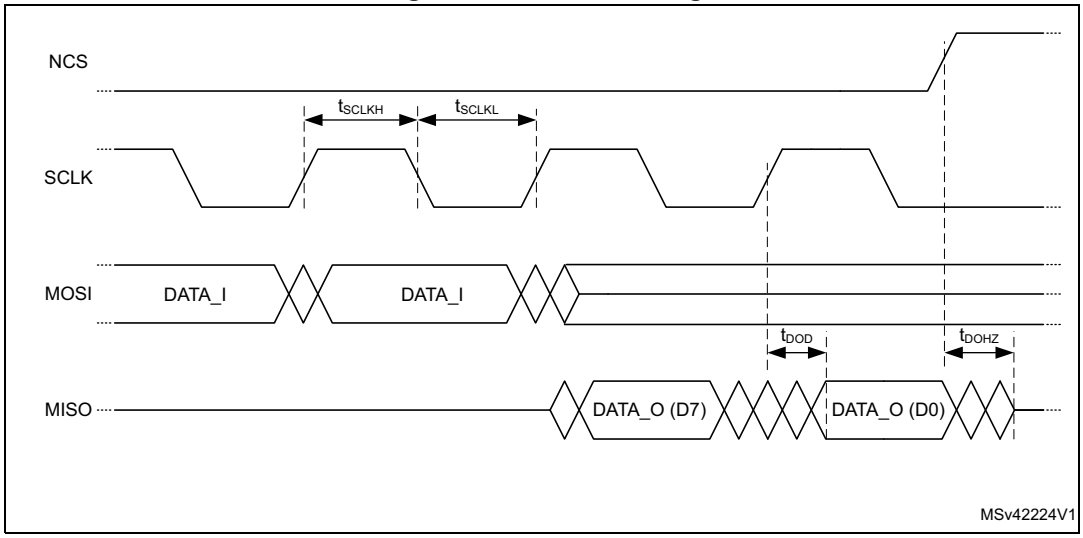


Figure 9 shows the corresponding timing waveforms and parameters for the SPI read command.

Figure 9. SPI Read timing



2.2.5 CLSYS output

The CLSYS output is intended to be used as a MCU clock source. Available frequencies are:

- 4 MHz
- 5 MHz
- 10 MHz
- 20 MHz

The CLSYS frequency is defined by clsys[2:0] option bits in the *Miscellaneous register 2* (0Eh).

2.2.6 IO signal level and output characteristics

The logic high level for the host communication and CLSYS is defined by the supply voltage connected to VDD_IO pin. The logic high level can be in the range between 1.65 V and 5.5 V. VDD_IO should be connected to the host system periphery supply voltage to ensure matching communication levels.

The digital outputs are by default configured for high-speed operation. A 5 MHz SPI clock is possible with a 50 pF capacitive load on the MISO and IRQ outputs and a minimum VDD_IO supply voltage of 3 V. A 3 MHz SPI clock is possible with a 50 pF load and a minimum V_{DD_IO} supply voltage of 1.65V.

To decrease the harmonic content of the digital output signals, it is possible to configure the device outputs to provide weak, sloped output signals by setting the hs_output option bit in the *Miscellaneous register 1* (0Dh) to low. In this configuration the possibility of interferences by the host system communication with other internal building blocks of the device is mitigated as well. Using this option a 2 MHz SPI clock is possible with maximum 50 pF capacitive load on MISO and IRQ and at least a V_{DD_IO} supply voltage of 3 V.

It is also possible to define open drain N-MOS outputs by setting the option bit open_dr high (register 0Dh). This option reduces the harmonic content on the MISO, IRQ, and CLSYS signals further. It also decreases cross-coupling effects that could interfere with operation of other blocks of the device.

2.2.7 OAD, OAD2 outputs

The OAD and OAD2 outputs are analog and digital test outputs. When used as analog outputs, the received sub-carrier signals or mixer analog DC output levels are multiplexed at these pins. The signal is centered to AGD level. When used as digital output, the levels are configured with VDD_IO. The OAD pins can be configured as high speed outputs by setting the option bit hs_oad in the *Miscellaneous register 1* (0Dh). During normal operation it is not recommended to use hs_oad, as higher harmonic content can increase the crosstalk to sensitive pins of the device.

2.3 PLL and VCO section

The PLL section comprises a voltage controlled oscillator, a pre-scaler, main and reference dividers, a phase-frequency detector, a charge pump and a loop filter.

Figure 10 shows a detailed block diagram of the PLL and VCO section of the ST25RU3993 device.

Figure 10. PLL and VCO section