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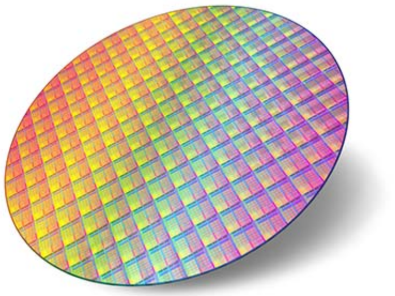
ST25TV16K
ST25TV64K

# NFC Type 5 / RFID tag IC with 16-Kbit or 64-Kbit EEPROM and protection

**Datasheet - production data**



Bumped and sawn wafer

## Features

### Contactless interface

- Based on ISO/IEC 15693
- NFC Forum Type 5 tag certified by the NFC Forum
- Supports all ISO/IEC 15693 modulations, coding, subcarrier modes and data rates
- Custom Fast read access up to 53 Kbit/s
- Single and multiple block reads (Same for Extended commands)
- Single and multiple block writes (Same for Extended commands) (up to 4)
- Internal tuning capacitance: 28.5 pF
- Kill capability for privacy protection

### Memory

- 16 KB or 64 Kbits of EEPROM
- RF interface accesses blocks of four bytes
- Typical write time: 5 ms for one block
- Data retention: 40 years
- Write cycles endurance:
  – 1 million write cycles at 25 °C
  – 600k write cycles at 85 °C

### Data protection

- User memory: one to four configurable areas, protectable in read and/or write by three 64-bit passwords
- System configuration: protected in write by a 64-bit password

### Temperature range

- From - 40 to 85 °C

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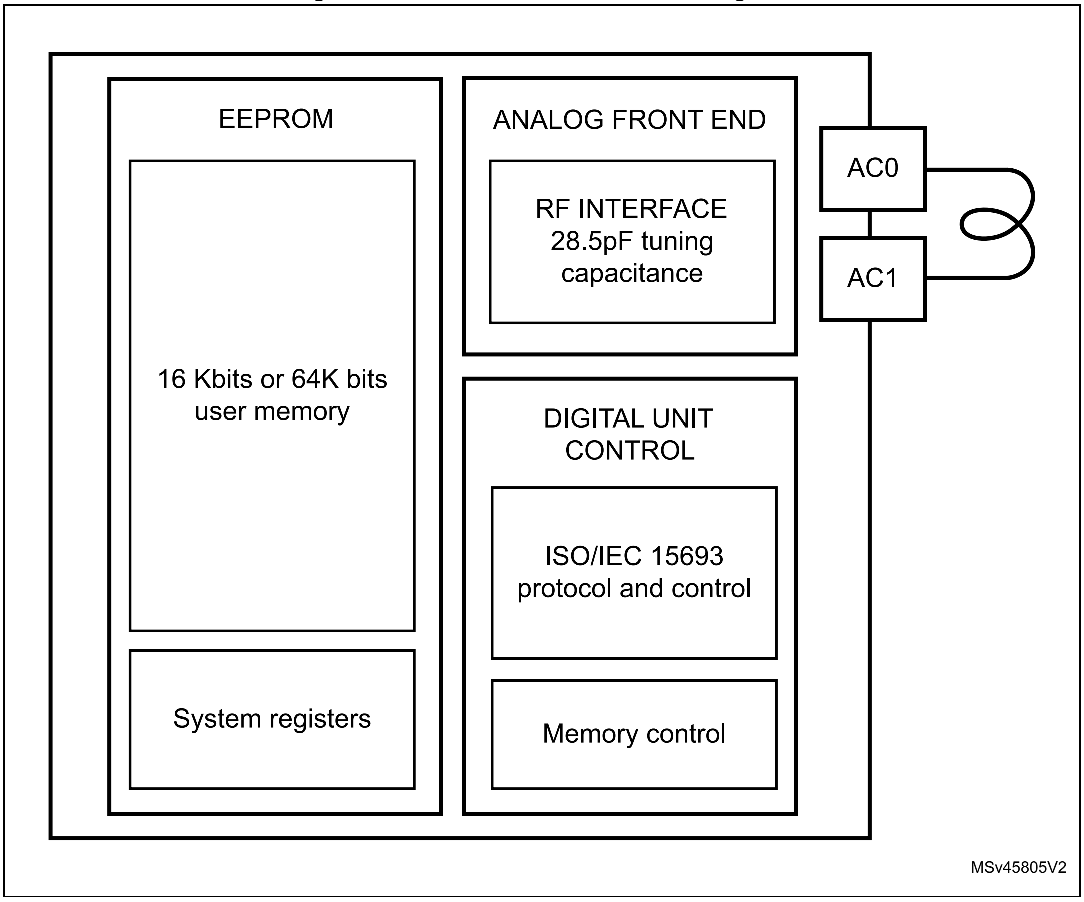
# 1 Description

The ST25TV16K/64K device is a NFC and RFID Tag offering 16 Kbit or 64 Kbit of electrically erasable programmable memory (EEPROM). ST25TV16K/64K acts as a contactless memory accessed through a RF link, following ISO/IEC 15693 or NFC forum type 5 recommendations, and powered by the received carrier electromagnetic wave.

## 1.1 ST25TV16K/64K block diagram

**Figure 1. ST25TV16K/64K block diagram**



# 2 Signal descriptions

## 2.1 Antenna coil (AC0, AC1)

These inputs are used exclusively to connect the ST25TV16K/64K devices to an external coil. It is advised not to connect any other DC or AC path to AC0 or AC1.

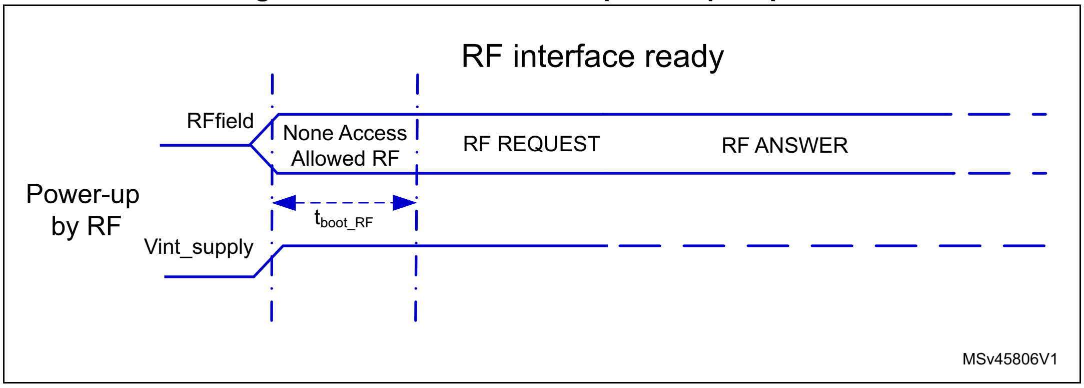
When correctly tuned, the coil is used to power and access the device using the ISO/IEC 15693 and ISO 18000-3 mode 1 protocols.

# 3 Power management

## 3.1 Device set

To ensure a proper boot of the RF circuitry, the RF field must be turned ON without any modulation for a minimum period of time $t_{RF\_ON}$. Before this time, ST25TV16K/64K ignores all received RF commands. (See *Figure 2*).

**Figure 2. ST25TV16K/64K RF power-up sequence**




## 3.2 Device reset

To ensure a proper reset of the RF circuitry, the RF field must be turned off (100% modulation) for a minimum $t_{RF\_OFF}$ period of time.

The RF access can be definitely disabled by setting the appropriate value in the KILL register.

# 4 Memory management

## 4.1 Memory organization overview

The ST25TV16K/64K memory is divided in two main memory areas:

- User memory
- System configuration area

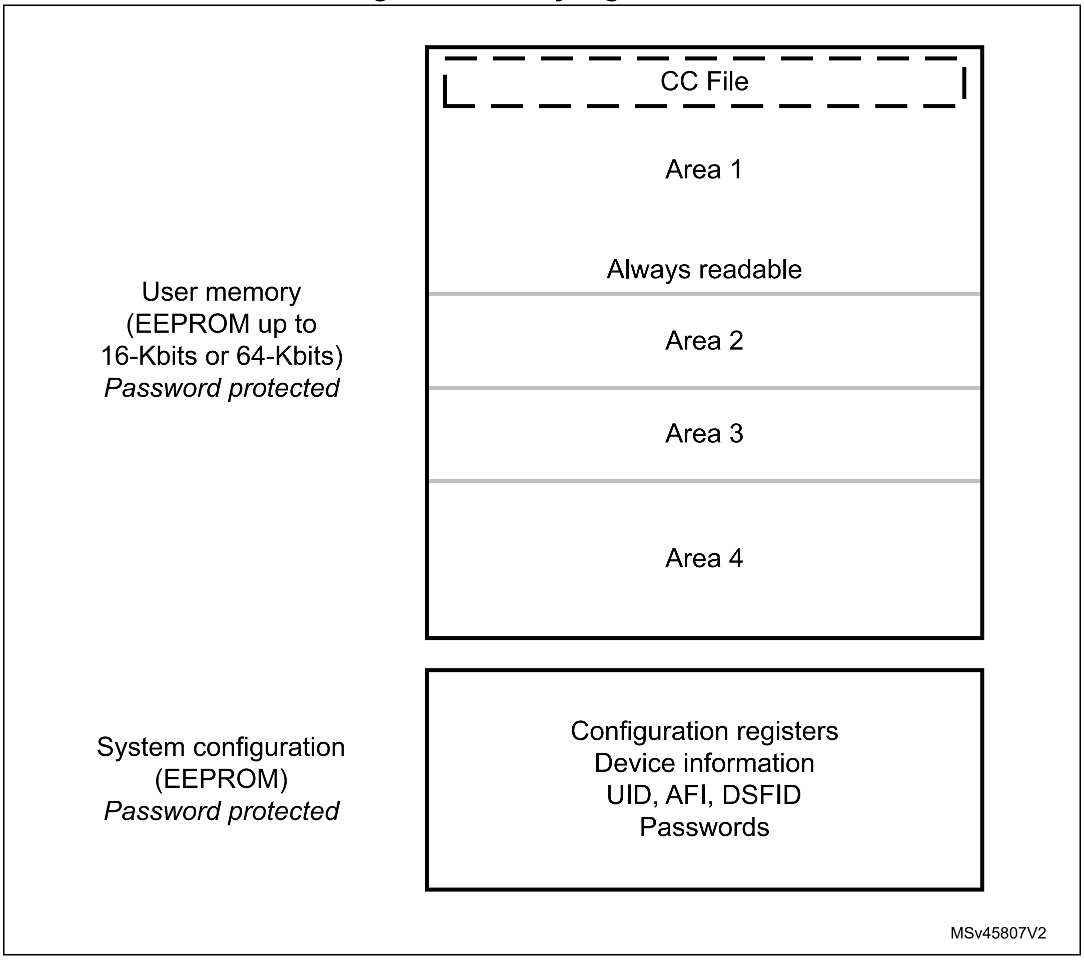
The ST25TV16K/64K user memory can be divided into 4 flexible user areas. Each area can be individually read - and/or - write-protected with one out of three specific 64-bit password.

The ST25TV16K/64K system configuration area contains registers to configure all ST25TV16K/64K features, which can be tuned by user. Its access is protected by a 64 bit configuration password.

This system configuration area also includes read only device information such as IC reference, memory size, as well as a 64-bit block that is used to store the 64-bit unique identifier (UID), and the AFI (default 00h) and DSFID (default 00h) registers. The UID is compliant with the ISO 15693 description, and its value is used during the anticollision sequence (Inventory). The UID value is written by ST on the production line. The AFI register stores the application family identifier. The DSFID register stores the data storage family identifier used in the anticollision algorithm.

The system configuration area includes four additional 64-bit blocks that store three RF user area access passwords and a RF configuration password.

**Figure 3. Memory organization**




## 4.2 User memory

User memory is addressed as blocks of 4 bytes, starting at address 0. RF Extended Read and Write commands can be used to address all ST25TV16K/64K memory blocks. Other read and write commands can only address up to block FFh.

All the blocks of the user memory are initialized to 00h in the factory.

*Table 1: User memory as seen by RF* shows how memory is seen from RF interface.

**Table 1. User memory as seen by RF**

<table>
<tr><th>RF command<br>(block addressing)</th><th colspan="4">User memory</th></tr>
<tr><td rowspan="9">Read Single Block<br>Read Multiple Blocks<br>Fast Read Single Block<br>Fast Read Multiple Blocks<br>Write Single Block<br>Write Multiple Blocks<br>Ext. Read Single Block<br>Ext. Read Multiple Blocks<br>Fast Ext. Read Single Block<br>Fast Ext. Read Multi. Blocks<br>Ext. Write Single Block<br>Ext. Write Multiple Blocks</td><td colspan="4">RF block (00)00h</td></tr>
<tr><td>Byte 0003h</td><td>Byte 0002h</td><td>Byte 0001h</td><td>Byte 0000h</td></tr>
<tr><td colspan="4">RF block (00)01h</td></tr>
<tr><td>Byte 0007h</td><td>Byte 0006h</td><td>Byte 0005h</td><td>Byte 0004h</td></tr>
<tr><td colspan="4">RF block (00)02h</td></tr>
<tr><td>Byte 0011h</td><td>Byte 0010h</td><td>Byte 0009h</td><td>Byte 0008h</td></tr>
<tr><td colspan="4">....</td></tr>
<tr><td colspan="4">RF block (00)FFh(1)</td></tr>
<tr><td>Byte 03FFh</td><td>Byte 03FEh</td><td>Byte 03FDh</td><td>Byte 03FCh</td></tr>
<tr><td rowspan="7">Ext. Read Single Block<br>Ext. Read Multiple Blocks<br>Fast Ext. Read Single Block<br>Fast Ext. Read Multi. Blocks<br>Ext. Write Single Block<br>Ext. Write Multiple Blocks</td><td colspan="4">RF block 0100h</td></tr>
<tr><td>Byte 0403h</td><td>Byte 0402h</td><td>Byte 0401h</td><td>Byte 0400h</td></tr>
<tr><td colspan="4">RF block 01FF(2)</td></tr>
<tr><td>Byte 07FFh</td><td>Byte 07FEh</td><td>Byte 07FDh</td><td>Byte 07FCh</td></tr>
<tr><td colspan="4">....</td></tr>
<tr><td colspan="4">RF block 07FFh</td></tr>
<tr><td>Byte 1FFFh</td><td>Byte 1FFEh</td><td>Byte 1FFDh</td><td>Byte 1FFCh</td></tr>
</table>

1. Last block accessible with Read Single Block, Read Multiple Blocks, Fast Read Single Block, Fast Read Multiple Blocks, Write Single Block and Write Multiple Blocks RF commands.
2. Last block of user memory in ST25TV16K.

### 4.2.1 User memory areas

The user memory can be split into different areas, each one with a distinct access privilege.

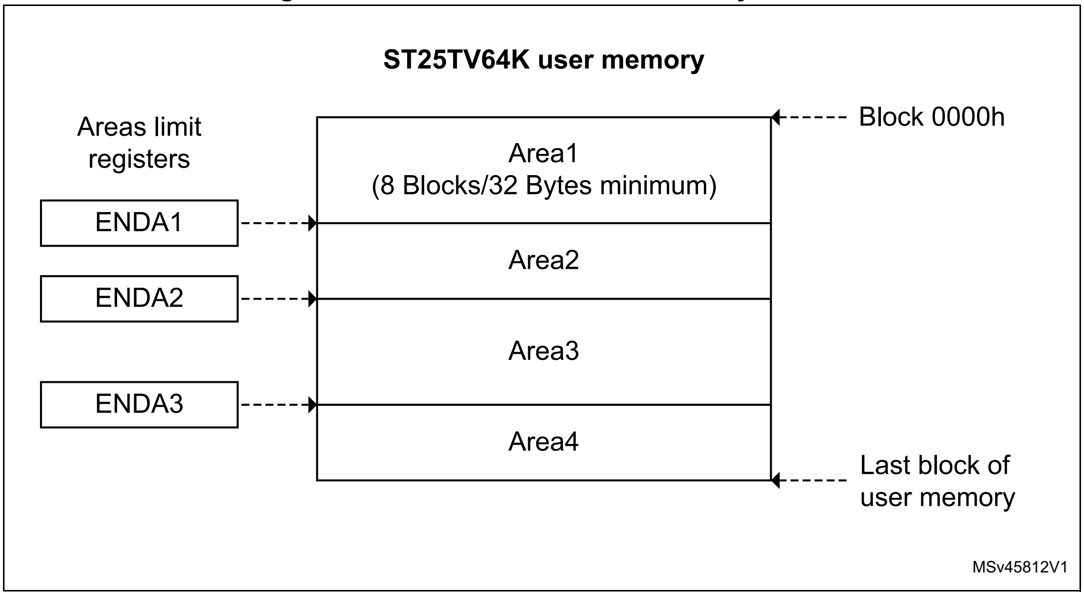
RF read and write commands are legal only within a same zone:

- A multiple read or a multiple write command is not executed and returns the error code 0Fh if addresses cross the area borders.

Each user memory area is defined by its ending block address $ENDA_i$. The starting block address is defined by the end of the preceding area.

There are three $ENDA_i$ registers in the configuration system memory, used to define the end block addresses of Area 1, Area 2 and Area 3. The end of Area 4 is always the last block of memory and is not configurable.

**Figure 4. ST25TV16K/64K user memory areas**




On factory delivery all $ENDA_i$ are set to maximum value, only Area1 exists and includes the full user memory.

A granularity of 8 Blocks (32 Bytes) is offered to code area ending points.

An area's end limit is coded as followed in $ENDA_i$ registers:

- Last block address of area = 8 x $ENDA_i$ + 7 => $ENDA_i$ = int(Last $Area_i$ block address / 8)
- As a consequence, ENDA1 = 0 means size of Area 1 is 8 blocks (32 Bytes).

**Table 2. Maximum user memory block addresses and $ENDA_i$ value**

| Device | Last user memory block address seen by RF | Maximum $ENDA_i$ value |
|---|---|---|
| ST25TV16K | 01FFh | 3Fh |
| ST25TV64K | 07FFh | FFh |

**Table 3. Areas and limit calculation from $ENDA_i$ registers**

| Area | Seen from RF interface |
|---|---|
| Area 1 | Block 0000h<br>…<br>Block (ENDA1*8)+7 |
| Area 2 | Block (ENDA1+1)*8<br>…<br>Block (ENDA2*8)+7 |
| Area 3 | Block (ENDA2+1)*8<br>…<br>Block (ENDA3*8)+7 |
| Area 4 | Block (ENDA3+1)*8<br>…<br>Last memory Block |

Organization of user memory in areas have the following characteristics:

- At least one area exists (Area1), starting at Block address 0000h and finishing at ENDA1, with ENDA1 = ENDA2 = ENDA3 = End of user memory (factory setting).
- Two Areas could be defined by setting ENDA1 < ENDA2 = ENDA3 = End of user memory.
- Three Areas may be defined by setting ENDA1 < ENDA2 < ENDA3 = End of user memory.
- A maximum of four areas may be defined by setting ENDA1 < ENDA2 < ENDA3 < End of user memory.
- Area 1 specificities
  - Start of Area1 is always Block address 0000h.
  - Area1 minimum size is 8 Blocks (32 Bytes) when ENDA1 = 00h.
  - Area1 is always readable.
- The last area always finishes on the last user memory Block address (ENDA4 doesn't exist).
- All areas are contiguous: end of Area(n) + one Block address is always start of Area(n+1).

### Area size programming

RF user must first open the configuration security session to write ENDAi registers.

When programming an ENDAi register, the following rule must be respected:

- ENDAi-1 < ENDAi ≤ ENDAi+1 = FFh (End of user memory).

This means that prior to programming any ENDAi register, its successor (ENDAi+1) must first be programmed to the last Block of memory:

- Successful ENDA3 programming condition: ENDA2 < ENDA3 ≤ End of user memory.
- Successful ENDA2 programming condition: ENDA1 < ENDA2 ≤ ENDA3 = End of user memory.
- Successful ENDA1 programming condition: ENDA1 ≤ ENDA2 = ENDA 3 = End of user memory.

If this rule is not respected, an error 0Fh is returned, and programming is not done.

In order to respect this rule, the following procedure is recommended when programming Areas size (even for changing only one Area size):

1. Ends of Areas 3 and 2 must first be set to the end of memory while respecting the following order:
   a) If ENDA3 ≠ end of user memory, then set ENDA3 = end of memory; else, do not write ENDA3.
   b) If ENDA2 ≠ end of user memory, then set ENDA2 = end of memory; else, do not write ENDA2.
2. Then, desired area limits can be set respecting the following order:
   a) Set new ENDA1 value.
   b) Set new ENDA2 value, with ENDA2 > ENDA1
   c) Set new ENDA3 value, with ENDA3 > ENDA2

Example of successive user memory area setting (for a ST25TV64K):

1. Initial state, 2 Areas are defined:
   a) ENDA1 = 10h (Last block of Area 1: (10h x 8) + 7 = 0087h)
   b) ENDA2 = FFh (Last block of Area 2: (FFh x 8) + 7 = 07FFh)
   c) ENDA3 = FFh (No Area 3)
      – Area 1 from Block 0000h to 0087h (136 Blocks)
      – Area 2 from Block 0088h to 07FFh (1912 Blocks)
      – There is no Area 3.
      – There is no Area 4.
2. Split of user memory in four areas:
   a) ENDA3 is not updated as it is already set to end of memory.
   b) ENDA2 is not updated as it is already set to end of memory.
   c) Set ENDA1 = 3Fh (Last block of Area 1: (3Fh x 8) + 7 = 01FFh)
   d) Set ENDA2 = 5Fh (Last block of Area 1: (5Fh x 8) + 7 = 02FFh)
   e) Set ENDA3 = BFh (Last block of Area 1: (BFh x 8) + 7 = 05FFh)
      – Area1 from Block 0000h to 01FFh (512 Blocks)
      – Area2 from Block 0200h to 02FFh (256 Blocks)
      – Area3 from Block 0300h to 05FFh (768 Blocks)
      – Area4 from Block 0600h to 07FFh (512 Blocks).
3. Return to a split in two equal areas:
   a) Set ENDA3 = FFh
   b) Set ENDA2 = FFh

c) Set ENDA1 = 7Fh (Last block of Area 1: (7Fh x 8) + 7 = 03FFh)

- Area1 from Block 0000h to 03FFh (1024 Blocks)
- Area2 from Block 0400h to 07FFh (1024 Blocks)
- There is no Area3.
- There is no Area4.

Programming ENDA3 to FFh in step 2.a would have resulted in into an error, since rule ENDAi-1 < ENDAi would not been respected (ENDA2 = ENDA3 in that case).

### Registers for user memory area configuration

**Table 4. ENDA1(1)**

| - | Command | Read Configuration (cmd code A0h) @05h<br>Write Configuration (cmd code A1h) @05h | |
|---|---|---|---|
| | Type | R always, W if configuration security session is open and configuration not locked | |
| **Bit** | **Name** | **Function** | **Factory Value** |
| b7-b0 | ENDA1 | End Area 1 = 8*ENDA1+7 when expressed in blocks (RF) | ST25TV16K 3Fh<br>ST25TV64K FFh |

1. Refer to *Table 7: System configuration memory map* for the ENDA1 register.

**Table 5. ENDA2(1)**

| - | Command | Read Configuration (cmd code A0h) @07h<br>Write Configuration (cmd code A1h) @07h | |
|---|---|---|---|
| | Type | R always, W if configuration security session is open and configuration not locked | |
| **Bit** | **Name** | **Function** | **Factory Value** |
| b7-b0 | ENDA2 | End Area 2 = 8 x ENDA2 + 7 when expressed in blocks (RF) | ST25TV16K 3Fh<br>ST25TV64K FFh |

1. Refer to *Table 7: System configuration memory map* for the ENDA2 register.

**Table 6. ENDA3(1)**

| - | Command | Read Configuration (cmd code A0h) @09h<br>Write Configuration (cmd code A1h) @09h | |
|---|---|---|---|
| | Type | R always, W if configuration security session is open and configuration not locked | |
| **Bit** | **Name** | **Function** | **Factory Value** |
| b7-b0 | ENDA3 | End Area 3 = 8 x ENDA3 + 7 when expressed in blocks (RF) | ST25TV16K 3Fh<br>ST25TV64K FFh |

1. Refer to *Table 7: System configuration memory map* for the ENDA3 register.

## 4.3 System configuration area

In addition to EEPROM user memory, ST25TV16K/64K includes a set of registers located in the system configuration area memory (EEPROM nonvolatile registers). Those registers are set during device configuration (i.e.: area extension), or by the application (i.e.: area protection). Registers content is read during the boot sequence and define basic ST25TV16K/64K behavior.

The registers located in the system configuration area can be accessed via dedicated Read Configuration and Write Configuration commands, with a pointer acting as the register address.

The configuration security session must first be open, by presenting a valid configuration password, to grant write access to system configuration registers.

*Table 7* shows the complete map of the system configuration area.

**Table 7. System configuration memory map**

| RF access | | Static Register | |
|---|---|---|---|
| **Address** | **Type** | **Name** | **Function** |
| 03h | RW(1) | *Table 8: KILL* | Tag kill |
| 04h | RW(1) | *Table 9: A1SS* | Area1 access protection |
| 05h | RW(1) | *Table 4: ENDA1* | Area 1 ending point |
| 06h | RW(1) | *Table 10: A2SS* | Area2 access protection |
| 07h | RW(1) | *Table 5: ENDA2* | Area 2 ending point |
| 08h | RW(1) | *Table 11: A3SS* | Area3 access protection |
| 09h | RW(1) | *Table 6: ENDA3* | Area 3 ending point |
| 0Ah | RW(1) | *Table 12: A4SS* | Area4 access protection |
| N/A | R(2)W(3) | *Table 13: LOCK_CCFILE* | Blocks 0 and 1 RF Write protection |
| 0Fh | RW(1) | *Table 14: LOCK_CFG* | Protect Write to system configuration registers |
| N/A | WO(4) | *Table 20: LOCK_DSFID* | DSFID lock status |
| NA | WO(5) | *Table 21: LOCK_AFI* | AFI lock status |
| N/A | RW(4) | *Table 22: DSFID* | DSFID value |
| N/A | RW(5) | *Table 23: AFI* | AFI value |
| N/A | RO | *Table 24: MEM_SIZE* | Memory size value in blocks, 2 bytes |
| | RO | *Table 25: BLK_SIZE* | Block size value in bytes |
| N/A | RO | *Table 26: IC_REF* | IC reference value |
| NA | RO | *Table 27: UID* | Unique identifier, 8 bytes |
| N/A | WO(6) | *Table 15: PWD_0* | Configuration security session password, 8 bytes |
| N/A | WO(6) | *Table 16: PWD_1* | User security session password 1, 8 bytes |
| N/A | WO(6) | *Table 17: PWD_2* | User security session password 2, 8 bytes |
| N/A | WO(6) | *Table 18: PWD_3* | User security session password 3, 8 bytes |

1. Write access is granted if RF configuration security session is open and configuration is not locked (LOCK_CFG register equals to 0).

2. LOCK_CCFILE content is only readable through reading the Block Security Status of blocks 00h and 001h (see *Section 5.2.3: User memory protection*)
3. Write access to bit 0 if Block 00h is not already locked and to bit 1 if Block 01h is not already locked.
4. Write access if DSFID is not locked
5. Write access if AFI is not locked.
6. Write access only if corresponding security session is open.

# 5 ST25TV16K/64K specific features

ST25TV16K/64K offers the data protection feature, both user memory and system configuration, and a kill mode.

Those features can be programmed by setting registers of the ST25TV16K/64K. ST25TV16K/64K can be partially customized using configuration registers located in the EEPROM system area.

These registers are dedicated to:

- Data Memory organization and protection $ENDA_i$, AiSS, LOCK_CCFILE.
- Kill mode, KILL
- The device's structure LOCK_CFG

A set of additional registers allows to identify and customize the product (DSFID, AFI, IC_REF, etc.).

Dedicated commands Read Configuration and Write Configuration must be used to access the configuration registers. Update is only possible when the access right has been granted by presenting the configuration password (PWD_0), and if the system configuration was not previously locked (LOCK_CFG=1).

After any valid write access to the configuration registers, the new configuration is immediately applied.

## 5.1 Kill feature

### 5.1.1 Kill register

**Table 8. KILL(1)**

| RF | Command | Read Configuration (cmd code A0h) @03h<br>Write Configuration (cmd code A1h) @03h | |
|---|---|---|---|
| | Type | R always, W if RF configuration security session is open and configuration not locked | |
| **Bit** | **Name** | **Function** | **Factory Value** |
| b0 | KILL_ERROR | 0: RF commands executed<br>1: ST25TV16K/64K is killed but still answers commands with error 0Fh | 0b |
| b1 | KILL_MUTE | 0: RF communication enabled<br>1: ST25TV16K/64K is killed and doesn't answer to any command | 0b |
| b7-b2 | RFU | - | 000000b |

1. Refer to *Table 7: System configuration memory map* for the KILL register.

### 5.1.2 Kill mode description

KILL register allow the user to definitely kill the ST25TV16K/64K tag.

KILL register is composed of two bits (see *Table 8: KILL*): KILL_ERROR and KILL_MUTE. For a normal usage of RF interface, bits KILL_MUTE and KILL_ERROR must be set to 0.

Three working modes are offered for ST25TV16K/64K:

- Kill mute mode:
  - When KILL_MUTE is set to 1, ST25TV16K/64K is killed. It can't be read or write and stay mute to any request. Kill mute mode is definitive.
- Kill error mode:
  - When KILL_MUTE is set to 0 and KILL_ERROR is set to 1, RF commands are interpreted but not executed. In case of a valid command, ST25TV16K/64K responds after t1 with the error code 0Fh. Inventory and Stay Quiet commands are not answered. Kill error mode is definitive
- Normal mode:
  - In normal usage, KILL_MUTE and KILL_ERROR are set to 0, ST25TV16K/64K processes the request and respond accordingly.

## 5.2 Data Protection

ST25TV16K/64K provides a special data protection mechanism based on passwords that unlock security sessions.

User memory can be protected for read and/or write access and system configuration can be protected from write access.

### 5.2.1 Data protection registers

**Table 9. A1SS(1)**

| RF | Command | Read Configuration (cmd code A0h) @04h<br>Write Configuration (cmd code A1h) @04h | |
|---|---|---|---|
| | Type | R always, W if configuration security session is open and configuration not locked | |
| **Bit** | **Name** | **Function** | **Factory Value** |
| b1-b0 | PWD_CTRL_A1 | 00: Area 1 user security session can't be open by password<br>01: Area 1 user security session is open by PWD_1<br>10: Area 1 user security session is open by PWD_2<br>11: Area 1 user security session is open by PWD_3 | 00b |
| b3-b2 | RW_PROTECTION_A1 | 00: Area 1 access: Read always allowed / Write always allowed<br>01: Area 1 access: Read always allowed, Write allowed if user security session is open<br>10: Area 1 access: Read always allowed, Write allowed if user security session is open<br>11: Area 1 access: Read always allowed, Write always forbidden | 00b |
| b7-b4 | RFU | - | 0000b |

1. Refer to *Table 7: System configuration memory map* for the A1SS register.