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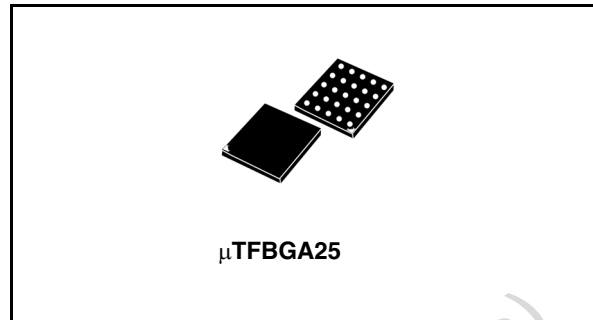
## Dual supply level translator for SD/ MINISD / T-FLASH

### Features

- High speed:
  - $t_{PD} = 6.2ns$  (Max.) at  $T_A = 85^\circ C$
  - $V_{CCB} = 3.0V$
  - $V_{CCA} = 2.3V$
- Low power dissipation:
  - $I_{CCA} = I_{CCB} = 5\mu A$  (Max.) at  $T_A = 85^\circ C$
- Balanced propagation delays:
  - $T_{PLH} \approx T_{PHL}$
- Power down protections on inputs and outputs
- $26\Omega$  series resistor on A-Side
- Operating voltage range:
  - $V_{CCA}$  (OPR) = 1.4V to  $V_{CCB}$
  - $V_{CCB}$  (OPR) = 1.4V to 3.6V
- Latch-up performance exceeds 500mA (JESD17)
- ESD performance:
  - HBM > 2kV (MIL STD 883 method 3015);
- RoHS compliant for  $\mu$ TFBGA25 package

### Description

The ST6G3237B is a dual supply low voltage CMOS Level Translator for SD/MiniSD/T-Flash fabricated with sub-micron silicon gate and five-layer metal wiring CMOS technology. Designed for use as an interface between a 3.3V bus and a 2.5V or 1.8V bus in a mixed 3.3V/1.8V, 3.3V/2.5V and 2.5V/1.8V supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation.



The A port is designed to track  $V_{CCA}$ . The B port is designed to track  $V_{CCB}$ .

This IC is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by CMD-dir/DATA0-dir/DAT123-dir inputs. The B-port interfaces with the 3V bus, the A-port with the 2.5V and 1.8V bus.

All inputs are equipped with protection circuits against static discharge, giving them  $\pm 2kV$  ESD immunity and transient excess voltage.

The ST6G3237B is  $V_{CCB} = 0V$  tolerant, achieving very low current consumption when the  $V_{CCB}$  is grounded.

**Figure 1. Device summary**

Part number	Package	Packaging
ST6G3237BTBR	$\mu$ TFBGA25	Tape and reel

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# 1 Logic diagram and truth table

Figure 1. Logic diagram

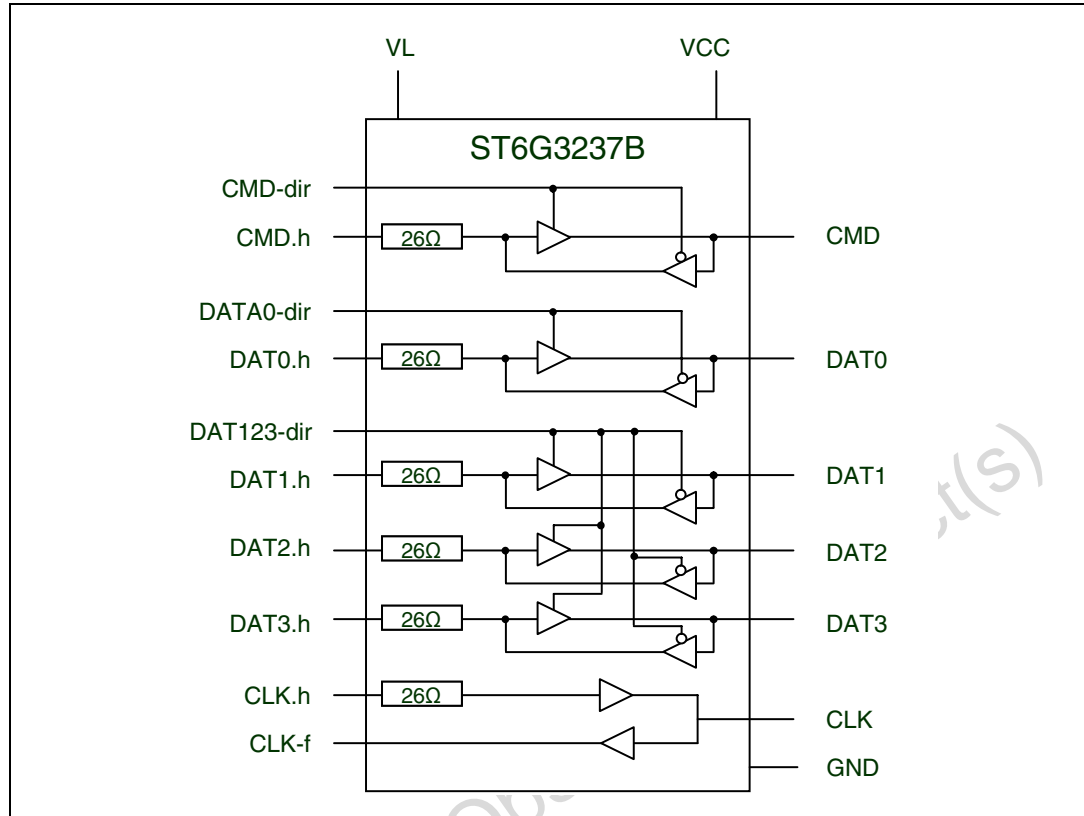


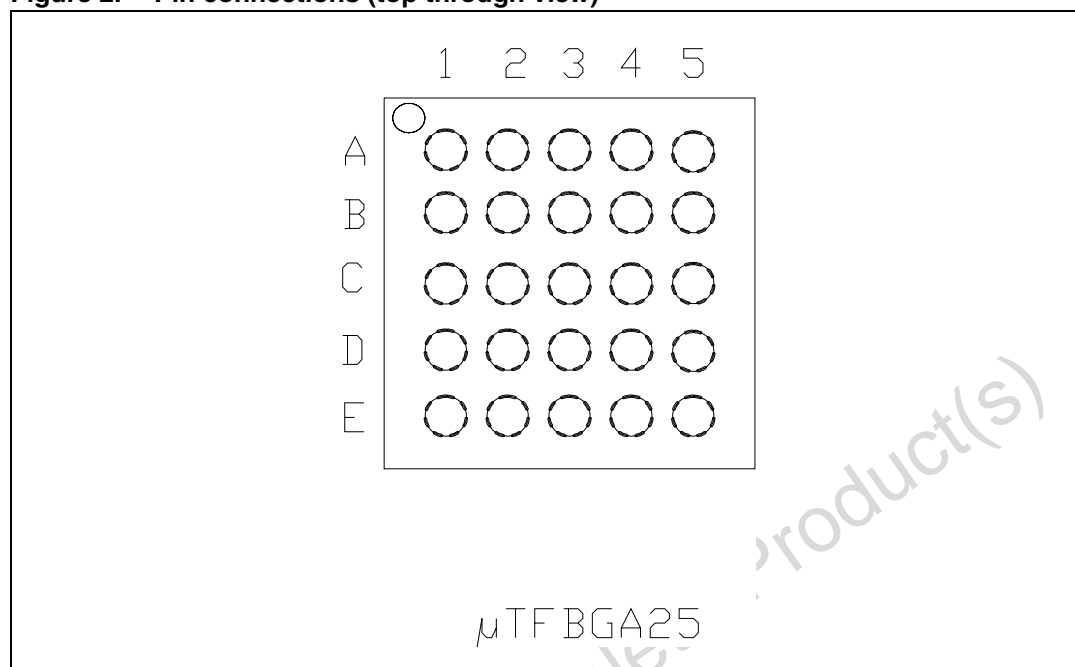
Table 2. Truth table

Function									Output
CMD-dir	DAT0-dir	DAT123-dir	CMD.h	CMD	DAT0.h	DAT0	DAT1.h DAT2.h DAT3.h	DAT1 DAT2 DAT3	
H	X	X	I	O	X	X	X	X	B = A
L	X	X	O	I	X	X	X	X	A = B
X	H	X	X	X	I	O	X	X	B = A
X	L	X	X	X	O	I	X	X	A = B
X	X	H	X	X	X	X	I	O	B = A
X	X	L	X	X	X	X	O	I	A = B

## 2 Pin settings

### 2.1 Pin connections

Figure 2. Pin connections (top through view)



## 2.2 Pin descriptions

Table 3. Pin descriptions

Pin N° μTFBGA25	Type	Side	Symbol	Name and function
A2	I	A-side	CMD-dir	Command direction HIGH = A to B LOW = B to A
D2	I/O	A-side	CMD.h	A-side Command
D4	I/O	B-Side	CMD	B-side Command
A3	I	A-Side	DAT0-dir	Data Direction HIGH = A to B (write) LOW = B to A (read)
D1	I/O	A-Side	DAT0.h	Data Input / Output
D5	I/O	B-Side	DAT0	Data Input / Output
E3	I	A-Side	DAT123-dir	Data Direction HIGH = A to B (write) LOW = B to A (read)
E1	I/O	A-Side	DAT1.h	Data Input / Output
A1	I/O	A-Side	DAT2.h	Data Input / Output
B1	I/O	A-Side	DAT3.h	Data Input / Output
E5	I/O	B-Side	DAT1	Data Input / Output
A5	I/O	B-Side	DAT2	Data Input / Output
B5	I/O	B-Side	DAT3	Data Input / Output
C1	I	A-Side	CLK.h	Clock Input
C5	O	B-Side	CLK	Clock Output
E2	O	A-Side	CLK-f	Clock Feedback
B3	-	A-Side	V <sub>CCA</sub>	Power supply
B4	-	B-Side	V <sub>CCB</sub>	Power supply
C3, C4	-	-	GND	Ground (0V)
A4, B2, C2, D3, E4	-	-	NC	No connect

- **CMD, Command** is a bidirectional line. The host and card drivers are operating in push-pull.
- **DAT0-3, Data lines** are bi-directional lines. Host and card drivers are operating in push-pull mode.
- **CLK, Clock** is a host to card signal. CLK operates in push-pull mode.
- **Feedback (return) Clock** is feedback clock signal from level shifter to host for controlling delays.

### 3 Electrical ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CCA}$	Supply voltage	-0.5 to 4.6	V
$V_{CCB}$	Supply voltage	-0.5 to 4.6	V
$V_I$	DC input voltage	-0.5 to 4.6	V
$V_{I/OA}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OB}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OA}$	DC output voltage	-0.5 to $V_{CCA} + 0.5$	V
$V_{I/OB}$	DC output voltage	-0.5 to $V_{CCB} + 0.5$	V
$I_{IK}$	DC input diode current	-20	mA
$I_{OK}$	DC output diode current	-50	mA
$I_{OA}$	DC output current	$\pm 50$	mA
$I_{OB}$	DC output current	$\pm 50$	mA
$I_{CCA}$	DC $V_{CC}$ or ground current	$\pm 100$	mA
$I_{CCB}$	DC $V_{CC}$ or ground current	$\pm 100$	mA
$P_D$	Power dissipation	400	mW
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead temperature (10 sec)	260	$^{\circ}\text{C}$

**Table 5. Recommended operating conditions**

Symbol	Parameter	Value	Unit
$V_{CCA}$	Supply Voltage	1.4 to $V_{CCB}$	V
$V_{CCB}$	Supply Voltage	1.4 to 3.6	V
$V_I$	Input Voltage (CMD-dir/DAT0-dir/DAT123-dir)	0 to $V_{CCA}$	V
$V_{I/OA}$	I/O Voltage	0 to $V_{CCA}$	V
$V_{I/OB}$	I/O Voltage	0 to $V_{CCB}$	V
$T_{op}$	Operating Temperature	-40 to +85	$^{\circ}\text{C}$
dt/dv	Input Rise and Fall Time <sup>(1)</sup>	0 to 10	ns/V

1.  $V_{IN}$  from 0.8V to 2.0V at  $V_{CC} = 3.0V$

## 4 Electrical characteristics

### 4.1 DC electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test Conditions		Value					Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V <sub>IH</sub> (A port)	High Level Input Voltage	1.4 – 1.95	V <sub>CCA</sub> to 3.6	0.65V <sub>CCA</sub>			0.65V <sub>CCA</sub>		V
		1.95 – 2.7		1.7			1.7		
		2.7 – 3.6		2.0			2.0		
V <sub>IL</sub> (A port)	Low Level Input Voltage	1.4 – 1.95	V <sub>CCA</sub> to 3.6			0.35V <sub>CCA</sub>		0.35V <sub>CCA</sub>	V
		1.95 – 2.7				0.7		0.7	
		2.7 – 3.6				0.8		0.8	
V <sub>IH</sub> (B port)	High Level Input Voltage	1.4 – 1.95	1.4 to V <sub>CCB</sub>	0.65V <sub>CCB</sub>			0.65V <sub>CCB</sub>		V
		1.95 – 2.7		1.7			1.7		
		2.7 – 3.6		2.0			2.0		
V <sub>IL</sub> (B port)	Low Level Input Voltage	1.4 – 1.95	1.4 to V <sub>CCB</sub>			0.35V <sub>CCB</sub>		0.35V <sub>CCB</sub>	V
		1.95 – 2.7				0.7		0.7	
		2.7 – 3.6				0.8		0.8	

- All A-port I/Os and control inputs are powered by V<sub>CCA</sub>
- All B-port I/Os are powered by V<sub>CCB</sub>



Table 7. DC specifications

Symbol	Parameter	Test conditions			Value					Unit
		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
V <sub>OH</sub> (A port)	High level output voltage	1.4-3.6	1.4-3.6	I <sub>OH</sub> = -100µA	V <sub>CCA</sub> - 0.1					V
		1.4	1.4	I <sub>OH</sub> = -1 mA	1.20					
		1.65	1.65	I <sub>OH</sub> = -2 mA	1.40					
		2.3	2.3	I <sub>OH</sub> = -4 mA	1.90					
		3	3	I <sub>OH</sub> = -8 mA	2.45					
V <sub>OL</sub> (A port)	Low level output voltage	1.4-3.6	1.4-3.6	I <sub>OL</sub> = 100µA			0.10			V
		1.4	1.4	I <sub>OL</sub> = 1 mA			0.20			
		1.65	1.65	I <sub>OL</sub> = 2 mA			0.25			
		2.3	2.3	I <sub>OL</sub> = 4 mA			0.40			
		3	3	I <sub>OL</sub> = 8 mA			0.55			
V <sub>OH</sub> (B port)	High level output voltage	1.4-3.6	1.4-3.6	I <sub>OH</sub> = -100µA	V <sub>CCA</sub> - 0.1					V
		1.4	1.4	I <sub>OH</sub> = -2 mA	1.25					
		1.65	1.65	I <sub>OH</sub> = -4 mA	1.45					
		2.3	2.3	I <sub>OH</sub> = -8 mA	1.90					
		3	3	I <sub>OH</sub> = -24 mA	2.45					
V <sub>OL</sub> (B port)	Low level output voltage	1.4-3.6	1.4-3.6	I <sub>OL</sub> = 100µA			0.10			V
		1.4	1.4	I <sub>OL</sub> = 2 mA			0.15			
		1.65	1.65	I <sub>OL</sub> = 4 mA			0.20			
		2.3	2.3	I <sub>OL</sub> = 8 mA			0.30			
		3	3	I <sub>OL</sub> = 24 mA			0.55			
I <sub>IA</sub> , I <sub>IB</sub>	Input leakage current	2.7	3.6	V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1		±1	µA
I <sub>OFF</sub>	Power OFF leakage current	0	0	V <sub>IA</sub> = GND to 3.6 V <sub>IB</sub> = GND to 3.6			±1.0		±10	µA
I <sub>CCA</sub>	Quiescent supply current for A-side	1.4	1.4-3.6	V <sub>IA</sub> = V <sub>CCA</sub> or GND			0.5		5	µA
		1.4 - 3.6	0	V <sub>IB</sub> = V <sub>CCB</sub> or GND						
		1.4 - 3.6	3.6	DIR = A to B						
I <sub>CCB</sub>	Quiescent supply current	1.4	1.4-3.6	V <sub>IA</sub> = V <sub>CCA</sub> or GND			0.5		5	µA
		1.4 - 3.6	3.6	V <sub>IB</sub> = V <sub>CCB</sub> or GND DIR = B to A						
I <sub>OZ</sub>	Leakage current when I/O are in High-Z	3.6	3.6	V <sub>IOA</sub> = V <sub>CCA</sub> or GND			±0.5		±5	µA

## 4.2 AC electrical characteristics

**Table 8. AC electrical characteristics**  $f = 1\text{MHz}$ , 50% duty cycle,  $C_L = 30\text{pF}$ ,  $R_L = 500\Omega$

Symbol	Parameter	Test condition $T_A = -40$ to $85\text{ }^\circ\text{C}$						Unit
		$V_{CCA}=1.8 \pm 0.15\text{V}$		$V_{CCA}=1.8 \pm 0.15\text{V}$		$V_{CCA}=2.5 \pm 0.2\text{V}$		
		$V_{CCB}=2.5 \pm 0.2\text{V}$		$V_{CCB}=3.0 \pm 0.3\text{V}$		$V_{CCB}=3.0 \pm 0.3\text{V}$		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation delay time A to B (CMD)	1.0	3.7	1.0	3.8	1.0	3.6	ns
	Propagation delay time B to A (CMD)	1.0	3.6	1.0	3.9	1.0	3.6	
	Propagation delay time A to B (CLK)	1.0	3.2	1.0	3.4	1.0	3.2	
	Propagation delay time B to A (CLK-f)	1.0	7.6	1.0	7.7	1.0	7.5	
	Propagation delay time An to Bn (DATn)	1.0	6.2	1.0	6.2	1.0	6.2	
	Propagation delay time Bn to An (DATn)	1.0	5.3	1.0	5.3	1.0	5.3	
$t_{PZL}$ $t_{PZH}$	Output enable time from An to Bn	1.0	2.9	1.0	3.0	1.0	2.9	ns
	Output enable time from Bn to An	1.0	4.3	1.0	4.5	1.0	4.2	
$t_{PLZ}$ $t_{PHZ}$	Output disable time from An to Bn	1.0	7.8	1.0	8	1.0	7.8	ns
	Output disable time from Bn to An	1.0	5.4	1.0	5.5	1.0	5.3	
$t_{OSLH}$ $t_{OSHL}$	Output to output skew time (note 1,2)		0.5		0.5		0.5	ns
$t_{CDLH}$ $t_{CDHL}$	Clock and data skew time		0.5		0.5		0.5	ns
$f_{\text{max}}$	Clock	From A to B	52		52		52	MHz
		From B to A	52		52		52	
	Data	From A to B	52		52		52	Mbps
		From B to A	52		52		52	

### 4.3 Output slew rate

**Table 9. Output slew rate** (f = 1MHz, 50% duty cycle, C<sub>L</sub> = 30pF, R<sub>L</sub> = 500Ω)

Symbol	Parameter	From	To	V <sub>CCA</sub> = 1.8V ± 0.15V V <sub>CCB</sub> = 3V ± 0.3V		Unit
				Min.	Max.	
t <sub>r</sub>	Rise time	20%	80%		3	ns
t <sub>f</sub>	Fall time	80%	20%		3	ns

### 4.4 Capacitance characteristics

**Table 10. Capacitance characteristics**

Symbol	Parameter	Test condition			Value			Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C			
					Min.	Typ.	Max.	
C <sub>INB</sub>	Input capacitance	Open	Open		5		pF	
C <sub>I/O</sub>	Input/Output capacitance	3.0	1.8		6		pF	
C <sub>PD</sub> (1)	Power dissipation capacitance	3.0	2.5	f=10MHz	29		pF	
		3.0	1.8		29			

1. C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. I<sub>CC(opr)</sub> - C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/16 (per circuit)

## 5 Test circuit

Figure 3. Test circuit

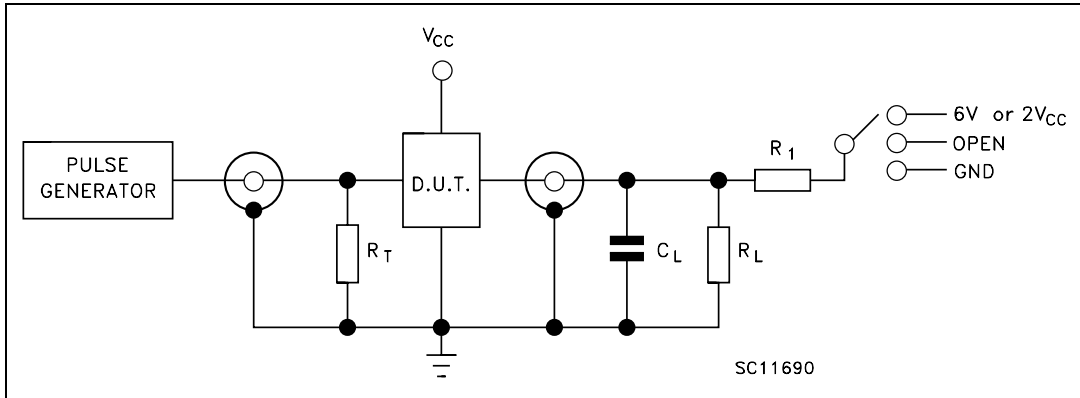


Table 11. Test values

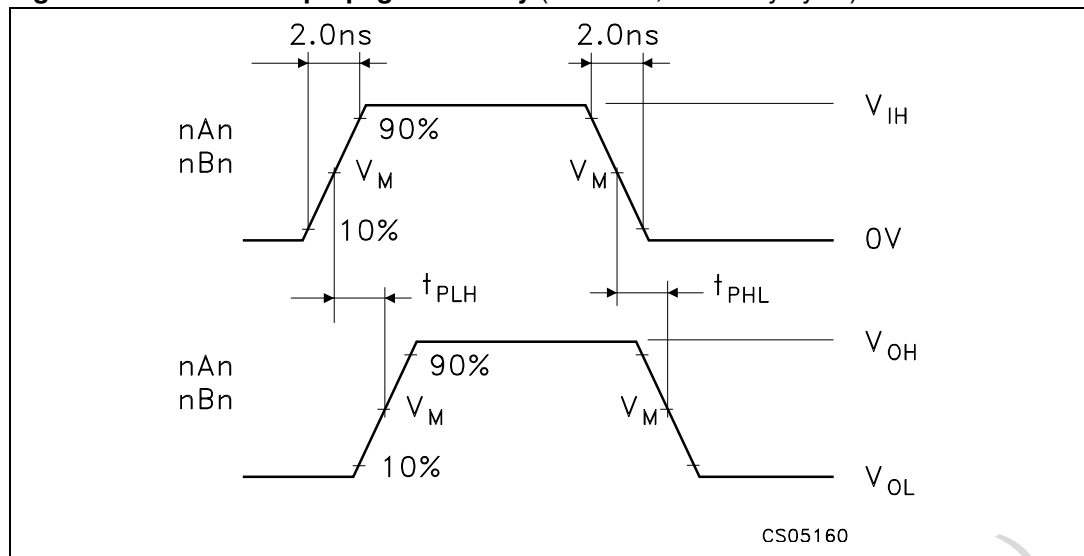
Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 3.0$ to $3.6V$ )	6V
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 2.3$ to $2.7V$ or $V_{CC} = 1.6$ to $1.95V$ )	$2V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

Table 12. Waveform symbol value

Symbol	$V_{CC}$		
	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V
$V_{IH}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_M$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OL} - 0.3V$	$V_{OL} - 0.15V$	$V_{OL} - 0.15V$

- $C_L = 30pF$  or equivalent (includes jig and probe capacitance)
- $R_L = R_1 = 500\Omega$  or equivalent
- $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

Figure 4. Waveform - propagation delay (f = 1MHz, 50% duty cycle)



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## 6 Package mechanical data

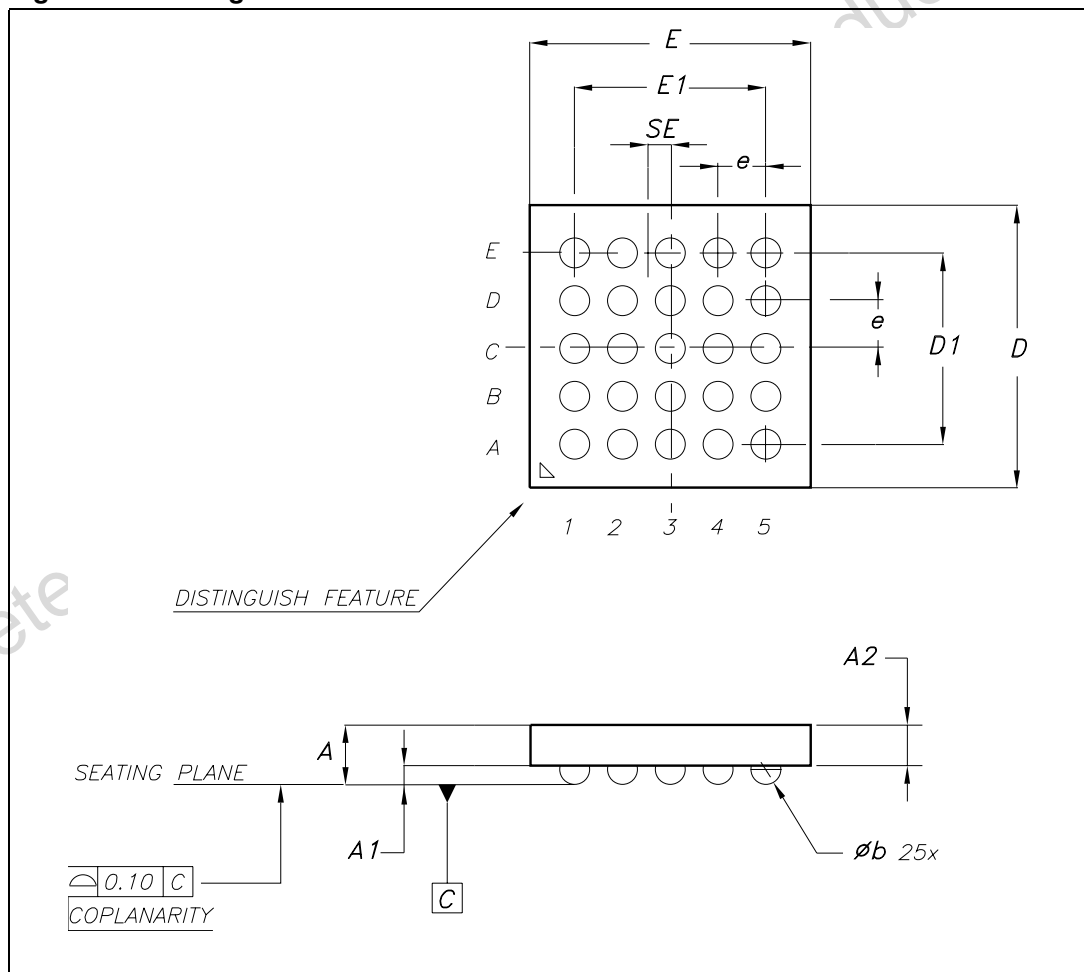
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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Table 13.  $\mu$ TFBGA25 Mechanical data

Dim.	mm.			mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.0	1.1	1.16	39.4	43.3	45.7
A1			0.25			9.8
A2	0.78		0.86	30.7		33.9
b	0.25	3.0	3.1	114.2	118.1	122.0
D	2.9	3.0	3.1	114.2	118.1	122.0
D1		2			78.8	
E	2.9	3.0	3.1	114.2	118.1	122.0
E1		2			78.8	
e		0.5			19.7	
SE		0.25			9.8	

Figure 5. Package dimensions



## 7 Revision history

Table 14. Revision history

Date	Revision	Changes
14-Jun-2007	1	First release

Obsolete Product(s) - Obsolete Product(s)



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