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## ST6G3244ME

Level translator for SD, SDIO, mini SD, and micro SD Cards  
with internal I/O supply and  $\pm 15$  kV ESD protection

### Features

- Supports 60 MHz clock rate
- Supports DDR mode for SD Card™
- Compliant with
  - SD Specification Part 1 Physical Layer Specification 3.00 (SDR12, SDR25, DDR50)
  - SD Specification Part 1 Physical Layer Specification 2.00
- Bi-directional with direction control pin
- Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- LDO power-down support. When the LDO is powered down,  $V_{CCB}$  is pulled to GND via the 130  $\Omega$  resistor. When  $V_{CCB} = 0$  V, there is no additional leakage seen on  $V_{CCA}$ .
- EMI filtering and signal conditioning
- Supports both 1.8 V and 2.9 V data translation on card side
- Integrated LDO to supply 1.8 V or 2.9 V power for B-side I/Os (pin-selectable); can be used also externally
- Integrated pull-up and pull-down resistors on B-side
- Operating voltage range
  - $V_{CCA} = 1.62$  V to 1.98 V
  - $V_{BAT} = 3.0$  V to 5.0 V
- Latch-up performance exceeds 100 mA (JEDEC Standard 78)
- ESD protection for card side (B-port, CD and WP pins)
  - $\pm 8$  kV contact discharge (IEC61000-4-2)
  - $\pm 15$  kV air-gap discharge (IEC61000-4-2)
- ESD protection for host side (A-side)
  - $\pm 2$  kV HBM (JEDEC 22-A114)
  - $\pm 200$  V MM (JEDEC 22-A115)



- Operating temperature range  $-40$  °C to  $+85$  °C
- Space-saving Flip Chip 25 package (2 x 2 x 0.605 mm, 0.4 mm bump pitch)
- RoHS compliant, lead-free soldering capable

### Applications

- Mobile phones, smartphones
- PDAs
- Cameras
- SD Card readers
- Any device with SD memory card

Table 1. Device summary

Order code	Package	Packing	Package topmark
ST6G3244MEBJR	Flip Chip 25 2 x 2 x 0.605 mm, 0.4 mm bump pitch	Tape and reel (5000 parts per reel)	VKH, VKV

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# 1 Description

The ST6G3244ME is a dual supply, low voltage 6-bit bi-directional CMOS level translator for SD, mini SD and micro SD Cards. Designed for use as an interface between baseband and memory cards, it achieves high speed operation while maintaining CMOS low-power dissipation.

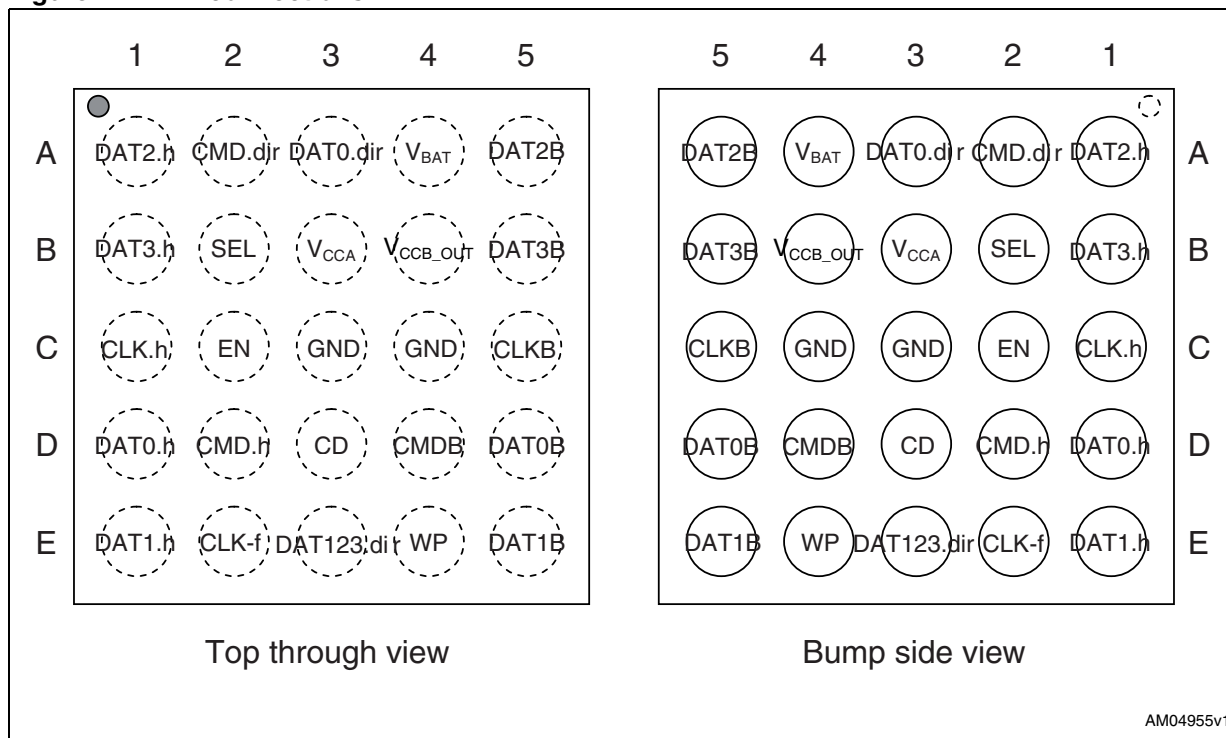
The A-port is designed to track  $V_{CCA}$ . The internal LDO is powered by  $V_{BAT}$  and provides a power supply of either 1.8 V or 2.9 V to the B-side I/Os (programmed by the SEL pin). The B-port is designed to track  $V_{CCB}$ . The  $V_{CCB}$  voltage can be also used externally. When  $V_{CCB} = 0$  V, there is no additional leakage seen on  $V_{CCA}$ . All outputs are push-pull type.

This device is intended for two-way asynchronous communication between data buses. The direction of data transmission is determined by CMD.dir, DAT0.dir and DAT123.dir inputs.

All inputs are equipped with protection circuits against electrostatic discharge, giving them  $\pm 2$  kV (on A-side) and  $\pm 15$  kV (on B-side, CD and WP) ESD and transient excess voltage immunity.

## 2 Functional description

Figure 1. Pin connections



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Table 2. Signal names (1)

Pin name	Bump	Type	Side	Description
V <sub>CCA</sub>	B3	Input	A	Host side positive power supply (1.8 V)
V <sub>CCB_OUT</sub>	B4	Output	B	Internal supply voltage decoupling, V <sub>CCB</sub> LDO output
V <sub>BAT</sub>	A4	Input	A	Battery power supply (3.0 - 5.0 V)
GND	C4	Ground	-	Ground
GND	C3	Ground	-	Ground
EN	C2	Input	A	Enable, active-high
SEL	B2	Input	A	V <sub>CCB</sub> selection (B-side supply voltage, 1.8 V/2.9 V)
CMD.dir	A2	Input	A	Command direction control
CMD.h	D2	I/O	A	Host side command
CLK.h	C1	Input	A	Host side clock input
CLK-f	E2	Output	A	Clock feedback to host
DAT0.dir	A3	Input	A	DAT0 direction control
DAT0.h	D1	I/O	A	Host side data input/output
DAT123.dir	E3	Input	A	DAT1, DAT2, DAT3 direction control
DAT1.h	E1	I/O	A	Host side data input/output

**Table 2. Signal names (continued)<sup>(1)</sup>**

Pin name	Bump	Type	Side	Description
DAT2.h	A1	I/O	A	Host side data input/output
DAT3.h	B1	I/O	A	Host side data input/output
WP	E4	Input to CPU	A	Write protect
CD	D3	Input to CPU	A	Card detect
CMDB	D4	I/O	B	Card side command
CLKB	C5	Output	B	Card side clock output
DAT0B	D5	I/O	B	Card side data input/output
DAT1B	E5	I/O	B	Card side data input/output
DAT2B	A5	I/O	B	Card side data input/output
DAT3B	B5	I/O	B	Card side data input/output

- Collective names are used for groups of pins in the datasheet:
  - \*.dir = CMD.dir, DAT0.dir, DAT123.dir
  - \*.h = CMD.h, CLK.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h
  - \*B = CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B
  - V<sub>IA</sub> = all A-side input pins.

**Table 3. Direction control**

EN	Command signals			Direction of A-side signals <sup>(1)</sup>					Direction of B-side signals <sup>(1)</sup>							
	CMD.dir	DAT0.dir	DAT123.dir	CMD.h	CLK.h	CLK-f	DAT0.h	DAT1.h	DAT2.h	DAT3.h	CMDB	CLKB	DAT0B	DAT1.B	DAT2.B	DAT3.B
H	H	X	X	IN	IN	OUT	X	X			OUT	OUT	X	X		
H	L	X	X	OUT	IN	OUT	X	X			IN	OUT	X	X		
H	X	H	X	X	IN	OUT	IN	X			X	OUT	OUT		X	
H	X	L	X	X	IN	OUT	OUT	X			X	OUT	IN		X	
H	X	X	H	X	IN	OUT	X	IN			X	OUT	X		OUT	
H	X	X	L	X	IN	OUT	X	OUT			X	OUT	X		IN	
L	X	X	X	X	X	Z	X	X			(2)	Z	(2)		(2)	

- When the direction of the A-side signal is INPUT, the host CPU WRITES to the SD Card (i.e. the direction of the B-side signal is OUTPUT).  
When the direction of the A-side signal is OUTPUT, the host CPU READS the SD Card (i.e. the direction of the B-side signal is INPUT).
- Level of the B-side signals when EN = L is defined by the internal resistors as listed in [Table 7](#).

**Note:** *During application design it has to be considered that the level shifter device needs some time to change the direction after a change of the .dir signal level. Valid data on the input of the corresponding channel can then start after a turn-around time, see the t<sub>TA</sub> specification in [Table 12](#).*



Figure 2. Block diagram

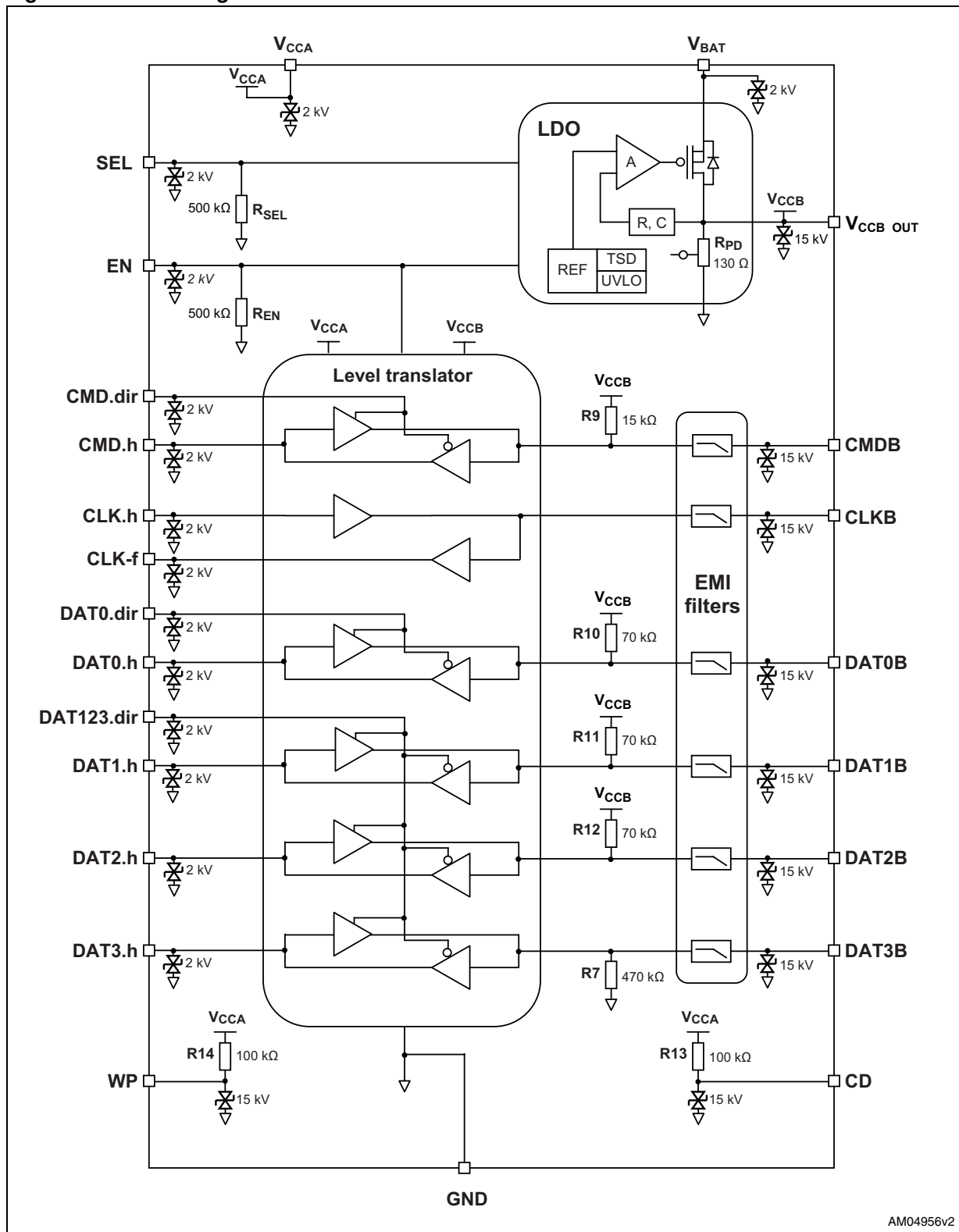
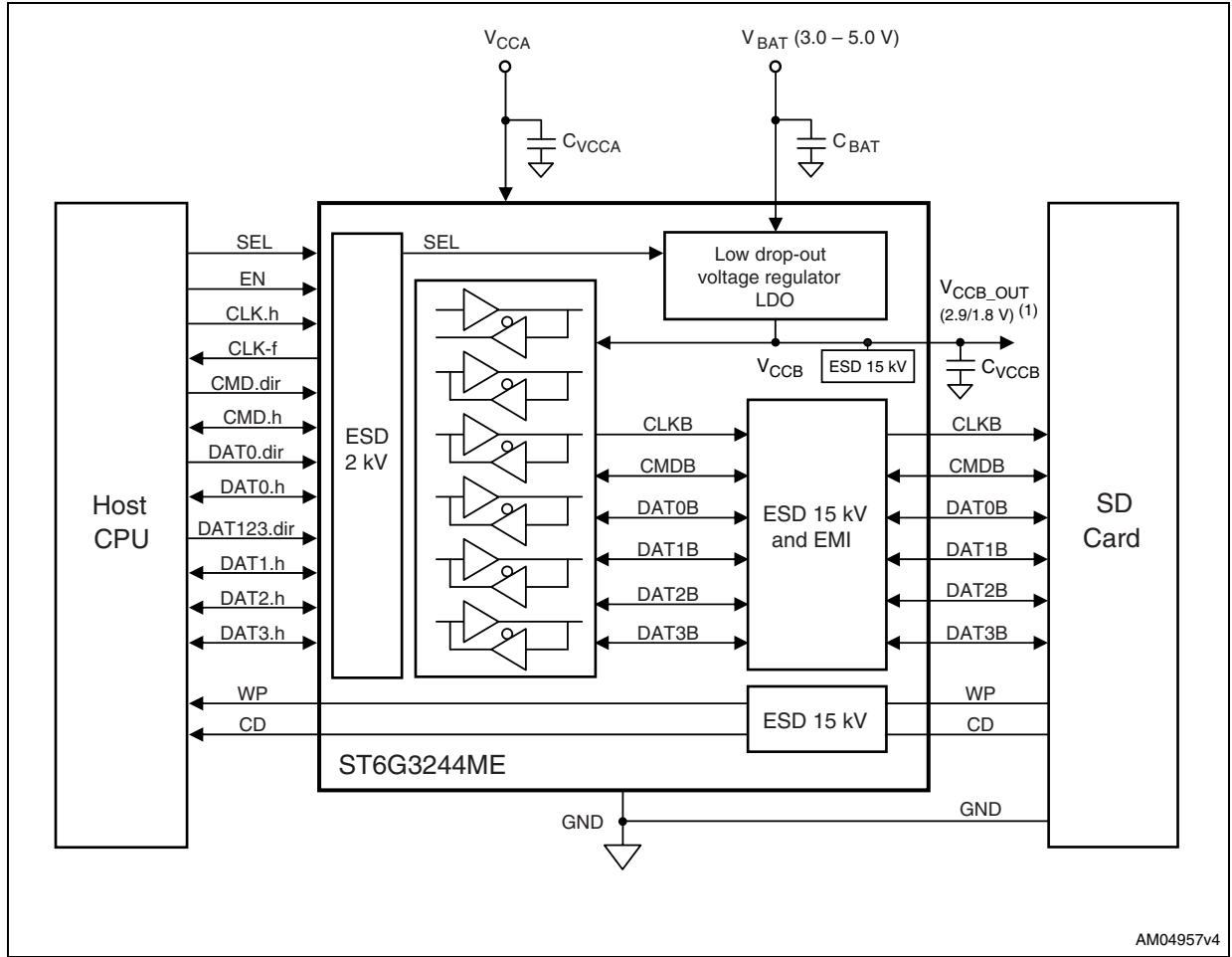


Figure 3. Typical application diagram



1. Can be used externally, however, note that it follows VCCB value that is switched between 2.9 and 1.8 V by the SEL pin.

### 3 Maximum ratings

Stressing the device above the rating listed in [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 5: Recommended operating conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter		Value	Unit	
T <sub>JMAX</sub>	Maximum junction temperature		150	°C	
R <sub>TH(J-A)</sub> <sup>(1)</sup>	Thermal resistance from junction to ambient (board: epoxy FR4, e <sub>(CU)</sub> = 40 μm, 4 layers)		64	°C/W	
P <sub>DMAX</sub>	Maximum power dissipation: $P_{DMAX} = (T_{JMAX} - T_{AMAX})/R_{TH(J-A)}$		1	W	
T <sub>STG</sub>	Storage temperature range		-55 to 150	°C	
V <sub>CCA</sub>	Power supply		-0.3 to 4.6	V	
V <sub>BAT</sub>	Battery power supply		-0.3 to 5.5	V	
V <sub>IO</sub>	CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B		-0.3 to V <sub>CCB</sub> + 0.3	V	
	V <sub>CCA</sub> , SEL, EN		-0.3 to 4.6		
	CMD.dir, CMD.h, CLK.h, CLK-f, DAT0.dir, DAT0.h, DAT123.dir, DAT1.h, DAT2.h, DAT3.h, WP, CD		-0.3 to V <sub>CCA</sub> + 0.3		
ESD	<b>A-side (host CPU), all pins:</b> V <sub>CCA</sub> , EN, SEL, DAT123.dir, CMD.dir, CMD.h, CLK.h, CLK-f, DAT0.dir, DAT0.h, DAT1.h, DAT2.h, DAT3.h, V <sub>BAT</sub>	HBM	JEDEC 22-A114	±2	kV
		MM	JEDEC 22-A115	±200	V
	<b>B-side (SD Card), external pins:</b> CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B, WP, CD, V <sub>CCB_OUT</sub>	Air discharge	IEC61000-4-2	±15	kV
		Contact discharge	IEC61000-4-2	±8	kV

1. The thermal resistance depends on the printed circuit board layout. To dissipate the heat efficiently away from the Flip-Chip bumps, it is recommended to make the copper planes as large as possible and consider using thermal vias.

## 4 DC and AC parameters

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>CCA</sub>	Power supply		1.62	1.8	1.98	V
V <sub>BAT</sub>	Battery power supply		3.0		5.0	V
C <sub>BAT</sub>	External battery capacitance	Ceramic capacitor	1.0	2.2	2.8	μF
C <sub>VCCA</sub>	V <sub>CCA</sub> decoupling capacitor	Ceramic capacitor	0.1			μF
C <sub>VCCB</sub>	Internal supply voltage (V <sub>CCB</sub> ) decoupling capacitor	Ceramic capacitor	1.0	2.2	2.8	μF
T <sub>A</sub>	Ambient operating temperature		-40	25	85	°C
T <sub>J</sub>	Junction operating temperature		-40	25	125	°C
P <sub>D</sub>	Maximum power dissipation	$P_D = (T_J - T_A)/R_{TH(J-A)}$			625	mW
V <sub>IO_B</sub>	I/O voltage on external pins (without WP and CD) - B-side	CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B	0		V <sub>CCB</sub>	V
V <sub>IO_A</sub>	I/O voltage on internal pins (includes WP and CD) - A-side	EN, SEL, WP, CD, DAT123.dir, CMD.dir, CMD.h, CLK.h, CLK-f, DAT0.dir, DAT0.h, DAT1.h, DAT2.h, DAT3.h	0		V <sub>CCA</sub>	V

**Table 6. Current levels under recommended operating conditions (T<sub>A</sub> = -40 °C to 85 °C)**

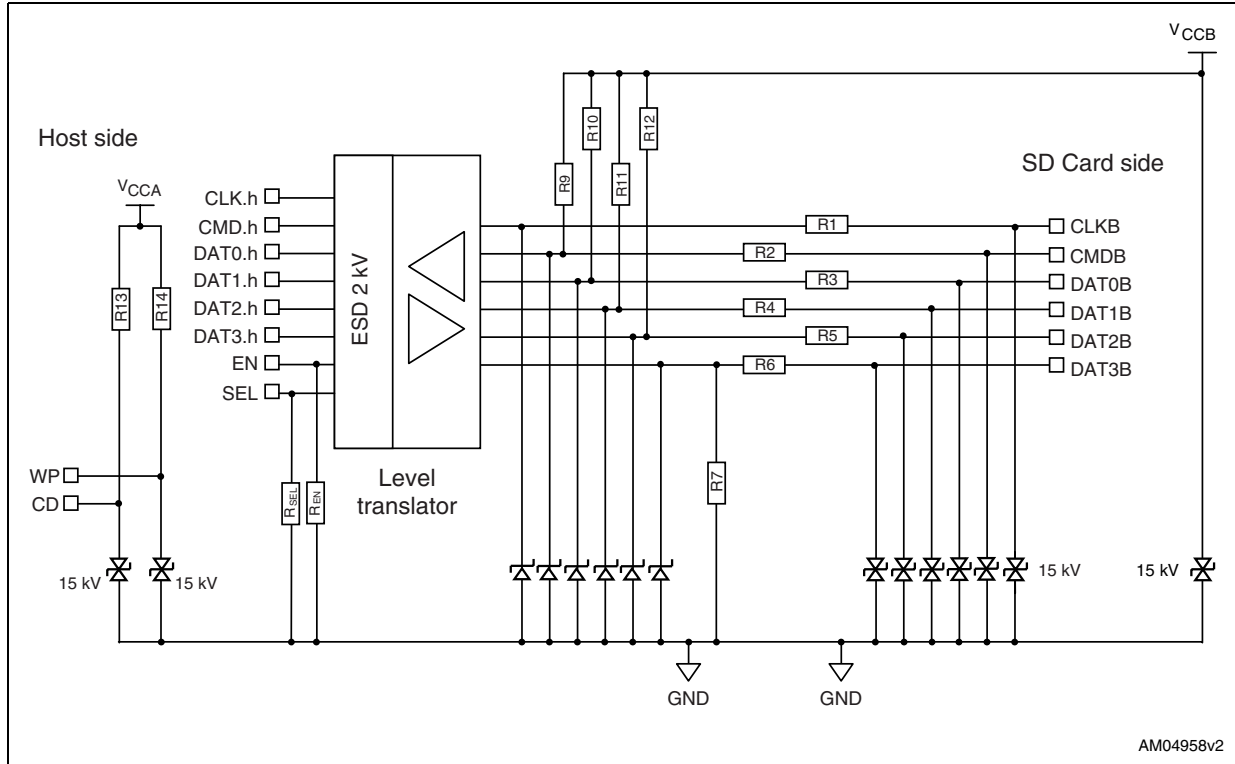
Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
I <sub>Q_OFF</sub>	Quiescent current consumption I <sub>CCA_OFF</sub>	V <sub>EN</sub> = 0.4 V, V <sub>BAT</sub> = 3.4 V, V <sub>CCA</sub> = 1.98 V *.dir, *B = 0 V, WP = CD = V <sub>CCA</sub>			1	μA
	Quiescent current consumption I <sub>BAT_OFF</sub>	All other pins floating			1	μA
I <sub>Q_ON</sub>	Quiescent current consumption (Ground pin current) I <sub>BAT</sub> + I <sub>CCA</sub>	*.dir = 0 V, V <sub>BAT</sub> = 3.4 V V <sub>EN</sub> = V <sub>CCA</sub> = V <sub>CLK.h</sub> = 1.98 V All other pins floating	I <sub>OUT</sub> = 100 μA		150 <sup>(2)</sup>	μA
			I <sub>OUT</sub> = 50 mA		250 <sup>(2)</sup>	
I <sub>CCA_ON</sub>	Quiescent current on V <sub>CCA</sub>	V <sub>EN</sub> = V <sub>CCA</sub> = 1.92 V, V <sub>BAT</sub> = 3.4 V, *.dir = V <sub>CCA</sub> , V <sub>IA</sub> = *.h = V <sub>CCA</sub>		3	10	μA

- Collective names for groups of pins:  
\*.dir = CMD.dir, DAT0.dir, DAT123.dir  
\*.h = CMD.h, CLK.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h  
\*B = CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B  
V<sub>IA</sub> = all A-side input pins.

- Guaranteed by design.

# 5 Passive integration and low-pass EMI filter

Figure 4. Circuit diagram of ST6G3244ME (without LDO)



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Table 7. Components

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
C <sub>IN-A</sub>	Input capacitance for A-side	V <sub>BAT</sub> = 3.4 V, *.dir = V <sub>EN</sub> = V <sub>CCA</sub> f = 1 MHz, V <sub>DC</sub> = 0 V ± 30 mV, V <sub>AC</sub> = 30 mV		5	10	pF
C <sub>IN-B</sub>	Input capacitance for B-side	V <sub>BAT</sub> = 3.4 V, *.dir = 0 V, V <sub>EN</sub> = V <sub>CCA</sub> f = 1 MHz, V <sub>DC</sub> = 0 V ± 30 mV, V <sub>AC</sub> = 30 mV		24	28	pF
R1, R2, R3, R4, R5, R6 <sup>(2)</sup>	EMIF resistors	T <sub>J</sub> = 25 °C	32	40	48	Ω
R10, R11, R12	DAT0B, DAT1B, DAT2B pull-up resistors	T <sub>J</sub> = 25 °C	49	70	91	kΩ
R9	CMDB pull-up resistor	T <sub>J</sub> = 25 °C	10.5	15	19.5	kΩ
R7	DAT3B pull-down resistor	T <sub>J</sub> = 25 °C	329	470	611	kΩ
R13	CD pull-up resistor	T <sub>J</sub> = 25 °C	70	100	130	kΩ
R14	WP pull-up resistor	T <sub>J</sub> = 25 °C	70	100	130	kΩ
R <sub>PD</sub>	LDO resistor	T <sub>J</sub> = 25 °C	90	130	170	Ω
R <sub>EN</sub>	EN pull-down resistor	T <sub>J</sub> = 25 °C		500		kΩ
R <sub>SEL</sub>	SEL pull-down resistor	T <sub>J</sub> = 25 °C		500		kΩ

1. See [Note 1 on page 7](#) for definition of collective names of pins, for example \*.dir.
2. These values are guaranteed by design and statistical process control.

Table 8. EMI filter attenuation

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IL <sub>0-200M</sub>	Filter attenuation <sup>(1)</sup>	Frequency range: 0 Hz to 200 MHz	6	-	-	dB
IL <sub>401-800M</sub>		Frequency range: 401 MHz to 800 MHz	10	-	-	
IL <sub>801-2500M</sub>		Frequency range: 801 MHz to 2.5 GHz	20	-	-	
IL <sub>2600-6000M</sub>		Frequency range: 2.6 GHz to 6 GHz	30	-	-	

1. Guaranteed by design.

## 6 Data transmission

All values in the tables below are guaranteed across the operating temperature and voltage range unless otherwise specified.

**Table 9. DC voltage levels on host CPU side ( $T_A = -40\text{ °C}$  to  $85\text{ °C}$ )**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{IHA}$	High level input voltage		$0.65 V_{CCA}$	$V_{CCA}$		V
$V_{ILA}$	Low level input voltage			0	$0.35 V_{CCA}$	V
$V_{OHA}$	High level output voltage	$I_{OH} = -6\text{ mA}$ , $V_{CCA} = 1.62\text{ V}$	$V_{CCA} - 0.45$	$V_{CCA}$		V
$V_{OLA}$	Low level output voltage	$I_{OL} = 7\text{ mA}$ , $V_{CCA} = 1.62\text{ V}$		0	0.45	V

**Table 10. DC voltage levels on SD Card side ( $T_A = -40\text{ °C}$  to  $85\text{ °C}$ )**

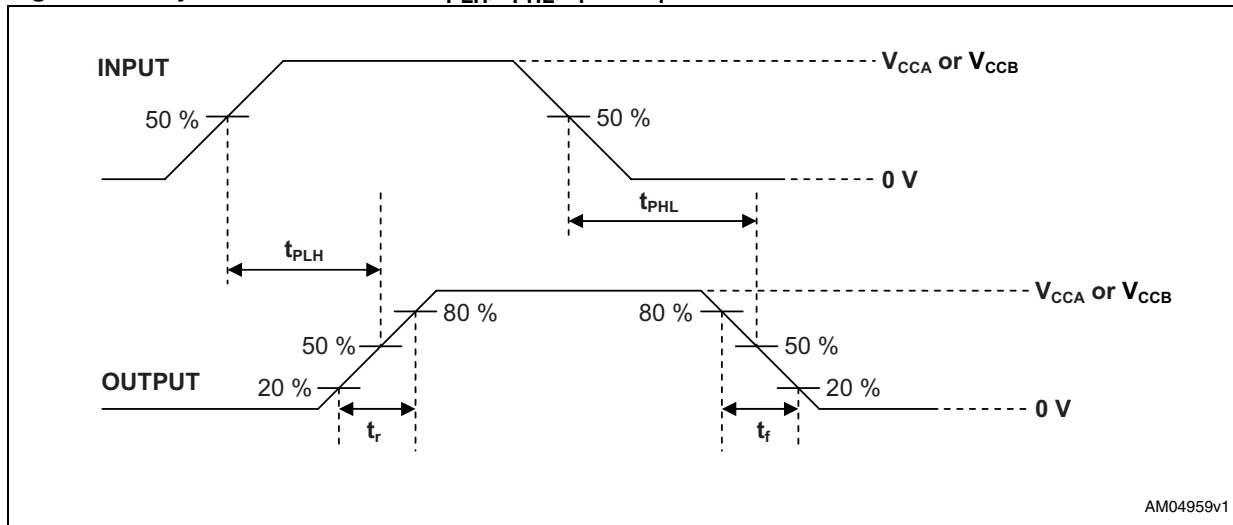
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{IHB}$	High level input voltage		$0.7 V_{CCB}$	$V_{CCB}$		V
$V_{ILB}$	Low level input voltage			0	$0.3 V_{CCB}$	V
$V_{OHB}$	High level output voltage	$I_{OH} = -4\text{ mA}$	$0.8 V_{CCB}$	$V_{CCB}$		V
$V_{OLB}$	Low level output voltage	$I_{OL} = 4\text{ mA}$		0	$0.2 V_{CCB}$	V

**Table 11. Leakage and short-circuit currents**

Symbol	Parameter	Test condition <sup>(1)</sup>	Min.	Typ.	Max.	Unit
$I_{LH}$	Leakage current on host side pins	$V_{SEL} = 0\text{ V}$ , $V_{EN} = *.dir = V_{CCA} = 1.98\text{ V}$ $V_{IA} = V_{CCA}$ or $0\text{ V}$ , $V_{BAT} = 3.4\text{ V}$			5	$\mu\text{A}$
$I_{LSD}$	Leakage current on SD Card side pins	$V_{SEL} = 0\text{ V}$ , $V_{BAT} = 3.4\text{ V}$ , $V_{CLK.h} = V_{CCA}$ $V_{CMD} = V_{DAT0} = V_{DAT1} = V_{DAT2} = V_{CCB}$ $V_{DAT3} = *.dir = 0\text{ V}$			5	$\mu\text{A}$
$I_{SCH}$	Short-circuit current on host side pins	SD Card input = H, host = $0\text{ V}$ SD Card input = $0\text{ V}$ , host = $V_{CCA} = 1.8\text{ V}$ $*.dir = 0\text{ V}$ , $V_{BAT} = 3.4\text{ V}$ , $T_J = 25\text{ °C}$		25		mA
$I_{SCSD}$	Short-circuit current on SD Card side pins	Host input = H, SD Card = $0\text{ V}$ Host input = L, SD Card = $V_{CCB} = 2.9\text{ V}$ , $T_J = 25\text{ °C}$ , $*.dir = V_{CCA} = 1.8\text{ V}$ , $V_{BAT} = 3.4\text{ V}$	25		70	mA
		Host input = H, SD Card = $0\text{ V}$ Host input = L, SD Card = $V_{CCB} = 1.8\text{ V}$ , $T_J = 25\text{ °C}$ , $*.dir = V_{CCA} = 1.8\text{ V}$ , $V_{BAT} = 3.4\text{ V}$	25		70	

- Collective names for groups of pins:  
 $*.dir = \text{CMD.dir, DAT0.dir, DAT123.dir}$   
 $*.h = \text{CMD.h, CLK.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h}$   
 $*B = \text{CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B}$   
 $V_{IA} = \text{all A-side input pins.}$

Figure 5. Symbol definitions of  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$  for AC characteristics



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Table 12. AC characteristics ( $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ )

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$t_{PHL}$	Propagation delay HL from host to SD	See <a href="#">Section 6.1</a>	$V_{CCB} = 1.8\text{ V}$		3.2	7	ns
			$V_{CCB} = 2.9\text{ V}$		3.2	5	
$t_{PLH}$	Propagation delay LH from host to SD	See <a href="#">Section 6.1</a>	$V_{CCB} = 1.8\text{ V}$		3.2	7	ns
			$V_{CCB} = 2.9\text{ V}$		3.2	5	
$t_{PHL}$	Propagation delay HL from SD to host	See <a href="#">Section 6.2</a>	$V_{CCB} = 1.8\text{ V}$		3.0	7	ns
			$V_{CCB} = 2.9\text{ V}$		2.8	5	
$t_{PLH}$	Propagation delay LH from SD to host	See <a href="#">Section 6.2</a>	$V_{CCB} = 1.8\text{ V}$		3.0	7	ns
			$V_{CCB} = 2.9\text{ V}$		2.8	5	
$t_r$	Rise time from host to SD	See <a href="#">Section 6.1</a>	$V_{CCB} = 1.8\text{ V}$		2.0	4	ns
			$V_{CCB} = 2.9\text{ V}$		2.0	4	
	Rise time from SD to host	See <a href="#">Section 6.2</a>	$V_{CCB} = 1.8\text{ V}$		2.0	4	
			$V_{CCB} = 2.9\text{ V}$		2.0	4	
$t_f$	Fall time from host to SD	See <a href="#">Section 6.1</a>	$V_{CCB} = 1.8\text{ V}$		2.0	4	ns
			$V_{CCB} = 2.9\text{ V}$		2.0	4	
	Fall time from SD to host	See <a href="#">Section 6.2</a>	$V_{CCB} = 1.8\text{ V}$		2.0	4	
			$V_{CCB} = 2.9\text{ V}$		2.0	4	
$t_{TA}$	Turn-around time (direction switch response, for all channels) <sup>(1)</sup>		$V_{CCB} = 1.8\text{ V}$ or $2.9\text{ V}$ , $C_L = 15\text{ pF}$		7.5	12	ns
$t_{SKEW}$	Delay differences from host to SD	See <a href="#">Section 6.1</a>	See <a href="#">Section 6.3</a>	-0.5	0	0.5	ns
$t_{CH2CH-SKEW}$	Channel-to-channel skew			-0.5	0	0.5	ns
$t_{SKEW.f}$	CLK-f to CMD, DAT delay (valid for PCB trace lengths from 20 mm to 100 mm)	See <a href="#">Section 6.2</a>	See <a href="#">Section 6.4</a>	0.3		1.2	ns
$t_{P\_CLKF}$	Propagation delay from CLK feedback	See <a href="#">Section 6.2</a>	$V_{CCB} = 1.8\text{ V}$		5.7	13.5	ns
			$V_{CCB} = 2.9\text{ V}$		5.5	9.5	



**Table 12. AC characteristics ( $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ ) (continued)**

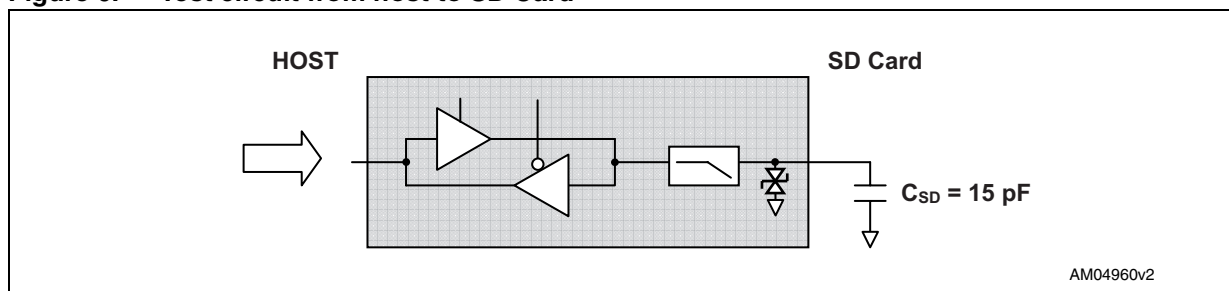
Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$t_{r\_CLKF}$	Rise time for CLK feedback	See <a href="#">Section 6.2</a>	$V_{CCB} = 1.8\text{ V}$		1.0	3	ns
			$V_{CCB} = 2.9\text{ V}$		1.0	3	
$t_{f\_CLKF}$	Fall time for CLK feedback	See <a href="#">Section 6.2</a>	$V_{CCB} = 1.8\text{ V}$		1.0	3	ns
			$V_{CCB} = 2.9\text{ V}$		1.0	3	
$f_{MAX}$	Clock rate					60	MHz
	Data rate					120	Mbps

1. The time after the .dir signal transition that the device needs to switch direction, after that it is ready to accept valid data on the switched input.

### 6.1 Test circuit from host to SD Card

The test circuit from the host to the SD Card is shown in [Figure 6](#). Timings are measured for the whole line cell (translator + EMI + ESD) on an external load  $C_{SD} = 15\text{ pF}$  (board capacitance  $5\text{ pF}$  + SD Card capacitance  $10\text{ pF}$ ).

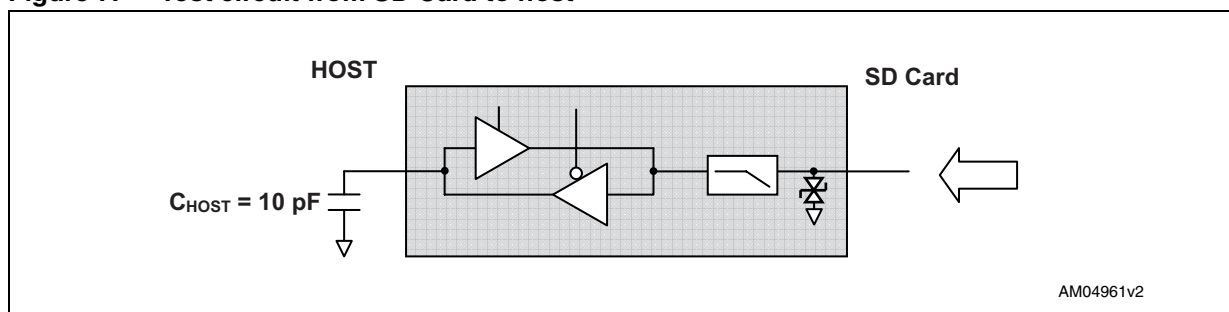
**Figure 6. Test circuit from host to SD Card**



### 6.2 Test circuit from SD Card to host

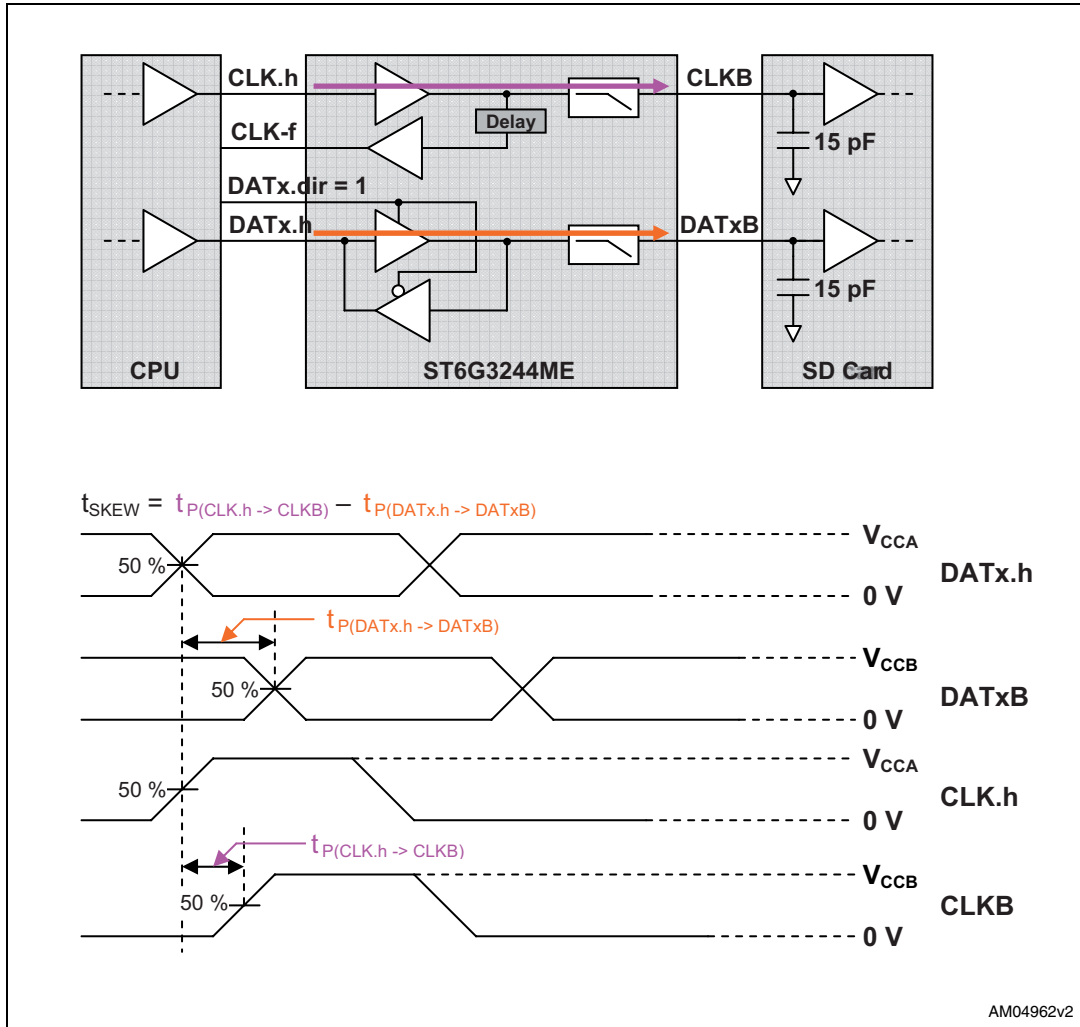
The test circuit from the SD Card to the host is shown in [Figure 7](#). Timings are measured for the whole line cell (translator + EMI + ESD) on an external load  $C_{HOST} = 10\text{ pF}$  (board capacitance + host capacitance).

**Figure 7. Test circuit from SD Card to host**



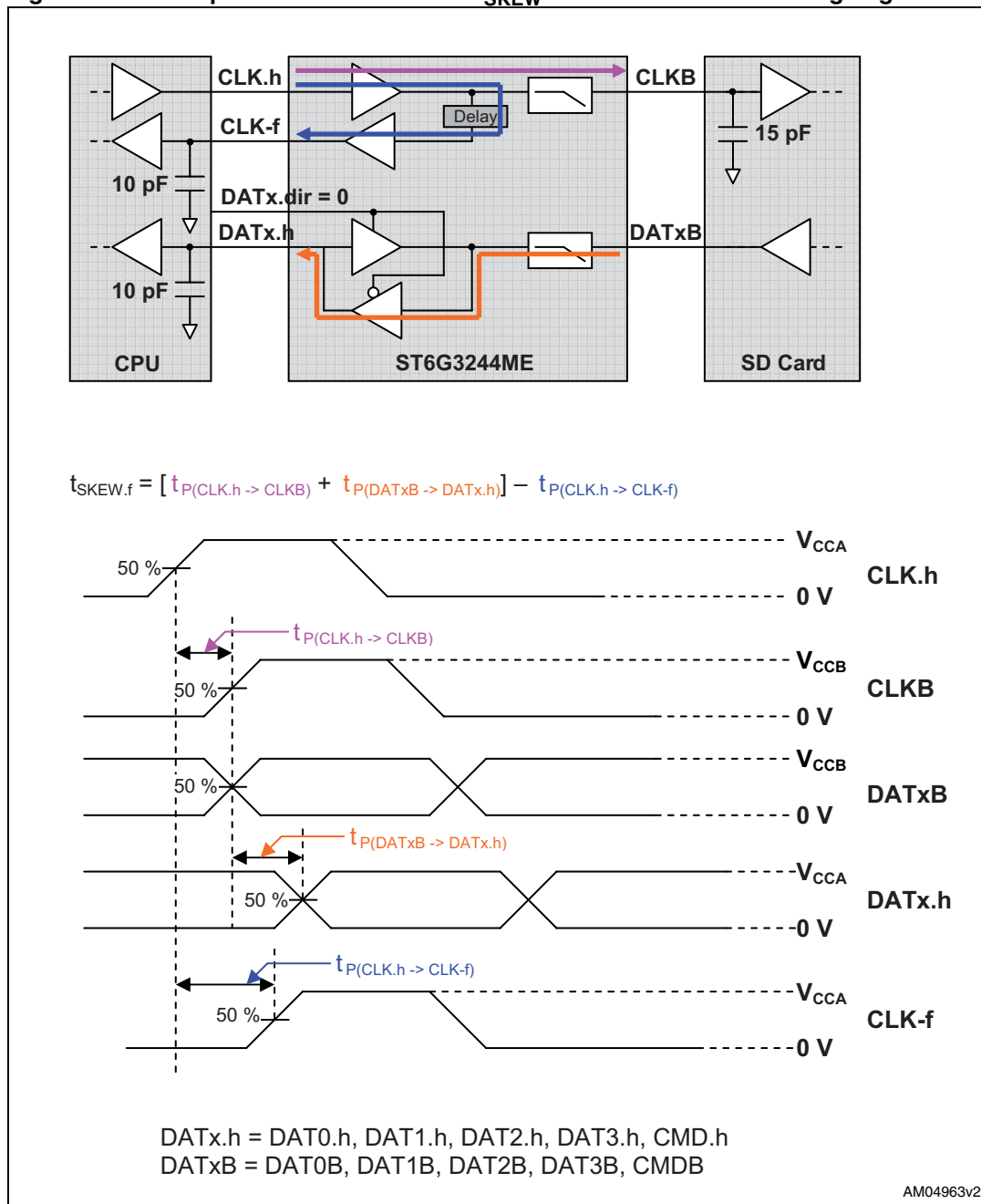
### 6.3 Measurement of $t_{\text{SKEW}}$ (SD Card to host) from rising edge CLK.h

Figure 8. Example of measurement of  $t_{\text{SKEW}}$  (SD Card to host) from rising edge CLK.h



### 6.4 Measurement of $t_{\text{SKEW.f}}$ (read mode) from rising edge CLK.h

Figure 9. Example of measurement of  $t_{\text{SKEW}}$  for read mode from rising edge CLK.h



# 7 Low drop-out voltage regulator

Figure 10. Low drop-out voltage regulator

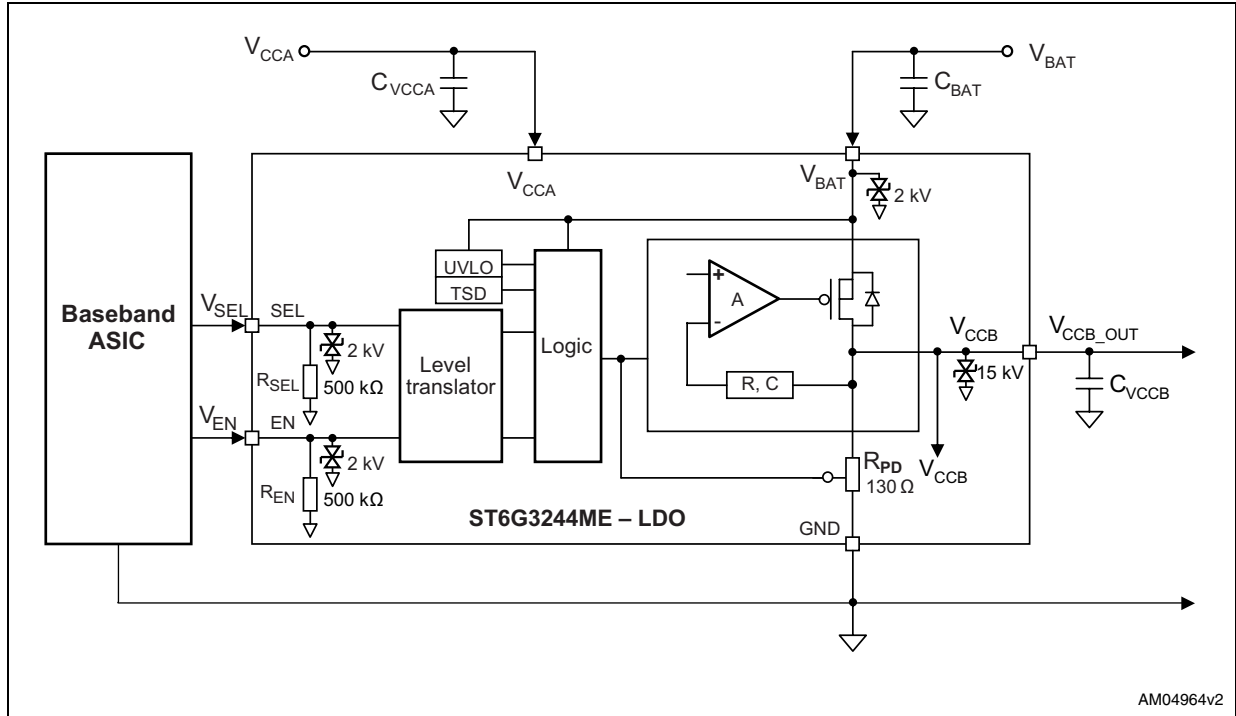


Table 13.  $V_{CCB}$  selection (B-side power supply voltage), EN pin control

EN	SEL	$V_{CCB}^{(1)}$ (V)
0	x	0 <sup>(2)</sup>
1	0	2.9
1	1	1.8

- $V_{CCB}$  is an internal B-side I/O power supply, tied to the  $V_{CCB\_OUT}$  pin for external decoupling capacitor.  $V_{CCB}$  supply voltage can also be used externally.
- Pulled down to GND by  $R_{PD}$ . When  $V_{CCB} = 0$  V, no additional leakage is seen on  $V_{CCA}$ .

**Table 14. LDO static parameters ( $V_{EN} = V_{CCA}$  unless otherwise specified)**

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$V_{CCB\_OUT}$	Regulated output voltage ( $V_{CCB}$ )	$V_{BAT} = 3 \text{ to } 5 \text{ V}$ , $SEL = 0$ $I_{OUT} = 0.1 \text{ to } 50 \text{ mA}$ , $T_J = -40 \text{ to } 125 \text{ }^\circ\text{C}$		2.75	2.90	3.05	V
		$V_{BAT} = 3 \text{ to } 5 \text{ V}$ , $SEL = 1$ $I_{OUT} = 0.1 \text{ to } 50 \text{ mA}$ , $T_J = -40 \text{ to } 125 \text{ }^\circ\text{C}$		1.71	1.8	1.89	
$V_{DO}$	Drop-out voltage	$V_{CCB\_OUT} \text{ (nom)} - 100 \text{ mV}$ $T_J = -40 \text{ to } 85 \text{ }^\circ\text{C}$ $SEL = 0$	$I_{OUT} = 50 \text{ mA}$		25	40	mV
$I_{OUT}$	$V_{CCB\_OUT}$ output current					50	mA
TSD	Thermal shutdown temperature	$V_{BAT} = 3.4 \text{ V}$	Shutdown (temp. $\uparrow$ )		150		$^\circ\text{C}$
			Reset (temp. $\downarrow$ )		130		
			Hysteresis		20		
UVLO	Undervoltage lockout	$T_J = -40 \text{ to } 125 \text{ }^\circ\text{C}$	Shutdown ( $V_{BAT} \downarrow$ )	2.3	2.5	2.7	V
			Reset ( $V_{BAT} \uparrow$ )	2.35	2.55	2.75	V
			Hysteresis		50		mV

Note: Level translator deactivated, \*.dir = 0, CLK.h =  $V_{CCA}$ , all other pins floating.

**Table 15. LDO dynamic parameters ( $V_{EN} = V_{CCA}$  unless otherwise specified)**

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
PSRR	Power supply rejection ratio	$V_{BAT} = 3.4 \text{ V}$ $I_{OUT} = 50 \text{ mA}$ $T_J = 25 \text{ }^\circ\text{C}$ $C_{VCCB} = 2.2 \text{ } \mu\text{F}$ , $ESR = 5 \text{ m}\Omega$	$f = 1 \text{ kHz}$		40		dB
			$f = 10 \text{ kHz}$		30		
$t_{START}$	Settling time	$V_{CCB\_OUT} \uparrow 95\% \text{ nom.}$ , $V_{BAT} = 5 \text{ V}$ , $I_{OUT} = 50 \text{ mA}$ , $T_J = -40 \text{ }^\circ\text{C to } 125 \text{ }^\circ\text{C}$ , $C_{VCCB} = 1 \text{ } \mu\text{F}$ , enable L $\rightarrow$ H, $SEL = 0$			30	100	$\mu\text{s}$
					30	100	
$t_{STOP}$	Discharge time	$V_{CCB\_OUT} \downarrow 10\% \text{ nom.}$ , $V_{BAT} = 3.4 \text{ V}$ , $I_{OUT} = 1 \text{ mA}$ , $T_J = 25 \text{ }^\circ\text{C}$ , $C_{VCCB} = 1 \text{ } \mu\text{F}$ , enable H $\rightarrow$ L, $SEL = 0$			0.6	1	ms
					0.6	1	

## 8 SD Card specification compliance

The ST6G3244ME is designed to be compliant with SD Card specifications. The reference standards used include:

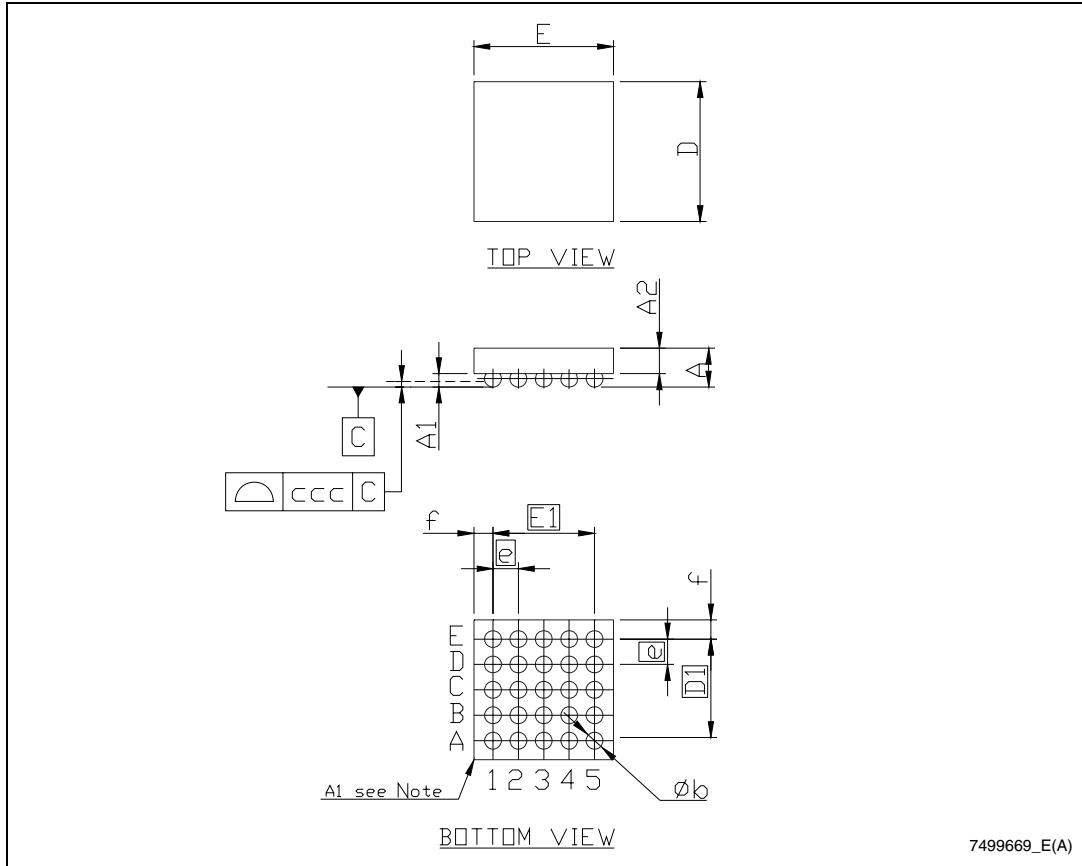
- SD Card Specification v3.00 (SDR12, SDR25, DDR50)
- SD Card Specification v2.00

The clock and data channels are designed to meet a 60 MHz clock rate and 120 Mbps data rate respectively to support both SDR and DDR modes.

## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 11. Package outline for Flip Chip 25 (2 mm x 2 mm x 0.605 mm, 0.4 mm pitch)



7499669\_E(A)

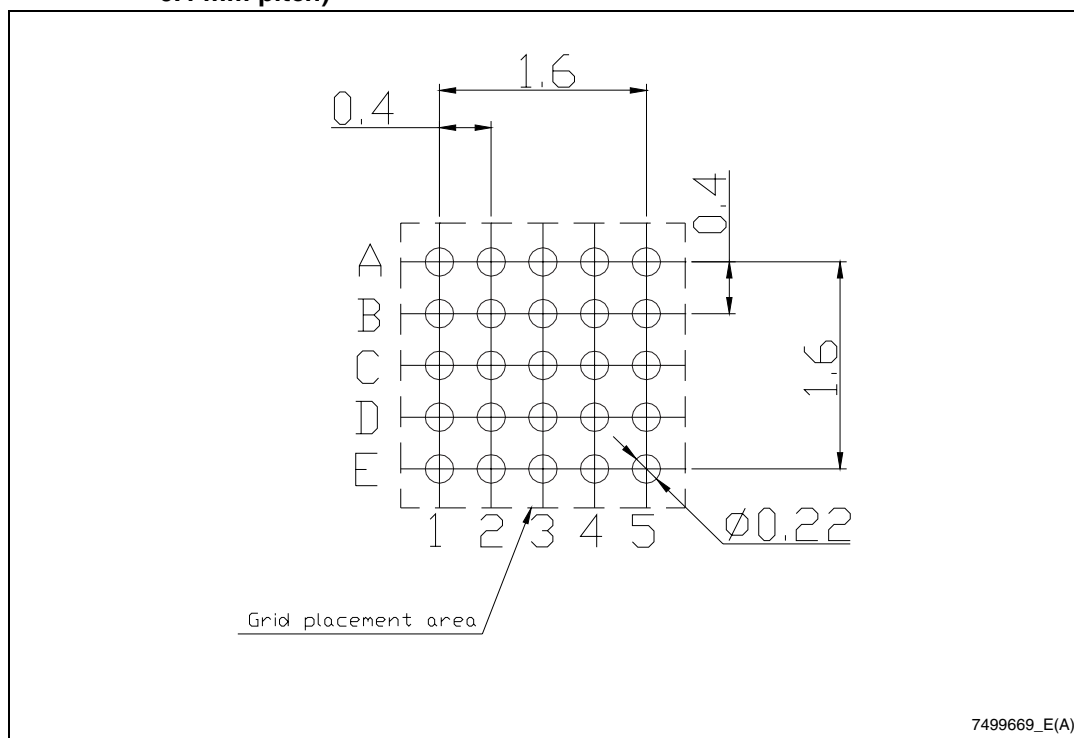
Note: The terminal A1 is on the top side of the package identified by a circular dot - typically 0.5 mm in diameter.

Table 16. Package mechanical data for Flip Chip 25 (2 mm x 2 mm x 0.605 mm, 0.4 mm pitch)

Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.560	0.605	0.650
A1	0.180	0.205	0.230
A2	0.380	0.400	0.420
b	0.230	0.255	0.280
D	1.985	2.00	2.015
D1	1.59	1.60	1.61
E	1.985	2.00	2.015
E1	1.59	1.60	1.61
e	0.36	0.40	0.44
f	0.190	0.200	0.210
ccc			0.05



Figure 12. Footprint recommendation for Flip Chip 25 (2 mm x 2 mm x 0.605 mm, 0.4 mm pitch)



## 10 Tape and reel information

**Figure 13. Pin 1 orientation in tape**

