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ST72321xx-Auto

8-bit MCU for automotive with 32/60 Kbyte Flash/ROM, ADC, 5 timers, SPI, SCI, I2C interface

Features

Memories

- 32 to 60 Kbyte dual voltage High Density Flash (HDFlash) or ROM ROM with readout protection capability. In-application programming and in-circuit programming for HDFlash devices
- 1 to 2 Kbyte RAM
- HDFlash endurance: 100 cycles, data retention 20 years

Clock, reset and supply management

- Enhanced low voltage supervisor (LVD) for main supply and auxiliary voltage detector (AVD) with interrupt capability
- Clock sources: crystal/ceramic resonator oscillators, internal RC oscillator and bypass for external clock
- PLL for 2x frequency multiplication
- 4 power saving modes: Halt, Active Halt, Wait and Slow

Interrupt management

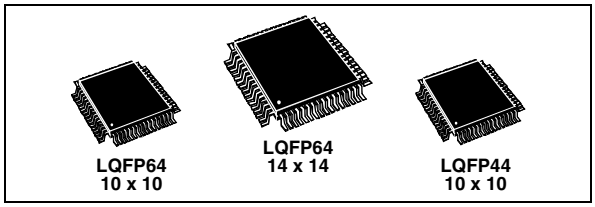
- Nested interrupt controller
- 14 interrupt vectors plus TRAP and RESET
- Top Level Interrupt (TLI) pin on 64-pin devices
- 15 external interrupt lines (on 4 vectors)

1 analog peripheral

- 10-bit ADC with up to 16 input ports

Up to 48 I/O ports

- 48//32 multifunctional bidirectional I/O lines
- 34//22 alternate function lines
- 16//12 high sink outputs



5 timers

- Main clock controller with Real-time base, Beep and Clock-out capabilities
- Configurable watchdog timer
- Two 16-bit timers with 2 input captures, 2 output compares, external clock input on 1 timer, PWM and pulse generator modes
- 8-bit PWM auto-reload timer with 2 input captures, 4 PWM outputs, output compare and time base interrupt, external clock with event detector

3 communications interfaces

- SPI synchronous serial interface
- SCI asynchronous serial interface
- I^2C multimaster interface

Instruction set

- 8-bit data manipulation
- 63 basic instructions
- 17 main addressing modes
- 8x8 unsigned multiply instruction

Development tools

- Full hardware/software development package, ICT capability

Table 1. Device summary

Reference	Part number
ST72321xx-Auto	ST72321AR6-Auto, ST72321R6-Auto, ST72321AR7-Auto, ST72321J7-Auto, ST72321R7-Auto ST72321AR9-Auto, ST72321J9-Auto, ST72321R9-Auto

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1 Description

The ST72321xx-Auto Flash and ROM devices are members of the ST7 microcontroller family designed for mid-range automotive applications running from 3.8 to 5.5V.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with Flash program memory. The ST7 family architecture offers both power and flexibility to software developers, enabling the design of highly efficient and compact application code.

The on-chip peripherals include an A/D converter, a PWM autoreload timer, two general purpose timers, I^2C, SPI, SCI interfaces.

For power economy, the microcontroller can switch dynamically into Wait, Slow, Active Halt or Halt mode when the application is in idle or standby state.

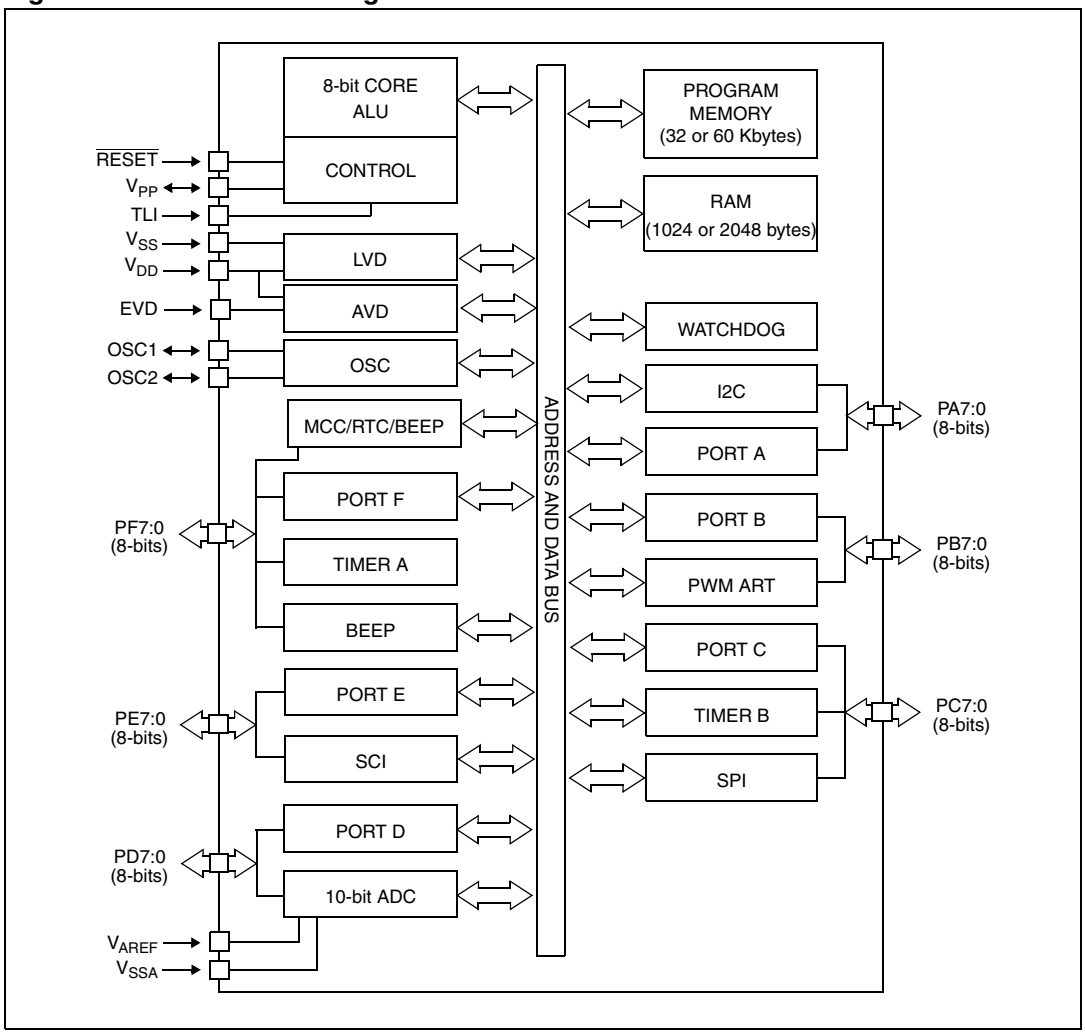
Table 2. Product overview

Reference	Program memory	RAM (stack)	Voltage range	Temp. range	Package
ST72321R9-Auto	60 Kbytes Flash/ROM	2048 (256) bytes	3.8V to 5.5V	Up to -40°C to 125°C	LQFP64 14x14
ST72321AR9-Auto					LQFP64 10x10
ST72321J9-Auto					LQFP48 10x10
ST72321R7-Auto	48 Kbytes Flash/ROM	1536 (256) byte			LQFP64 14x14
ST72321AR7-Auto					LQFP64 10x10
ST72321J7-Auto					LQFP48 10x10
ST72321R6-Auto	32 Kbytes Flash/ROM	1024 (256) byte			LQFP64 14x14
ST72321AR6-Auto					LQFP64 10x10

Typical applications include

- all types of car body applications such as window lift, DC motor control, rain sensors
- safety microcontroller in airbag and engine management applications
- auxiliary functions in car radios

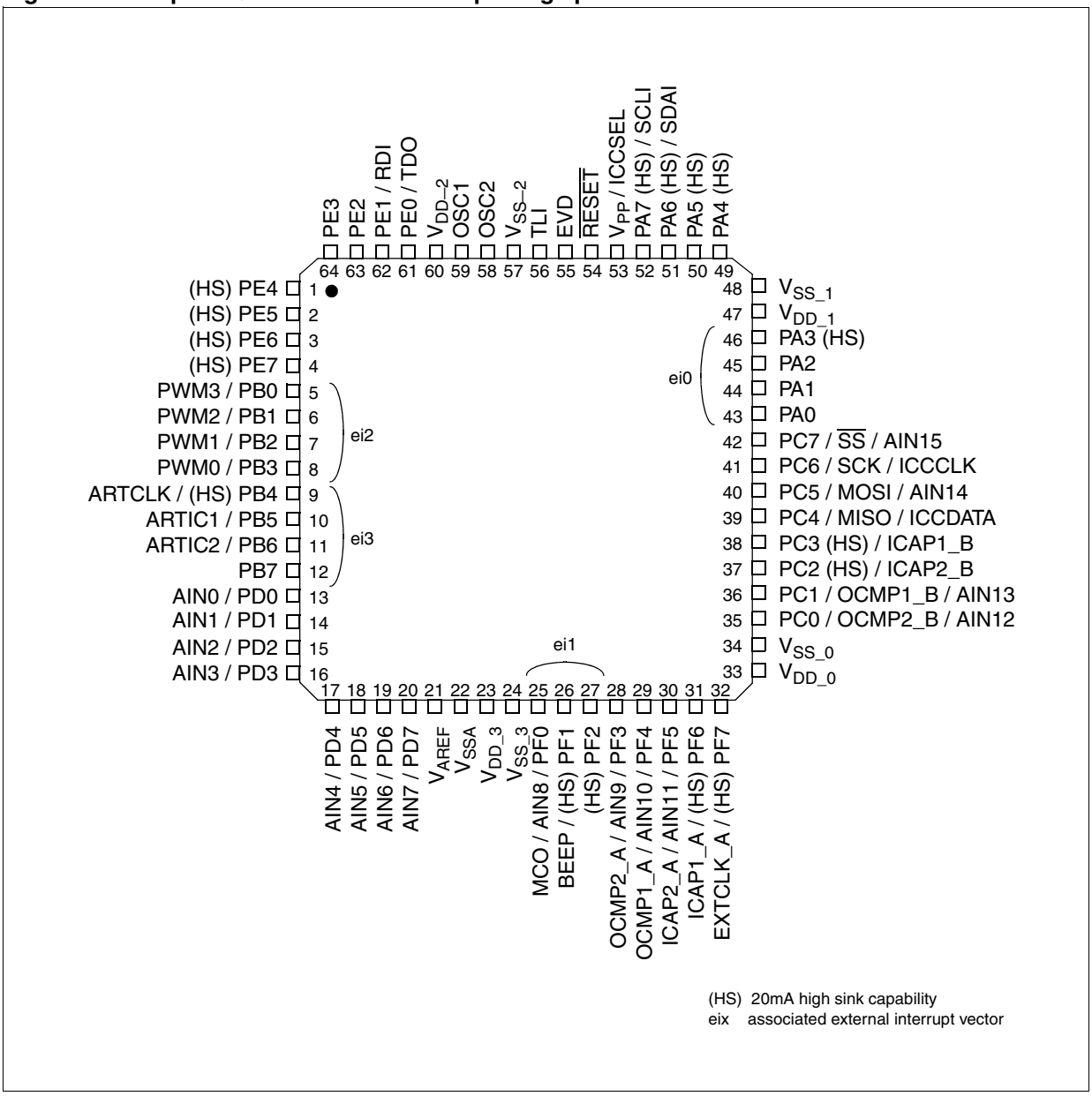
Figure 1. Device block diagram



2 Package pinout and pin description

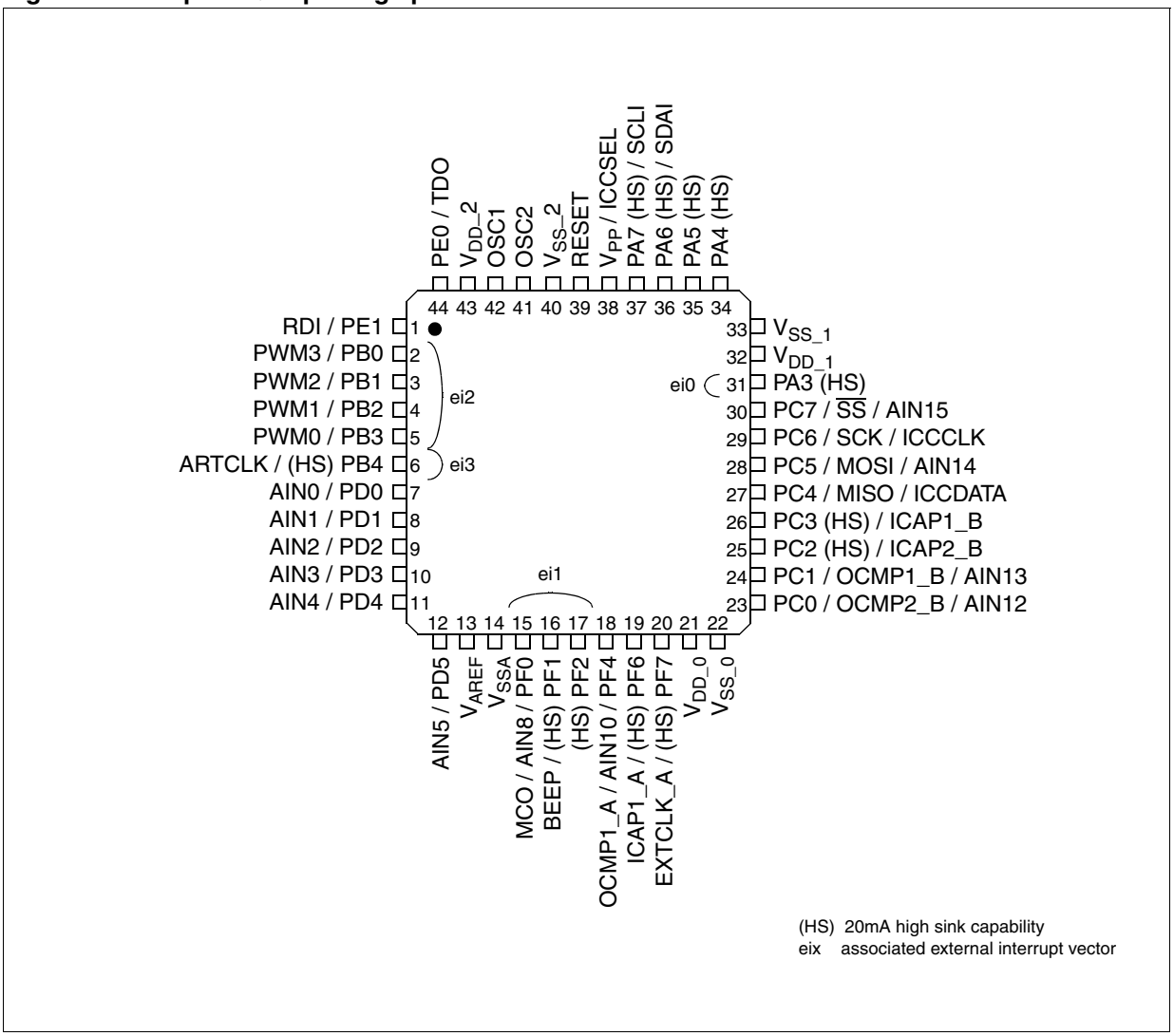
2.1 Package pinout

Figure 2. 64-pin LQFP 14x14 and 10x10 package pinout



For external pin connection guidelines, refer to *Section 19: Electrical characteristics*.

Figure 3. 44-pin LQFP package pinout



2.2 Pin description

In the device pin description table, the RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Refer to *Section 9: I/O ports on page 70* for more details on the software configuration of the I/O ports.

Table 3. Device pin description

Pin No.		Pin name	Type	Level		Port						Main function (after reset)	Alternate function
						Input				Output			
LQFP64	LQFP44			Input	Output	float	wpu	int	ana	OD	PP		
1	-	PE4(HS)	I/O	C_T	HS	**X**	X			X	X	Port E4	
2	-	PE5(HS)	I/O	C_T	HS	**X**	X			X	X	Port E5	
3	-	PE6(HS)	I/O	C_T	HS	**X**	X			X	X	Port E6	
4	-	PE7(HS)	I/O	C_T	HS	**X**	X			X	X	Port E7	
5	2	PB0/PWM3	I/O	C_T		**X**	ei2			X	X	Port B0	PWM Output 3
6	3	PB1/PWM2	I/O	C_T		**X**	ei2			X	X	Port B1	PWM Output 2
7	4	PB2/PWM1	I/O	C_T		**X**	ei2			X	X	Port B2	PWM Output 1
8	5	PB3/PWM0	I/O	C_T		**X**		ei2		X	X	Port B3	PWM Output 0
9	6	PB4(HS)/ARTCLK	I/O	C_T	HS	**X**	ei3			X	X	Port B4	PWM-ART External Clock
10	-	PB5 / ARTIC1	I/O	C_T		**X**	ei3			X	X	Port B5	PWM-ART Input Capture 1
11	-	PB6 / ARTIC2	I/O	C_T		**X**	ei3			X	X	Port B6	PWM-ART Input Capture 2
12	-	PB7	I/O	C_T		**X**		ei3		X	X	Port B7	
13	7	PD0/AIN0	I/O	C_T		**X**	X		X	X	X	Port D0	ADC Analog Input 0
14	8	PD1/AIN1	I/O	C_T		**X**	X		X	X	X	Port D1	ADC Analog Input 1
15	9	PD2/AIN2	I/O	C_T		**X**	X		X	X	X	Port D2	ADC Analog Input 2
16	10	PD3/AIN3	I/O	C_T		**X**	X		X	X	X	Port D3	ADC Analog Input 3
17	11	PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4
18	12	PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5
19	-	PD6/AIN6	I/O	C_T		**X**	X		X	X	X	Port D6	ADC Analog Input 6
20	-	PD7/AIN7	I/O	C_T		**X**	X		X	X	X	Port D7	ADC Analog Input 7
21	13	V_{AREF}(1)	I									Analog Reference Voltage for ADC	
22	14	V_{SSA}(1)	S									Analog Ground Voltage	
23	-	V_{DD_3}(1)	S									Digital Main Supply Voltage	
24	-	V_{SS_3}(1)	S									Digital Ground Voltage	

Table 3. Device pin description (continued)

Pin No.		Pin name	Type	Level		Port						Main function (after reset)	Alternate function	
						Input				Output				
LQFP64	LQFP44			Input	Output	float	wpu	int	ana	OD	PP			
25	15	PF0/MCO/AIN8	I/O	C_T		**X**	ei1		X	X	X	Port F0	Main clock out (f_{OSC}/2)	ADC Analog Input 8
26	16	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
27	17	PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
28	-	PF3/OCMP2_A/ AIN9	I/O	C_T		**X**	X		X	X	X	Port F3	Timer A Output Compare 2	ADC Analog Input 9
29	18	PF4/OCMP1_A/ AIN10	I/O	C_T		**X**	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
30	-	PF5/ICAP2_A/ AIN11	I/O	C_T		**X**	X		X	X	X	Port F5	Timer A Input Capture 2	ADC Analog Input 11
31	19	PF6(HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
32	20	PF7(HS)/ EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
33	21	V_{DD_0}(1)	S									Digital Main Supply Voltage		
34	22	V_{SS_0}(1)	S									Digital Ground Voltage		
35	23	PC0/OCMP2_B/ AIN12	I/O	C_T		**X**	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
36	24	PC1/OCMP1_B/ AIN13	I/O	C_T		**X**	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13
37	25	PC2(HS)/ ICAP2_B	I/O	C_T	HS	**X**	X			X	X	Port C2	Timer B Input Capture 2	
38	26	PC3(HS)/ ICAP1_B	I/O	C_T	HS	**X**	X			X	X	Port C3	Timer B Input Capture 1	
39	27	PC4/MISO/ ICCDATA	I/O	C_T		**X**	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
40	28	PC5/MOSI/AIN14	I/O	C_T		**X**	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14

Table 3. Device pin description (continued)

Pin No.		Pin name	Type	Level		Port						Main function (after reset)	Alternate function	
						Input				Output				
LQFP64	LQFP44			Input	Output	float	wpu	int	ana	OD	PP			
41	29	PC6/SCK/ICCCLK	I/O	C_T		**X**	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output
													Caution: Negative current injection not allowed on this pin (Flash devices only)	
42	30	PC7/$\overline{SS}$/AIN15	I/O	C_T		**X**	X		X	X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
43	-	PA0	I/O	C_T		**X**	ei0			X	X	Port A0		
44	-	PA1	I/O	C_T		**X**	ei0			X	X	Port A1		
45	-	PA2	I/O	C_T		**X**	ei0			X	X	Port A2		
46	31	PA3(HS)	I/O	C_T	HS	**X**		ei0		X	X	Port A3		
47	32	V_{DD_1} (1)	S									Digital Main Supply Voltage		
48	33	V_{SS_1} (1)	S									Digital Ground Voltage		
49	34	PA4(HS)	I/O	C_T	HS	**X**	X			X	X	Port A4		
50	35	PA5(HS)	I/O	C_T	HS	**X**	X			X	X	Port A5		
51	36	PA6(HS)/SDAI	I/O	C_T	HS	**X**				T		Port A6	I^2C Data	
52	37	PA7(HS)/SCLI	I/O	C_T	HS	**X**				T		Port A7	I^2C Clock	
53	38	V_{PP}/ ICCSEL	I									Must be tied low. In Flash programming mode, this pin acts as the programming voltage input V_{PP}. See *Section 19.9.2: ICCSEL/VPP pin* for more details. High voltage must not be applied to ROM devices.		
54	39	$\overline{RESET}$	I/O	C_T								Top priority non-maskable interrupt		
55	-	EVD	I	A								External voltage detector		
56	-	TLI	I	C_T				X				Top level interrupt input pin		
57	40	V_{SS_2} (1)	S									Digital Ground Voltage		
58	41	OSC2(2)	I/O									Resonator oscillator inverter output		
59	42	OSC1(2)	I									External clock input or Resonator oscillator inverter input		
60	43	V_{DD_2} (1)	S									Digital Main Supply Voltage		
61	44	PE0/TDO	I/O	C_T		**X**	X			X	X	Port E0	SCI Transmit Data Out	
62	1	PE1/RDI	I/O	C_T		**X**	X			X	X	Port E1	SCI Receive Data In	

Table 3. Device pin description (continued)

Pin No.		Pin name	Type	Level		Port						Main function (after reset)	Alternate function
						Input				Output			
LQFP64	LQFP44			Input	Output	float	wpu	int	ana	OD	PP		
63	-	PE2 (Flash device)	I/O	C_T			X					Port E2 **Caution:** In Flash devices this port is always input with weak pull-up.	
		PE2 (ROM device)				X				X	X	Port E2 **Caution:** In ROM devices, no weak pull-up present on this port. In LQFP44 this pin is not connected to an internal pull-up like other unbonded pins. It is recommended to configure it as output push-pull to avoid added current consumption.	
64	-	PE3	I/O	C_T		X	X			X	X	Port E3	

1. It is mandatory to connect all available V_{DD} and V_{AREF} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.
2. OSC1 and OSC2 pins connect a crystal/ceramic resonator or an external source to the on-chip oscillator; see *Section 6: Supply, reset and clock management* and *Section 19.5: Clock and timing characteristics on page 195* for more details.

Legend / Abbreviations for *Table 3*:

Type: I = input, O = output, S = supply

Input level: A = dedicated analog input

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$; C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt[a], ana = analog
- Output: OD = open-drain[b], PP = push-pull

a. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, otherwise the configuration is floating interrupt input.

b. In the open-drain output column, “T” defines a true open-drain I/O (P-Buffer and protection diode to V_{DD} are not implemented). See *Section 9: I/O ports on page 70* and *Section 19.8: I/O port pin characteristics on page 203* for more details.