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ST72324Bxx

8-bit MCU, 3.8 to 5.5 V operating range with 8 to 32 Kbyte Flash/ROM, 10-bit ADC, 4 timers, SPI, SCI

Features

Memories

- 8 to 32 Kbyte dual voltage High Density Flash (HDFlash) or ROM with readout protection capability. In-application programming and In-circuit programming for HDFlash devices
- 384 bytes to 1 Kbyte RAM
- HDFlash endurance: 1 kcycle at 55 °C, data retention 40 years at 85 °C

Clock, reset and supply management

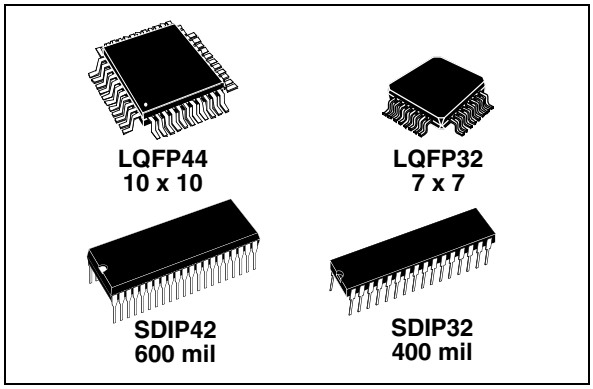
- Enhanced low voltage supervisor (LVD) with programmable reset thresholds and auxiliary voltage detector (AVD) with interrupt capability
- Clock sources: crystal/ceramic resonator oscillators, int. RC osc. and ext. clock input
- PLL for 2x frequency multiplication
- 4 power saving modes: Slow, Wait, Active-halt, and Halt

Interrupt management

- Nested interrupt controller. 10 interrupt vectors plus TRAP and RESET. 9/6 ext. interrupt lines (on 4 vectors)

Up to 32 I/O ports

- 32/24 multifunctional bidirectional I/Os, 22/17 alternate function lines, 12/10 high sink outputs



4 timers

- Main clock controller with real-time base, Beep and clock-out capabilities
- Configurable watchdog timer
- 16-bit Timer A with 1 input capture, 1 output compare, ext. clock input, PWM and pulse generator modes
- 16-bit Timer B with 2 input captures, 2 output compares, PWM and pulse generator modes

2 communication interfaces

- SPI synchronous serial interface
- SCI asynchronous serial interface

1 analog peripheral (low current coupling)

- 10-bit ADC with up to 12 input ports

Development tools

- In-circuit testing capability

Table 1. Device summary

Device	Memory	RAM (stack)	Voltage range	Temp. range	Package
ST72324BK2	Flash/ROM 8 Kbytes	384 (256) bytes	3.8 to 5.5 V	up to -40 to 125 °C	LQFP32 7x7/ SDIP32
ST72324BK4	Flash/ROM 16 Kbytes	512 (256) bytes			
ST72324BK6	Flash/ROM 32 Kbytes	1024 (256) bytes			
ST72324BJ2	Flash/ROM 8 Kbytes	384 (256) bytes			LQFP44 10x10/ SDIP42
ST72324BJ4	Flash/ROM 16 Kbytes	512 (256) bytes			
ST72324BJ6	Flash/ROM 32 Kbytes	1024 (256) bytes			

Contents

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1 Description

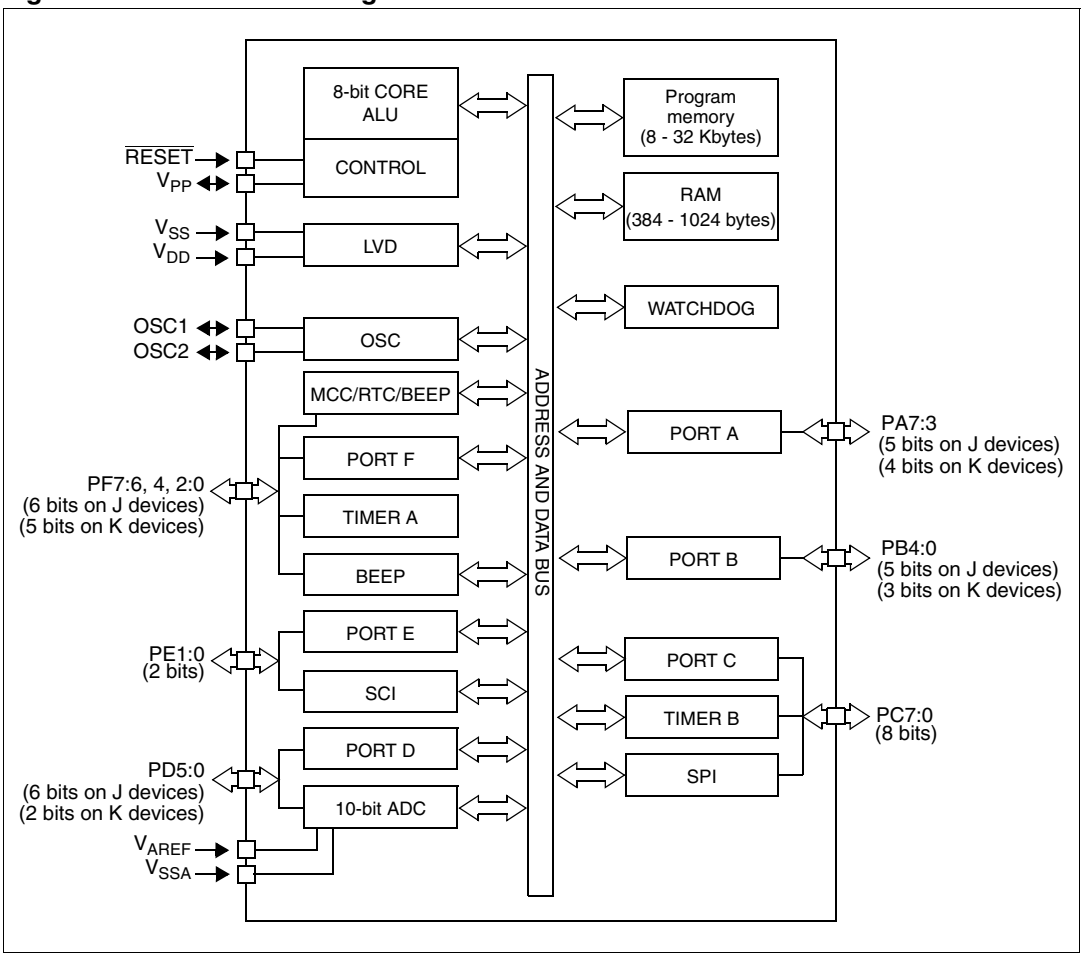
The ST72324Bxx devices are members of the ST7 microcontroller family designed for mid-range applications running from 3.8 to 5.5 V. Different package options offer up to 32 I/O pins.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with Flash or ROM program memory. The ST7 family architecture offers both power and flexibility to software developers, enabling the design of highly efficient and compact application code.

The on-chip peripherals include an A/D converter, two general purpose timers, an SPI interface and an SCI interface. For power economy, the microcontroller can switch dynamically into, Slow, Wait, Active-halt or Halt mode when the application is in idle or stand-by state.

Typical applications include consumer, home, office and industrial products.

Figure 1. Device block diagram



2 Pin description

Figure 2. 44-pin LQFP package pinout

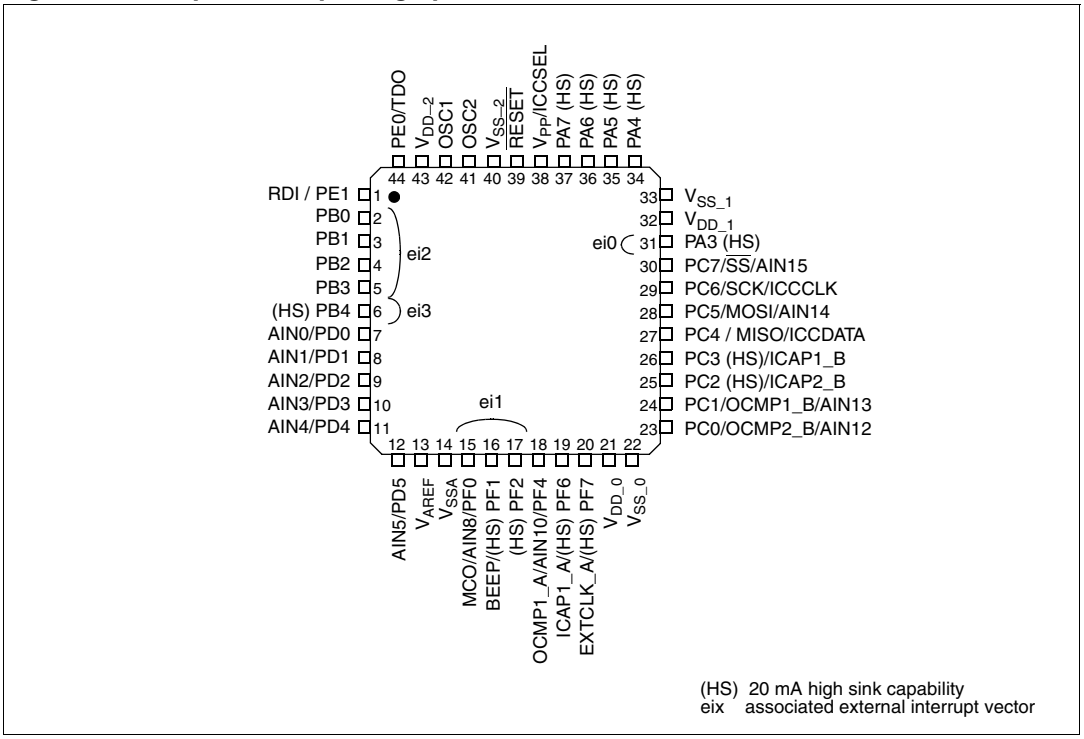


Figure 3. 42-pin SDIP package pinout

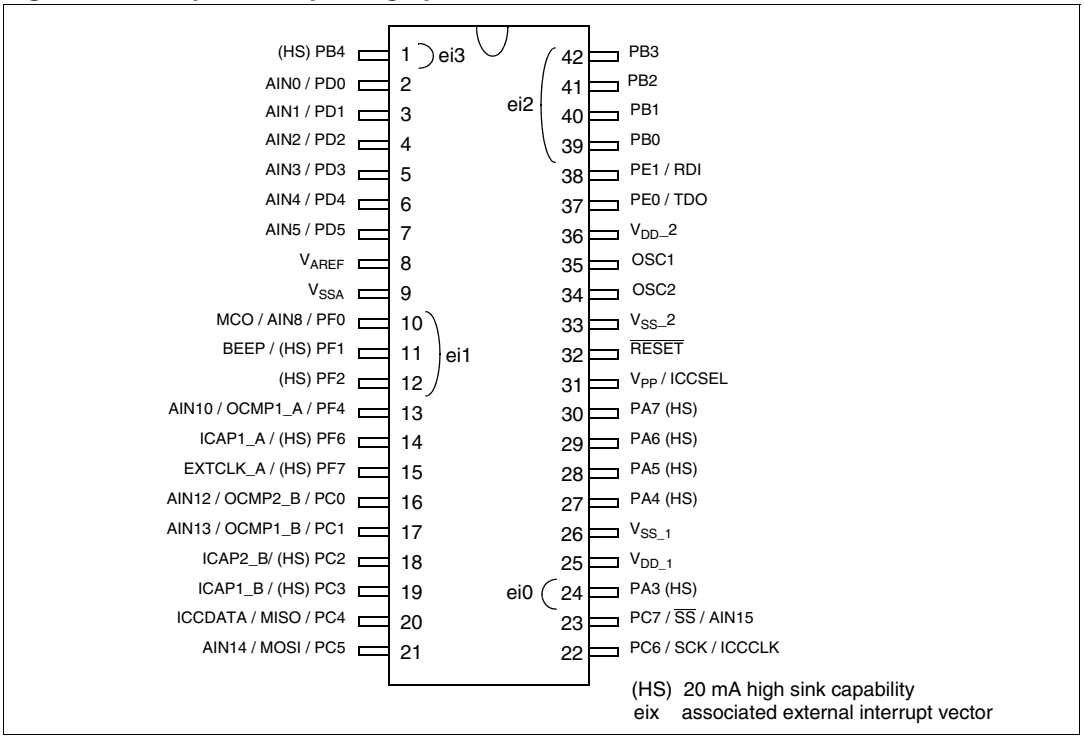


Figure 4. 32-pin LQFP package pinout

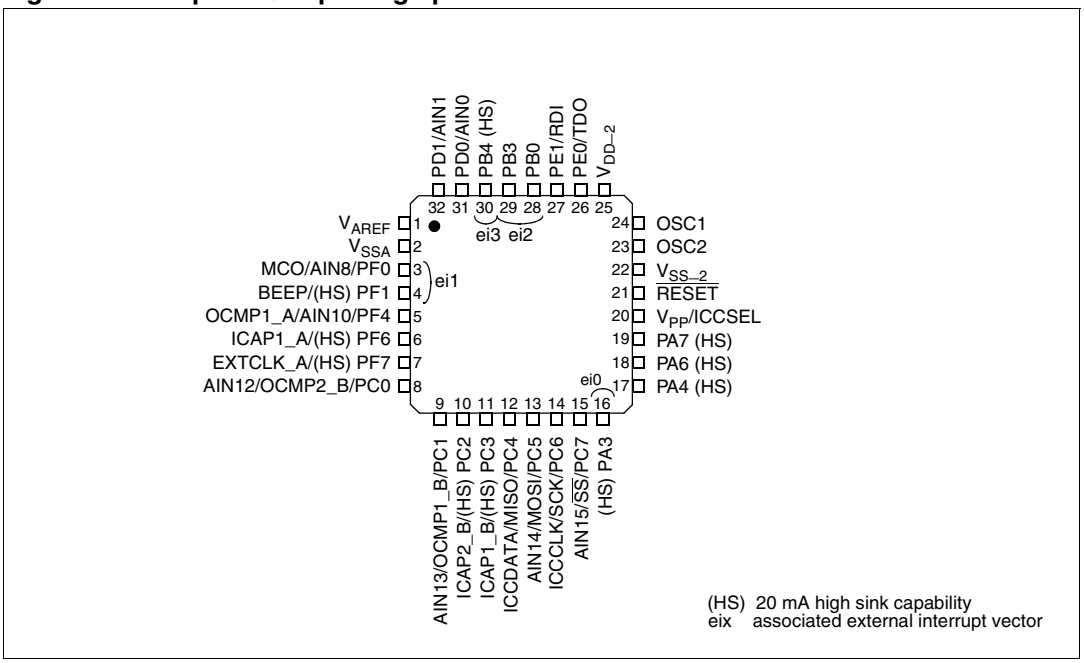
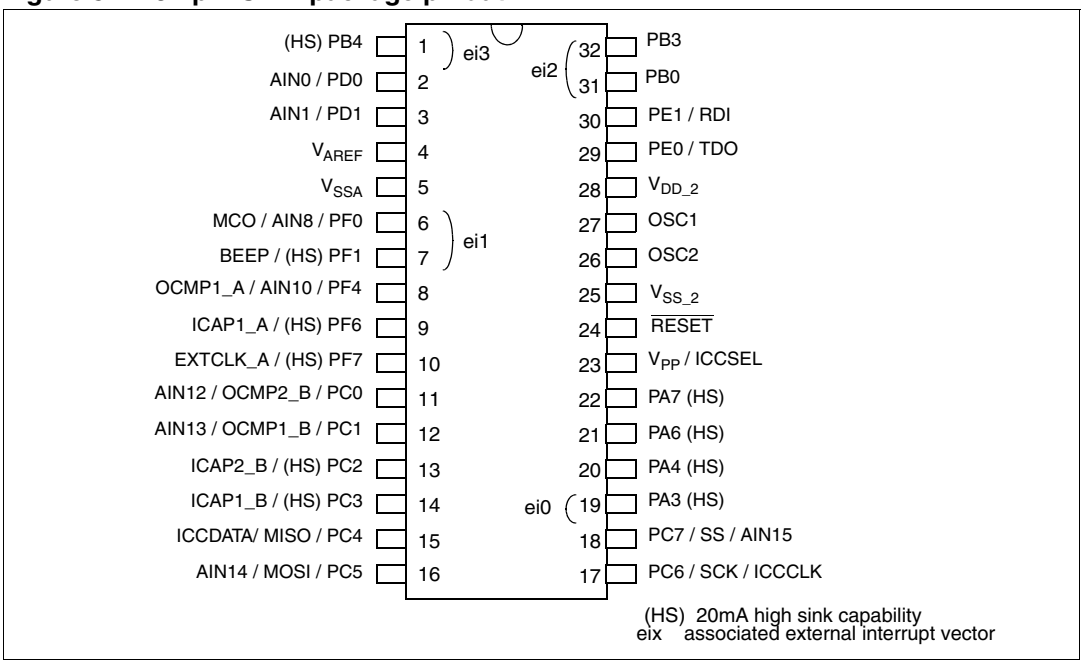


Figure 5. 32-pin SDIP package pinout



See *Section 12: Electrical characteristics on page 141* for external pin connection guidelines.

Refer to *Section 9: I/O ports on page 58* for more details on the software configuration of the I/O ports.

The reset configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Legend / Abbreviations for *Table 2:*

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C = CMOS $0.3V_{DD}/0.7_{DD}$
C_T = CMOS $0.3V_{DD}/0.7_{DD}$ with input trigger

Output level: HS = 20 mA high sink (on N-buffer only)

Port and control configuration:

Input: float = floating, wpu = weak pull-up, int = interrupt[a], ana = analog ports

Output: OD = open drain[b], PP = push-pull

Table 2. Device pin description

Pin No.				Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
								Input				Output				
LQFP44	SDIP42	LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
6	1	30	1	PB4 (HS)	I/O	C_T	HS	X	ei3			X	X	Port B4		
7	2	31	2	PD0/AIN0	I/O	C_T		X	X		X	X	X	Port D0	ADC Analog Input 0	
8	3	32	3	PD1/AIN1	I/O	C_T		X	X		X	X	X	Port D1	ADC Analog Input 1	
9	4			PD2/AIN2	I/O	C_T		X	X		X	X	X	Port D2	ADC Analog Input 2	
10	5			PD3/AIN3	I/O	C_T		X	X		X	X	X	Port D3	ADC Analog Input 3	
11	6			PD4/AIN4	I/O	C_T		X	X		X	X	X	Port D4	ADC Analog Input 4	
12	7			PD5/AIN5	I/O	C_T		X	X		X	X	X	Port D5	ADC Analog Input 5	
13	8	1	4	V_{AREF}[1]	S									Analog Reference Voltage for ADC		
14	9	2	5	V_{SSA}[1]	S									Analog Ground Voltage		
15	10	3	6	PF0/MCO/AIN8	I/O	C_T		X	ei1		X	X	X	Port F0	Main clock out (f_{CPU})	ADC Analog Input 8
16	11	4	7	PF1 (HS)/BEEP	I/O	C_T	HS	X	ei1			X	X	Port F1	Beep signal output	
17	12			PF2 (HS)	I/O	C_T	HS	X	ei1			X	X	Port F2		
18	13	5	8	PF4/OCMP1_A/ AIN10	I/O	C_T		X	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
19	14	6	9	PF6 (HS)/ICAP1_A	I/O	C_T	HS	X	X			X	X	Port F6	Timer A Input Capture 1	
20	15	7	10	PF7 (HS)/ EXTCLK_A	I/O	C_T	HS	X	X			X	X	Port F7	Timer A External Clock Source	

a. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

b. In the open drain output column, ‘T’ *defines a true open drain I/O (P-Buffer and protection diode to V_{DD} are not implemented). See Section 9: I/O ports and Section 12.9: I/O port pin characteristics for more details.*

Table 2. Device pin description (continued)

Pin No.				Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
								Input				Output				
LQFP44	SDIP42	LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
21				V_{DD_0} (1)	S									Digital Main Supply Voltage		
22				V_{SS_0} (1)	S									Digital Ground Voltage		
23	16	8	11	PC0/OCMP2_B /AIN12	I/O	C_T		X	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
24	17	9	12	PC1/OCMP1_B /AIN13	I/O	C_T		X	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13
25	18	10	13	PC2 (HS)/ ICAP2_B	I/O	C_T	HS	X	X			X	X	Port C2	Timer B Input Capture 2	
26	19	11	14	PC3 (HS)/ ICAP1_B	I/O	C_T	HS	X	X			X	X	Port C3	Timer B Input Capture 1	
27	20	12	15	PC4/MISO/ICC DATA	I/O	C_T		X	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
28	21	13	16	PC5/MOSI/ AIN14	I/O	C_T		X	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
29	22	14	17	PC6/SCK/ ICCCLK	I/O	C_T		X	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output
30	23	15	18	PC7/$\overline{SS}$/AIN15	I/O	C_T		X	X		X	X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
31	24	16	19	PA3 (HS)	I/O	C_T	HS	X		ei 0		X	X	Port A3		
32	25			V_{DD_1} (1)	S									Digital Main Supply Voltage		
33	26			V_{SS_1} (1)	S									Digital Ground Voltage		
34	27	17	20	PA4 (HS)	I/O	C_T	HS	X	X			X	X	Port A4		
35	28			PA5 (HS)	I/O	C_T	HS	X	X			X	X	Port A5		
36	29	18	21	PA6 (HS)	I/O	C_T	HS	X				T		Port A6 (2)		
37	30	19	22	PA7 (HS)	I/O	C_T	HS	X				T		Port A7 (2)		
38	31	20	23	V_{PP} /ICCSEL	I									Must be tied low. In the flash programming mode, this pin acts as the programming voltage input V_{PP}. See *Section 12.10.2* for more details. High voltage must not be applied to ROM devices.		
39	32	21	24	RESET	I/O	C_T								Top priority non maskable interrupt.		
40	33	22	25	V_{SS_2} (1)	S									Digital Ground Voltage		

Table 2. Device pin description (continued)

Pin No.				Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function
								Input				Output			
LQFP44	SDIP42	LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP		
41	34	23	26	OSC2(3)	O									Resonator oscillator inverter output	
42	35	24	27	OSC1(3)	I									External clock input or Resonator oscillator inverter input	
43	36	25	28	V_{DD_2}(1)	S									Digital Main Supply Voltage	
44	37	26	29	PE0/TDO	I/O	C_T		X	X			X	X	Port E0	SCI Transmit Data Out
1	38	27	30	PE1/RDI	I/O	C_T		X	X			X	X	Port E1	SCI Receive Data In
2	39	28	31	PB0	I/O	C_T		X	ei2			X	X	Port B0	**Caution:** Negative current injection not allowed on this pin(4)
3	40			PB1	I/O	C_T		X	ei2			X	X	Port B1	
4	41			PB2	I/O	C_T		X	ei2			X	X	Port B2	
5	42	29	32	PB3	I/O	C_T		X		ei2		X	X	Port B3	

1. It is mandatory to connect all available V_{DD} and V_{REF} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.
2. On the chip, each I/O port has eight pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.
3. OSC1 and OSC2 pins connect a crystal/ceramic resonator, or an external source to the on-chip oscillator; see *Section 1: Description* and *Section 12.6: Clock and timing characteristics* for more details.
4. For details refer to *Section 12.9.1 on page 158*

3 Register and memory map

As shown in *Figure 6*, the MCU is capable of addressing 64 Kbytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, up to 1024 bytes of RAM and up to 32 Kbytes of user program memory. The RAM space includes up to 256 bytes for the stack from 0100h to 01FFh.

The highest address bytes contain the user reset and interrupt vectors.

Caution: Never access memory locations marked as 'Reserved'. Accessing a reserved area can have unpredictable effects on the device.

Figure 6. Memory map

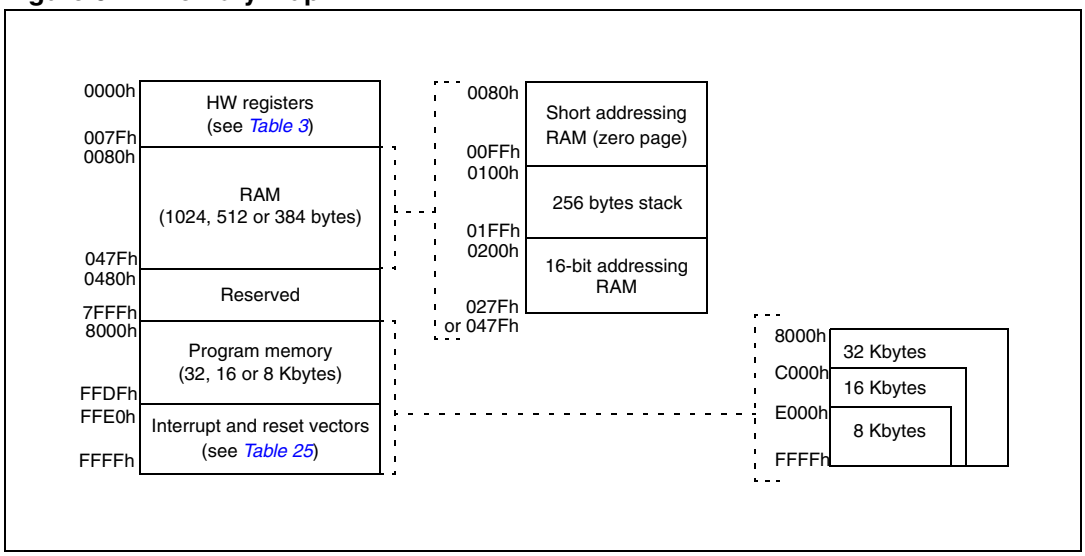


Table 3. Hardware register map

Address	Block	Register label	Register name	Reset status	Remarks
0000h 0001h 0002h	Port A(1)	PADR PADDR PAOR	Port A data register Port A data direction register Port A option register	00h(2) 00h 00h	R/W R/W R/W
0003h 0004h 0005h	Port B(1)	PBDR PBDDR PBOR	Port B data register Port B data direction register Port B option register	00h(2) 00h 00h	R/W R/W R/W
0006h 0007h 0008h	Port C	PCDR PCDDR PCOR	Port C data register Port C data direction register Port C option register	00h(2) 00h 00h	R/W R/W R/W
0009h 000Ah 000Bh	Port D(1)	PDADR PDDDR PDOR	Port D data register Port D data direction register Port D option register	00h(2) 00h 00h	R/W R/W R/W
000Ch 000Dh 000Eh	Port E(1)	PEDR PEDDR PEOR	Port E data register Port E data direction register Port E option register	00h(2) 00h 00h	R/W R/W(1) R/W(1)

Table 3. Hardware register map (continued)

Address	Block	Register label	Register name	Reset status	Remarks
000Fh 0010h 0011h	Port F(1)	PFDR PFDDR PFOR	Port F data register Port F data direction register Port F option register	00h(2) 00h 00h	R/W R/W R/W
0012h to 0020h	Reserved area (15 bytes)				
0021h 0022h 0023h	SPI	SPIDR SPICR SPICSR	SPI data I/O register SPI control register SPI control/status register	xxh 0xh 00h	R/W R/W R/W
0024h 0025h 0026h 0027h	ITC	ISPR0 ISPR1 ISPR2 ISPR3	Interrupt software priority register 0 Interrupt software priority register 1 Interrupt software priority register 2 Interrupt software priority register 3	FFh FFh FFh FFh	R/W R/W R/W R/W
0028h		EICR	External interrupt control register	00h	R/W
0029h	Flash	FCSR	Flash control/status register	00h	R/W
002Ah	Watchdog	WDGCR	Watchdog control register	7Fh	R/W
002Bh	SI	SICSR	System integrity control/status register	000x 000xb	R/W
002Ch 002Dh	MCC	MCCSR MCCBCR	Main clock control/status register Main clock controller: beep control register	00h 00h	R/W R/W
002Eh to 0030h	Reserved area (3 bytes)				
0031h 0032h 0033h 0034h 0035h 0036h 0037h 0038h 0039h 003Ah 003Bh 003Ch 003Dh 003Eh 003Fh	Timer A	TACR2 TACR1 TACSR TAIC1HR TAIC1LR TAOC1HR TAOC1LR TACHR TACLR TAACHR TAACLR TAIC2HR TAIC2LR TAOC2HR TAOC2LR	Timer A control register 2 Timer A control register 1 Timer A control/status register Timer A input capture 1 high register Timer A input capture 1 low register Timer A output compare 1 high register Timer A output compare 1 low register Timer A counter high register Timer A counter low register Timer A alternate counter high register Timer A alternate counter low register Timer A input capture 2 high register Timer A input capture 2 low register Timer A output compare 2 high register Timer A output compare 2 low register	00h 00h xxxx x0xxb xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read only Read only R/W R/W Read only Read only Read only Read only Read only Read only R/W R/W
0040h	Reserved area (1 byte)				

Table 3. Hardware register map (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0041h	Timer B	TBCR2	Timer B control register 2	00h	R/W
0042h		TBCR1	Timer B control register 1	00h	R/W
0043h		TBCSR	Timer B control/status register	xxxx x0xxb	R/W
0044h		TBIC1HR	Timer B input capture 1 high register	xxh	Read only
0045h		TBIC1LR	Timer B input capture 1 low register	xxh	Read only
0046h		TBOC1HR	Timer B output compare 1 high register	80h	R/W
0047h		TBOC1LR	Timer B output compare 1 low register	00h	R/W
0048h		TBCHR	Timer B counter high register	FFh	Read only
0049h		TBCLR	Timer B counter low register	FCh	Read only
004Ah		TBACHR	Timer B alternate counter high register	FFh	Read only
004Bh		TBACLR	Timer B alternate counter low register	FCh	Read only
004Ch		TBIC2HR	Timer B input capture 2 high register	xxh	Read only
004Dh		TBIC2LR	Timer B input capture 2 low register	xxh	Read only
004Eh		TBOC2HR	Timer B output compare 2 high register	80h	R/W
004Fh		TBOC2LR	Timer B output compare 2 low register	00h	R/W
0050h	SCI	SCISR	SCI status register	C0h	Read only
0051h		SCIDR	SCI data register	xxh	R/W
0052h		SCIBRR	SCI baud rate register	00h	R/W
0053h		SCICR1	SCI control register 1	x000 0000b	R/W
0054h		SCICR2	SCI control register 2	00h	R/W
0055h		SCIERPR	SCI extended receive prescaler register	00h	R/W
0056h			Reserved area	---	
0057h		SCIETPR	SCI extended transmit prescaler register	00h	R/W
0058h to 006Fh	Reserved area (24 bytes)				
0070h	ADC	ADCCSR	Control/status register	00h	R/W
0071h		ADCDRH	Data high register	00h	Read only
0072h		ADCDRL	Data low register	00h	Read only
0073h 007Fh	Reserved area (13 bytes)				

1. The bits associated with unavailable pins must always keep their reset value.
2. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.

Legend: x = undefined, R/W = read/write

4 Flash program memory

4.1 Introduction

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a byte-by-byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (in-circuit programming) or IAP (in-application programming).

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (in-circuit programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (in-application programming). In this mode, all sectors, except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Readout protection
- Register Access Security System (RASS) to prevent accidental programming or erasing

4.3 Structure

The Flash memory is organized in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see *Table 4*). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see *Figure 7*). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 4. Sectors available in Flash devices

Flash size	Available sectors
4 Kbytes	Sector 0
8 Kbytes	Sectors 0, 1
>8 Kbytes	Sectors 0, 1, 2

4.3.1 Readout protection

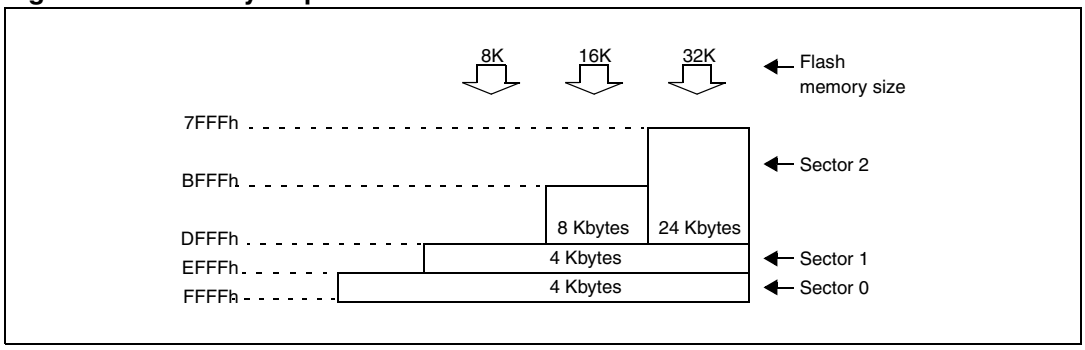
Readout protection, when selected, provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

In Flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased.

Readout protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the option list.

Figure 7. Memory map and sector address

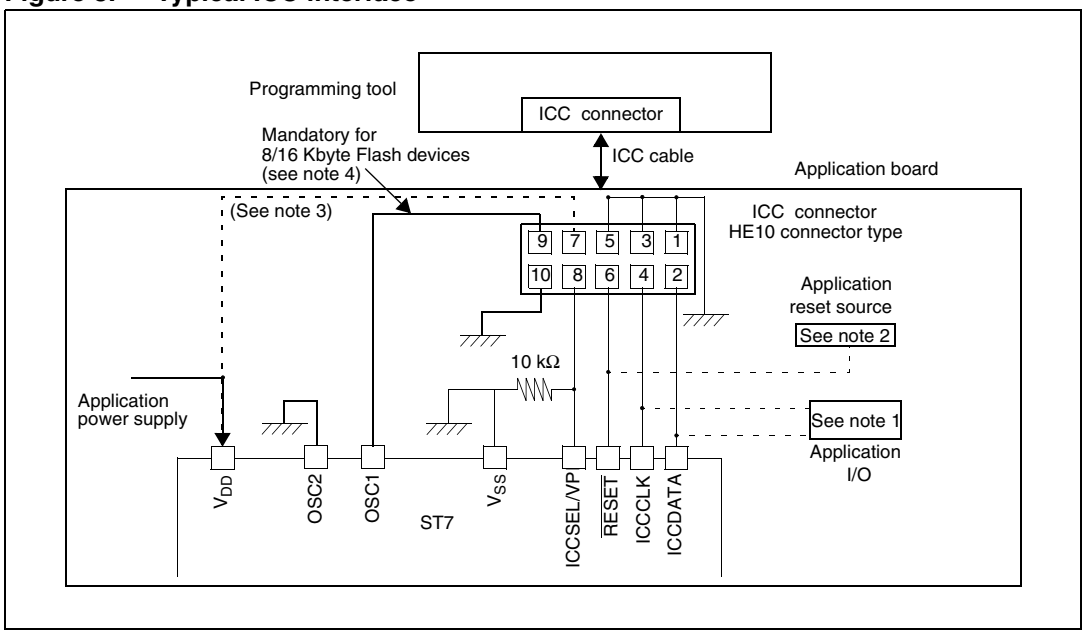


4.4 ICC interface

ICC needs a minimum of 4 and up to 6 pins to be connected to the programming tool (see *Figure 8*). These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input/output serial data pin
- ICCSEL/V_{PP}: programming voltage
- OSC1 (or OSCIN): main clock input for external source (optional)
- V_{DD}: application board power supply (optional, see *Figure 8*, Note 3)

Figure 8. Typical ICC interface



1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the programming tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.
2. During the ICC session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (PUSH-pull output or pull-up resistor <1 kΩ). A schottky diode can be used to isolate the application reset circuit in this case. When using a classical RC network with R>1kΩ or a reset management IC with open drain output and pull-up resistor >1 kΩ, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.
3. The use of Pin 7 of the ICC connector depends on the programming tool architecture. This pin must be connected when using most ST programming tools (it is used to monitor the application power supply). Please refer to the programming tool manual.
4. Pin 9 has to be connected to the OSC1 (OSCIN) pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC2 grounded in this case.

Caution: External clock ICC entry mode is mandatory in ST72F324B 8/16 Kbyte Flash devices. In this case pin 9 must be connected to the OSC1 (OSCIN) pin of the ST7 and OSC2 must be grounded. 32 Kbyte Flash devices may use external clock or application clock ICC entry mode.