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ST72344xx, ST72345xx

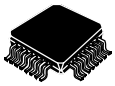
8-bit MCU with up to 16 Kbytes Flash memory, 10-bit ADC, two 16-bit timers, two I2C, SPI, SCI

Datasheet – production data

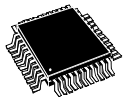
Features

- Memories
  - up to 16 Kbytes Program memory: single voltage extended Flash (XFlash) with read-out and write protection, in-circuit and in-application programming (ICP and IAP). 10,000 write/erase cycles guaranteed, data retention: 20 years at 55 °C.
  - up to 1 Kbyte RAM
  - 256 bytes data EEPROM with readout protection. 300,000 write/erase cycles guaranteed, data retention: 20 years at 55 °C.
- Clock, reset and supply management
  - Power on / power off safe reset with 3 programmable threshold levels (LVD)
  - Auxiliary voltage detector (AVD)
  - Clock sources: crystal/ceramic resonator oscillators, high-accuracy internal RC oscillator or external clock
  - PLL for 4x or 8x frequency multiplication
  - 5 power-saving modes: Slow, Wait, Halt, Auto-wakeup from Halt and Active-halt
  - Clock output capability (f_{CPU})
- Interrupt management
  - Nested interrupt controller
  - 10 interrupt vectors plus TRAP and RESET
  - 9 external interrupt lines on 4 vectors
- Up to 34 I/O ports
  - up to 34 multifunctional bidirectional I/O lines
  - up to 12 high sink outputs (10 on 32-pin devices)
- 4 timers
  - Configurable window watchdog timer
  - Real-time base
  - 16-bit timer A with: 1 input capture, 1 output compare, external clock input, PWM and pulse generator modes

LQFP48
7 x 7 mm



LQFP32
7 x 7 mm



LQFP44
10 x 10 mm

  - 16-bit timer B with: 2 input captures, 2 output compares, PWM and pulse generator modes
- 3 communication interfaces
  - I^2C multimaster / slave
  - I^2C slave 3 addresses, no stretch, with DMA access and byte pair coherency on I^2C read
  - SCI asynchronous serial interface (LIN compatible)
  - SPI synchronous serial interface
- 1 analog peripheral
  - 10-bit ADC with 12 input channels (8 on 32-pin devices)
- Instruction set
  - 8-bit data manipulation
  - 63 basic instructions with illegal opcode detection
  - 17 main addressing modes
  - 8 x 8 unsigned multiply instruction
- Development tools
  - Full hardware/software development package
  - On-chip debug module

Table 1. Device summary

References	Part numbers
ST72344xx	ST72344K2, ST72344K4, ST72344S2, ST72344S4
ST72345xx	ST72345C4

Contents

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1 Description

The ST7234x devices are members of the ST7 microcontroller family. *Table 2* gives the available part numbers and details on the devices. All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

They feature single-voltage Flash memory with byte-by-byte in-circuit programming (ICP) and in-application programming (IAP) capabilities.

Under software control, all devices can be placed in Wait, Slow, Auto-wakeup from Halt, Active-halt or Halt mode, reducing the power consumption when the application is in idle or stand-by state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

The devices feature an on-chip debug module (DM) to support in-circuit debugging (ICD). For a description of the DM registers, refer to the ST7 ICC Protocol Reference Manual.

Figure 1. General block diagram

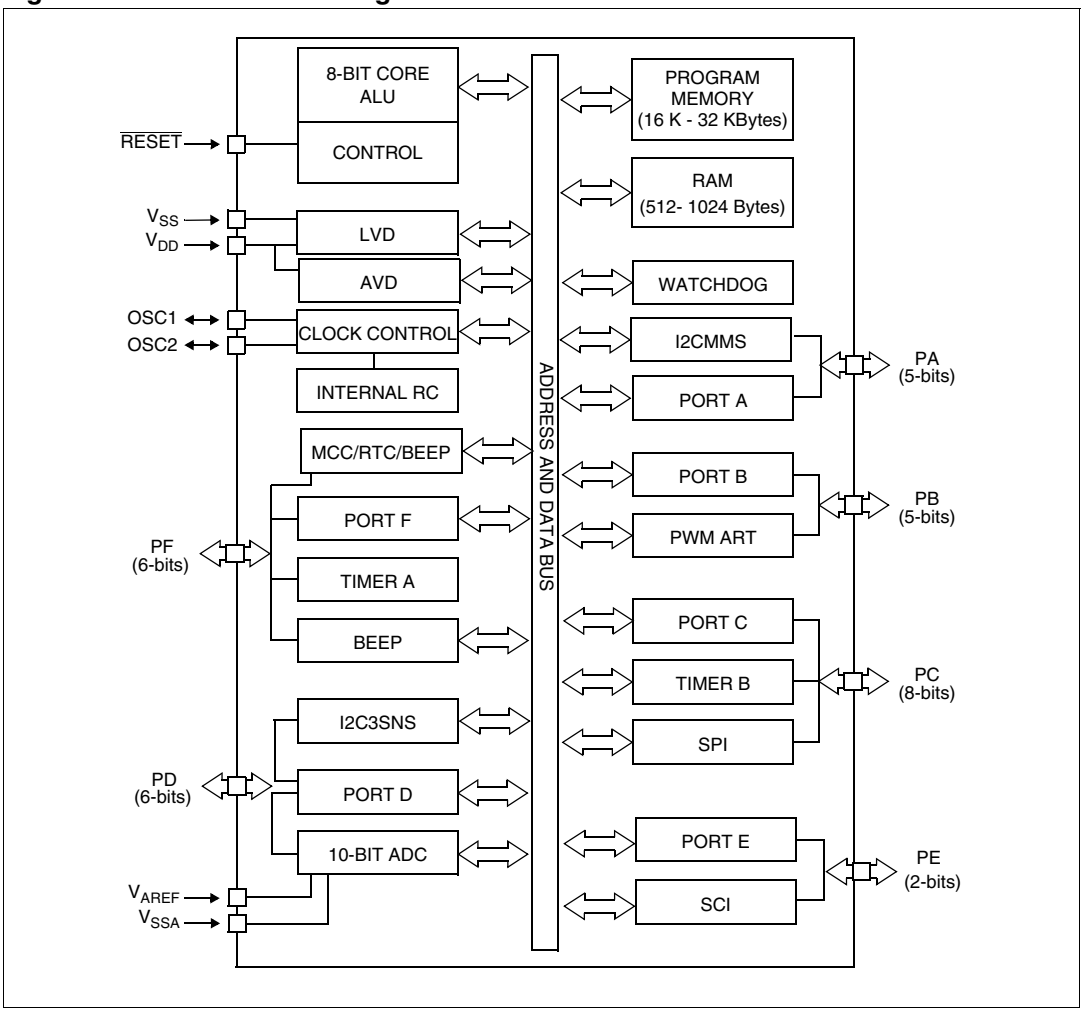


Table 2. ST72344xx and ST72345xx features

Features	ST72344K2, ST72344K4, ST72344S2, ST72344S4		ST72345C4
Program memory - bytes	8,000	16,000	16,000
RAM (stack) - bytes	512 bytes (256 bytes)	1 Kbyte (256 bytes)	1 Kbyte (256 bytes)
EEPROM data - bytes	256	256	256
Common peripherals	Window watchdog, 2 16-bit timers, SCI, SPI, I2CMMS		
Other peripherals	10-bit ADC		I2C3SNS, 10-bit ADC
CPU frequency	8 MHz @ 3.3 V to 5.5 V, 4 MHz @ 2.7 V to 5.5 V		
Temperature range	-40 °C to +85 °C		
Package	LQFP32 7x7, LQFP44 10x10		LQFP48 7x7

2 Pin description

Figure 2. LQFP32 package pinout

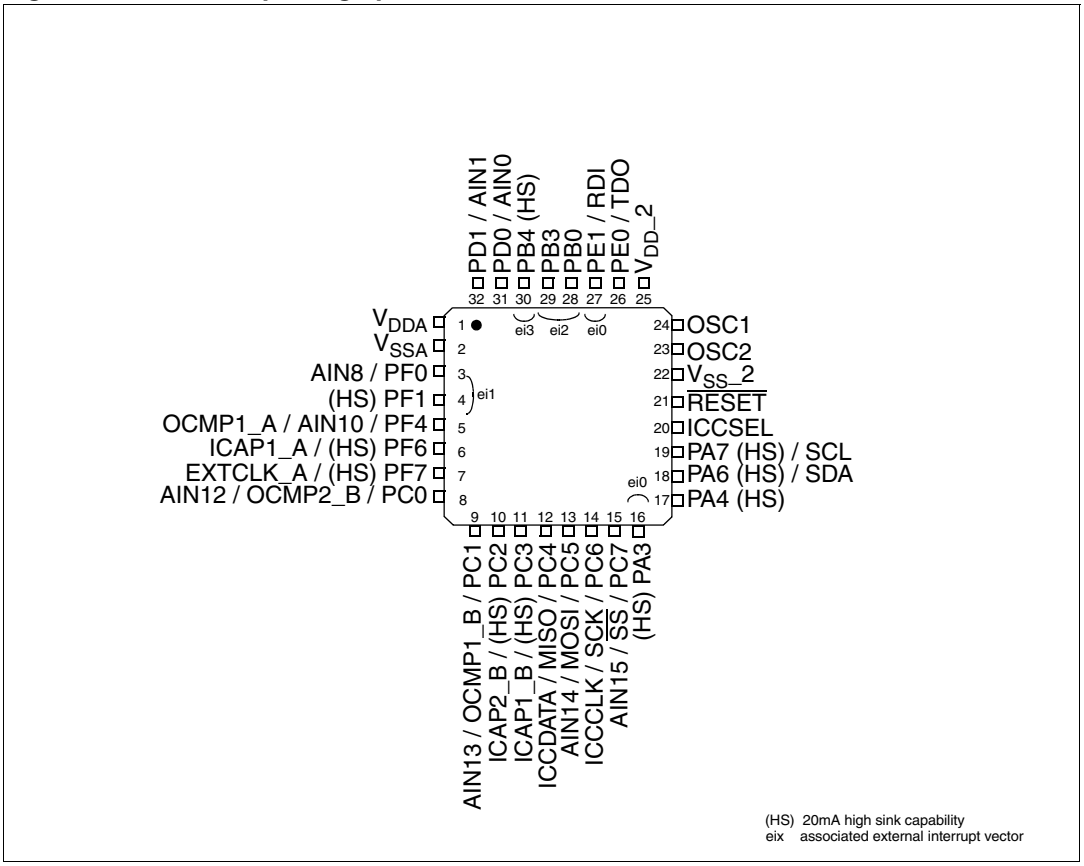


Figure 3. LQFP44 package pinout

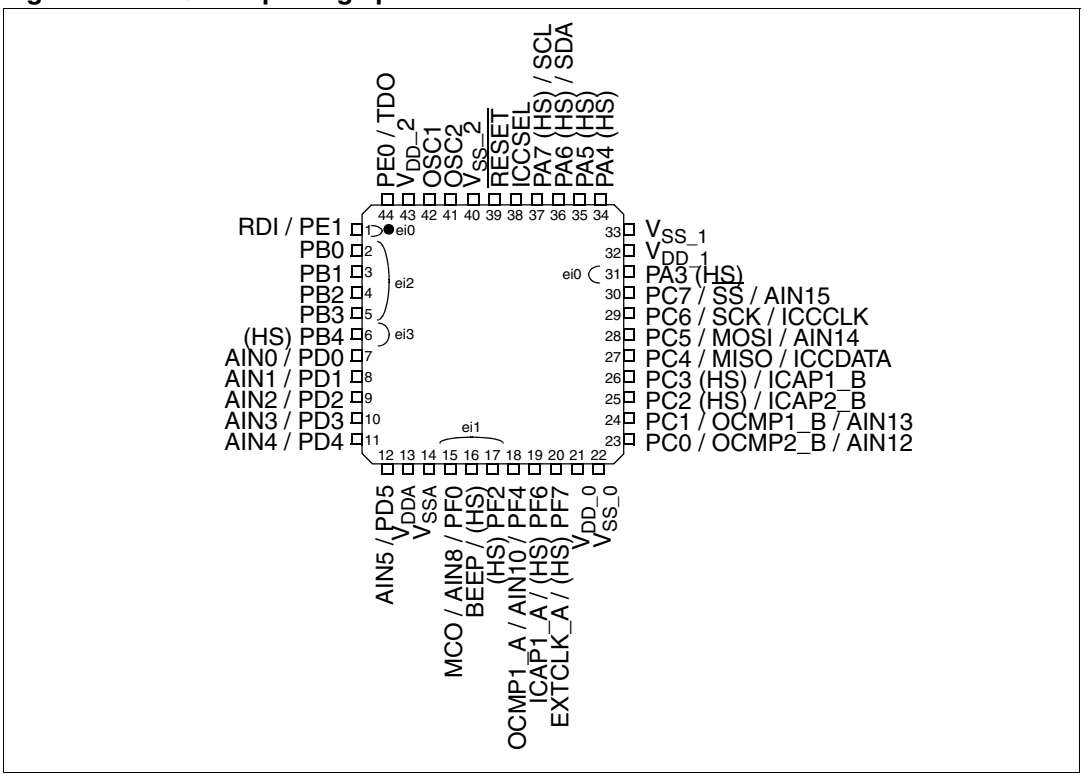
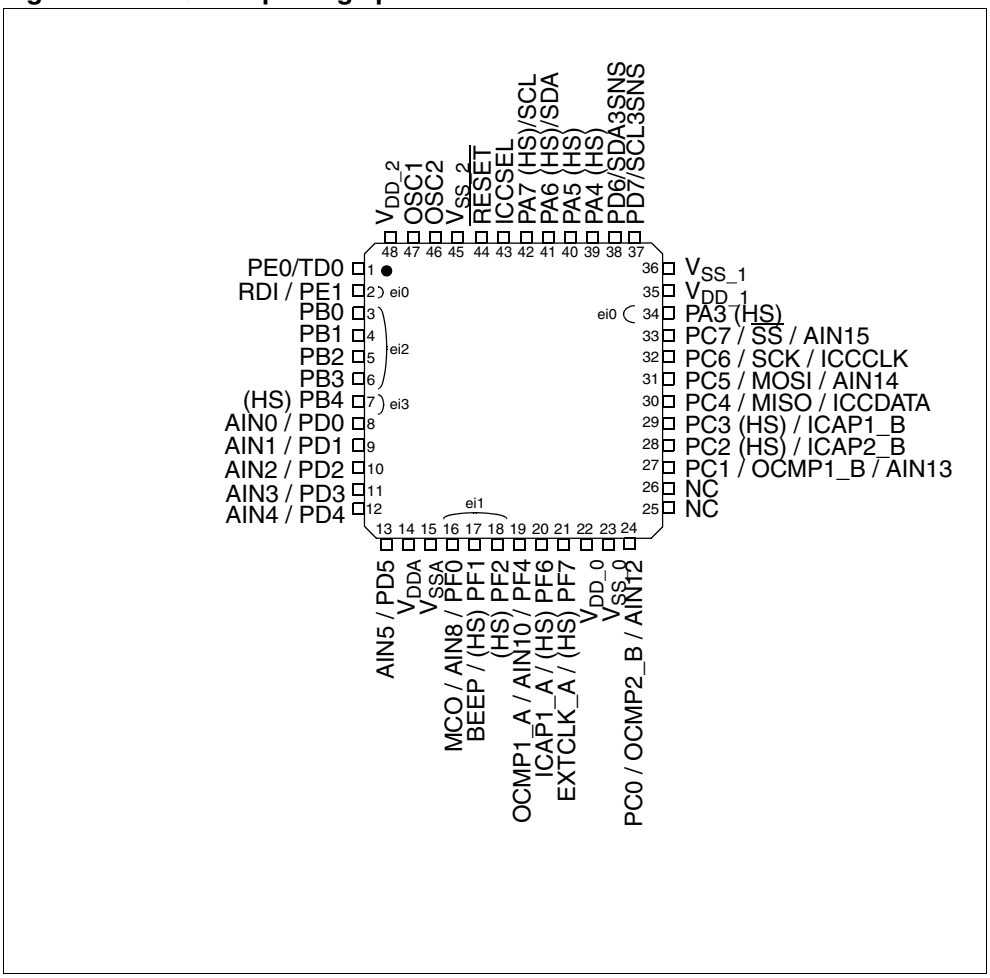


Figure 4. LQFP48 package pinout



Note: For external pin connection guidelines, refer to Section 13: Electrical characteristics.

Legend / Abbreviations for *Table 3*:

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20 mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog
- Output: OD = open drain [2], PP = push-pull

The reset configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

On the chip, each I/O port may have up to 8 pads. Pads that are not bonded to external pins are set in input pull-up configuration after reset through the option byte Package selection. The configuration of these pads must be kept at reset state to avoid added current consumption.

Table 3. Device pin description

Pin n°			Pin name	Type	Level		Port						Main function (after reset)	Alternate function	
							Input [1]				Output				
LQFP32	LQFP44	LQFP48			Input	Output	float	wpu	int	ana	OD	PP			
1	13	14	V_{DDA} [2]	S									Analog supply voltage		
2	14	15	V_{SSA} [2]	S									Analog ground voltage		
3	15	16	PF0/MCO/AIN8	I/O	C_T		X	ei1		X	X	X	Port F0	Main clock out (f_{OSC}/2)	ADC analog input 8
4	16	17	PF1 (HS)/BEEP	I/O	C_T	HS	X	ei1			X	X	Port F1	Beep signal output	
-	17	18	PF2 (HS) [3]	I/O	C_T	HS	X		ei1		X	X	Port F2		
5	18	19	PF4/OCMP1_A/AIN10	I/O	C_T		X	X		X	X	X	Port F4	Timer A output compare 1	ADC analog input 10
6	19	20	PF6 (HS)/ICAP1_A	I/O	C_T	HS	X	X			X	X	Port F6	Timer A Input Capture 1	
7	20	21	PF7 (HS)/EXTCLK_A	I/O	C_T	HS	X	X			X	X	Port F7	Timer A external clock source	
-	21	22	V_{DD_0} [2]	S									Digital main supply voltage		
-	22	23	V_{SS_0} [2]	S									Digital ground voltage		
8	23	24	PC0/OCMP2_B/AIN12	I/O	C_T		X	X		X	X	X	Port C0	Timer B output compare 2	ADC analog input 12
9	24	27	PC1/OCMP1_B/AIN13	I/O	C_T		X	X		X	X	X	Port C1	Timer B output compare 1	ADC analog input 13

Table 3. Device pin description (continued)

Pin n°			Pin name	Type	Level		Port						Main function (after reset)	Alternate function	
							Input (1)				Output				
LQFP32	LQFP44	LQFP48			Input	Output	float	wpu	int	ana	OD	PP			
10	25	28	PC2 (HS)/ICAP2_B	I/O	C_T	HS	X	X			X	X	Port C2	Timer B input capture 2	
11	26	29	PC3 (HS)/ICAP1_B	I/O	C_T	HS	X	X			X	X	Port C3	Timer B input capture 1	
12	27	30	PC4/MISO/ICCDATA	I/O	C_T		X	X			X	X	Port C4	SPI Master In / Slave Out data	ICC data input
13	28	31	PC5/MOSI/AIN14	I/O	C_T		X	X		X	X	X	Port C5	SPI Master Out / Slave In data	ADC analog input 14
14	29	32	PC6/SCK/ICCCLK	I/O	C_T		X	X			X	X	Port C6	SPI serial clock	ICC clock output
15	30	33	PC7/$\overline{SS}$/AIN15	I/O	C_T		X	X		X	X	X	Port C7	SPI slave select (active low)	ADC analog input 15
16	31	34	PA3 (HS)	I/O	C_T	HS	X		ei0		X	X	Port A3		
-	32	35	V_{DD_1} (2)	S									Digital main supply voltage		
-	33	36	V_{SS_1} (2)	S									Digital ground voltage		
-	-	37	PD7 (3)/ SCL3SNS	I/O	C_T	HS	X				T (4)		Port D7	I2C3SNS serial clock	
-	-	38	PD6 (3)/ SDA3SNS	I/O	C_T	HS	X				T		Port D6	I2C3SNS serial data	
17	34	39	PA4 (HS)	I/O	C_T	HS	X	X			X	X	Port A4		
-	35	40	PA5 (HS) (3)	I/O	C_T	HS	X	X			X	X	Port A5		
18	36	41	PA6 (HS)/SDA	I/O	C_T	HS	X				T		Port A6	I2C serial data	
19	37	42	PA7 (HS)/SCL	I/O	C_T	HS	X				T		Port A7	I2C serial clock	
20	38	43	ICCSEL (5)	I									ICC mode selection		
21	39	44	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt.		
22	40	45	V_{SS_2} (2)	S									Digital ground voltage		
23	41	46	OSC2	O									Resonator oscillator inverter output		
24	42	47	OSC1	I									External clock input or resonator oscillator inverter input		
25	43	48	V_{DD_2} (2)	S									Digital main supply voltage		
26	44	1	PE0/TDO	I/O	C_T		X	X			X	X	Port E0	SCI transmit data out	

Table 3. Device pin description (continued)

Pin n°			Pin name	Type	Level		Port						Main function (after reset)	Alternate function
							Input (1)				Output			
LQFP32	LQFP44	LQFP48			Input	Output	float	wpu	int	ana	OD	PP		
27	1	2	PE1/RDI	I/O	C_T		X		ei0		X	X	Port E1	SCI receive data in
28	2	3	PB0	I/O	C_T		X	ei2			X	X	Port B0	
-	3	4	PB1 (3)	I/O	C_T		X	ei2			X	X	Port B1	
-	4	5	PB2 (3)	I/O	C_T		X	ei2			X	X	Port B2	
29	5	6	PB3	I/O	C_T		X		ei2		X	X	Port B3	
30	6	7	PB4 (HS)	I/O	C_T	HS	X	ei3			X	X	Port B4	
31	7	8	PD0/AIN0	I/O	C_T		X	X		X	X	X	Port D0	ADC analog input 0
32	8	9	PD1/AIN1	I/O	C_T		X	X		X	X	X	Port D1	ADC analog input 1
-	9	10	PD2/AIN2	I/O	C_T		X	X		X	X	X	Port D2	ADC analog input 2
-	10	11	PD3/AIN3	I/O	C_T		X	X		X	X	X	Port D3	ADC analog input 3
-	11	12	PD4/AIN4	I/O	C_T		X	X		X	X	X	Port D4	ADC analog input 4
-	12	13	PD5/AIN5	I/O	C_T		X	X		X	X	X	Port D5	ADC analog input 5

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.
2. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.
3. Pulled-up by hardware when not present on the package.
4. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V_{DD} are not implemented).
5. Internal weak pull-down.

3 Register and memory map

As shown in *Figure 5*, the MCU is capable of addressing 64 Kbytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, up to 1 Kbyte of RAM, 256 bytes of Data EEPROM and up to 16 Kbytes of user program memory. The RAM space includes up to 256 bytes for the stack from 0100h to 01FFh.

The highest address bytes contain the user reset and interrupt vectors.

Figure 5. Memory map

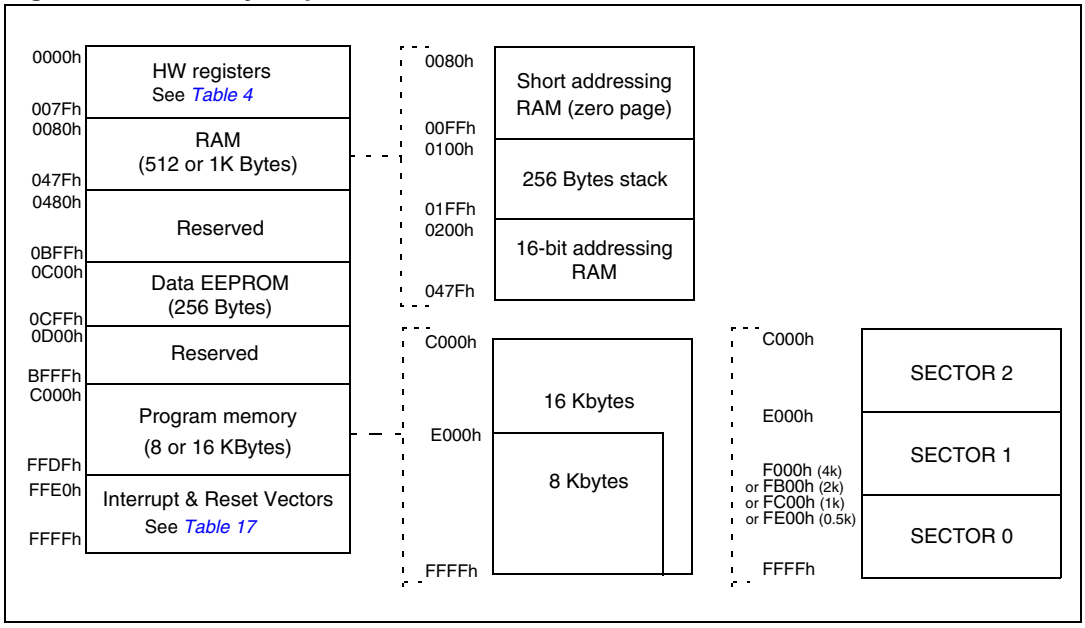


Table 4. Hardware register map

Address	Block	Register label	Register name	Reset status (1)	Remarks (2)
0000h 0001h 0002h	Port A (3)	PADR PADDR PAOR	Port A Data Register Port A Data Direction Register Port A Option Register	00h (4) 00h 00h	R/W R/W R/W
0003h 0004h 0005h	Port B (3)	PBDR PBDDR PBOR	Port B Data Register Port B Data Direction Register Port B Option Register	00h (4) 00h 00h	R/W R/W R/W
0006h 0007h 0008h	Port C (3)	PCDR PCDDR PCOR	Port C Data Register Port C Data Direction Register Port C Option Register	00h (4) 00h 00h	R/W R/W R/W
0009h 000Ah 000Bh	Port D (3)	PDADR PDDDR PDOR	Port D Data Register Port D Data Direction Register Port D Option Register	00h (4) 00h 00h	R/W R/W R/W
000Ch 000Dh 000Eh	Port E (3)	PEDR PEDDR PEOR	Port E Data Register Port E Data Direction Register Port E Option Register	00h (4) 00h 00h	R/W R/W R/W
000Fh 0010h 0011h	Port F (3)	PFDR PFDDR PFOR	Port F Data Register Port F Data Direction Register Port F Option Register	00h (4) 00h 00h	R/W R/W R/W
0012h to 0016h	Reserved area (5 bytes)				
0017h 0018h	RC	RCCRH RCCRL	RC oscillator Control Register High RC oscillator Control Register Low	FFh 03h	R/W R/W
0019h	Reserved area (1 byte)				
001Ah to 001Fh	DM (5)	Reserved area (6 bytes)			
00020h	EEPROM	EECSR	Data EEPROM Control/Status Register	00h	R/W
0021h 0022h 0023h	SPI	SPIDR SPICR SPICSR	SPI Data I/O Register SPI Control Register SPI Control Status Register	xxh 0xh 00h	R/W R/W R/W
0024h 0025h 0026h 0027h	ITC	ISPR0 ISPR1 ISPR2 ISPR3	Interrupt Software Priority Register 0 Interrupt Software Priority Register 1 Interrupt Software Priority Register 2 Interrupt Software Priority Register 3	FFh FFh FFh FFh	R/W R/W R/W R/W
0028h		EICR	External Interrupt Control Register	00h	R/W
00029h	Flash	FCSR	Flash Control/Status Register	00h	R/W
002Ah	WWDG	WDGCR	Watchdog Control Register	7Fh	R/W
002Bh	SI	SICSR	System Integrity Control/Status Register	000x 000xb	R/W
002Ch 002Dh	MCC	MCCSR MCCBCR	Main Clock Control/Status Register MCC Beep Control Register	00h 00h	R/W R/W
002Eh 002Fh	AWU	AWUCSR AWUPR	AWU Control/Status Register AWU Prescaler Register	00h FFh	R/W R/W
0030h	WWDG	WDGWR	Window Watchdog Control Register	7Fh	R/W

Table 4. Hardware register map (continued)

Address	Block	Register label	Register name	Reset status (1)	Remarks (2)
0031h	TIMER A	TACR2	Timer A Control Register 2	00h	R/W
0032h		TACR1	Timer A Control Register 1	00h	R/W
0033h		TACSR	Timer A Control/Status Register	xxh	R/W
0034h		TAIC1HR	Timer A Input Capture 1 High Register	xxh	Read Only
0035h		TAIC1LR	Timer A Input Capture 1 Low Register	xxh	Read Only
0036h		TAOC1HR	Timer A Output Compare 1 High Register	80h	R/W
0037h		TAOC1LR	Timer A Output Compare 1 Low Register	00h	R/W
0038h		TACHR	Timer A Counter High Register	FFh	Read Only
0039h		TACLR	Timer A Counter Low Register	FCh	Read Only
003Ah		TAACHR	Timer A Alternate Counter High Register	FFh	Read Only
003Bh		TAACLR	Timer A Alternate Counter Low Register	FCh	Read Only
003Ch		TAIC2HR	Timer A Input Capture 2 High Register	xxh	Read Only
003Dh		TAIC2LR	Timer A Input Capture 2 Low Register	xxh	Read Only
003Eh		TAOC2HR	Timer A Output Compare 2 High Register	80h	R/W
003Fh		TAOC2LR	Timer A Output Compare 2 Low Register	00h	R/W
0040h	Reserved area (1 Byte)				
0041h	TIMER B	TBCR2	Timer B Control Register 2	00h	R/W
0042h		TBCR1	Timer B Control Register 1	00h	R/W
0043h		TBCSR	Timer B Control/Status Register	xxh	R/W
0044h		TBIC1HR	Timer B Input Capture 1 High Register	xxh	Read Only
0045h		TBIC1LR	Timer B Input Capture 1 Low Register	xxh	Read Only
0046h		TBOC1HR	Timer B Output Compare 1 High Register	80h	R/W
0047h		TBOC1LR	Timer B Output Compare 1 Low Register	00h	R/W
0048h		TBCHR	Timer B Counter High Register	FFh	Read Only
0049h		TBCLR	Timer B Counter Low Register	FCh	Read Only
004Ah		TBACHR	Timer B Alternate Counter High Register	FFh	Read Only
004Bh		TBACLR	Timer B Alternate Counter Low Register	FCh	Read Only
004Ch		TBIC2HR	Timer B Input Capture 2 High Register	xxh	Read Only
004Dh		TBIC2LR	Timer B Input Capture 2 Low Register	xxh	Read Only
004Eh		TBOC2HR	Timer B Output Compare 2 High Register	80h	R/W
004Fh		TBOC2LR	Timer B Output Compare 2 Low Register	00h	R/W
0050h	SCI	SCISR	SCI Status Register	C0h	Read Only
0051h		SCIDR	SCI Data Register	xxh	R/W
0052h		SCIBRR	SCI Baud Rate Register	00h	R/W
0053h		SCICR1	SCI Control Register 1	x000 0000b	R/W
0054h		SCICR2	SCI Control Register 2	00h	R/W
0055h			Reserved area	--	
0056h		SCIERPR	SCI Extended Receive Prescaler Register	00h	R/W
0057h		SCIETPR	SCI Extended Transmit Prescaler Register	00h	R/W
0058h	I^2C	I2CCR	I^2C Control Register	00h	R/W
0059h		I2CSR1	I^2C Status Register 1	00h	Read Only
005Ah		I2CSR2	I^2C Status Register 2	00h	Read Only
005Bh		I2CCCR	I^2C Clock Control Register	00h	R/W
005Ch		I2COAR1	I^2C Own Address Register 1	00h	R/W
005Dh		I2COAR2	I^2C Own Address Register2	40h	R/W
005Eh		I2CDR	I^2C Data Register	00h	R/W
005Fh	Reserved area (1 byte)				