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ST72521xx-Auto

8-bit MCU for automotive with 32/60 Kbyte Flash/ROM, ADC, 5 timers, SPI, SCI, I2C, CAN interface

Features

Memories

- 32 to 60 Kbyte dual voltage High Density Flash (HDFlash) or ROM with readout protection capability. In-application programming and in-circuit programming for HDFlash devices
- 1 to 2 Kbyte RAM
- HDFlash endurance: 100 cycles, data retention 20 years

Clock, reset and supply management

- Enhanced low voltage supervisor (LVD) for main supply and auxiliary voltage detector (AVD) with interrupt capability
- Clock sources: crystal/ceramic resonator oscillators, internal RC oscillator and bypass for external clock
- PLL for 2x frequency multiplication
- 4 power saving modes: Halt, Active Halt, Wait and Slow

Interrupt management

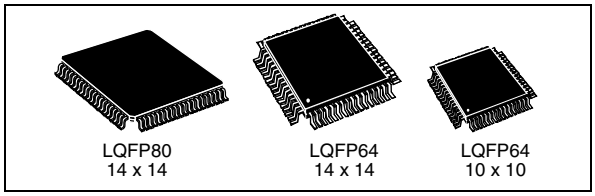
- Nested interrupt controller
- 14 interrupt vectors plus TRAP and RESET
- Top Level Interrupt (TLI) pin
- 15 external interrupt lines (on 4 vectors)

Analog peripheral

- 10-bit ADC with up to 16 input ports

Up to 64 I/O ports

- 48 multifunctional bidirectional I/O lines
- 34 alternate function lines
- 16 high sink outputs



5 timers

- Main clock controller with Real-time base, Beep and Clock-out capabilities
- Configurable watchdog timer
- Two 16-bit timers with 2 input captures, 2 output compares, external clock input on 1 timer, PWM and pulse generator modes
- 8-bit PWM auto-reload timer with 2 input captures, 4 PWM outputs, output compare and time base interrupt, external clock with event detector

4 communications interfaces

- SPI synchronous serial interface
- SCI asynchronous serial interface
- I^2C multimaster interface (SMbus V1.1 compliant)
- CAN interface (2.0B passive)

Instruction set

- 8-bit data manipulation
- 63 basic instructions
- 17 main addressing modes
- 8x8 unsigned multiply instruction

Development tools

- Full HW/SW development pkg, ICT capability

Table 1. Device summary

Reference	Part number
ST72521xx-Auto	ST72521R6-Auto ST72521R9-Auto ST72521AR9-Auto ST72521M9-Auto

Contents

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1 Description

The ST72521xx-Auto Flash and ROM devices are members of the ST7 microcontroller family designed for mid-range automotive applications running from 3.8 to 5.5V.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with Flash or ROM program memory. The ST7 family architecture offers both power and flexibility to software developers, enabling the design of highly efficient and compact application code.

The on-chip peripherals include an A/D converter, a PWM autoreload timer, two general purpose timers, I^2C, SPI, SCI and CAN (controller area network) bus interfaces.

For power economy, the microcontroller can switch dynamically into Wait, Slow, Active Halt or Halt mode when the application is in idle or standby state.

Table 2. Device summary

Reference	Program memory	RAM (stack)	Voltage range	Temp. range	Package
ST72521M9-Auto	60 Kbytes Flash	2048 (256) bytes	3.8V to 5.5V	Up to -40°C to 125°C	LQFP80 14x14
ST72521R9-Auto					LQFP64 14x14
ST72521AR9-Auto					LQFP64 10x10
ST72521R6-Auto	32 Kbytes Flash	1024 (256) byte			LQFP64 14x14
ST72521AR6-Auto					LQFP64 10x10
ST72521BM9-Auto	60 Kbytes ROM	2048 (256) bytes			LQFP80 14x14
ST72521BR9-Auto					LQFP64 14x14
ST72521BAR9-Auto					LQFP64 10x10
ST72521BR6-Auto	32 Kbytes ROM	1024 (256) byte			LQFP64 14x14
ST72521BAR6-Auto					LQFP64 10x10

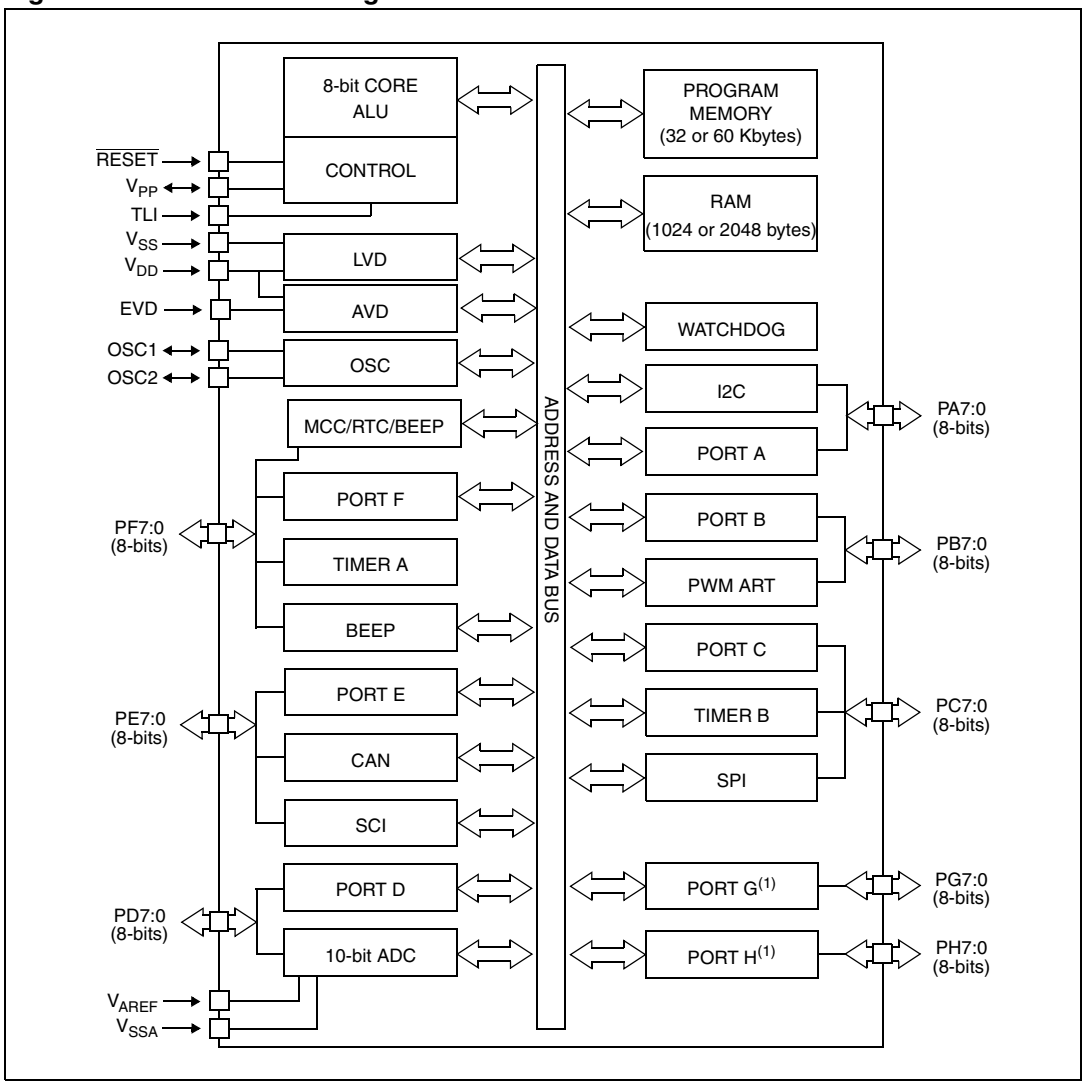
Typical applications include

- all types of car body applications such as window lift, DC motor control, rain sensors
- car body controllers, low end junction boxes
- auxiliary functions in car radios

Related documentation

Migrating applications from ST72511/311/314 to ST72521/321/324 (AN1131)

Figure 1. Device block diagram



1. On certain devices only (see *Section Table 3.: Device pin description on page 23*)

2 Package pinout and pin description

2.1 Package pinout

Figure 2. 80-pin LQFP 14x14 package pinout

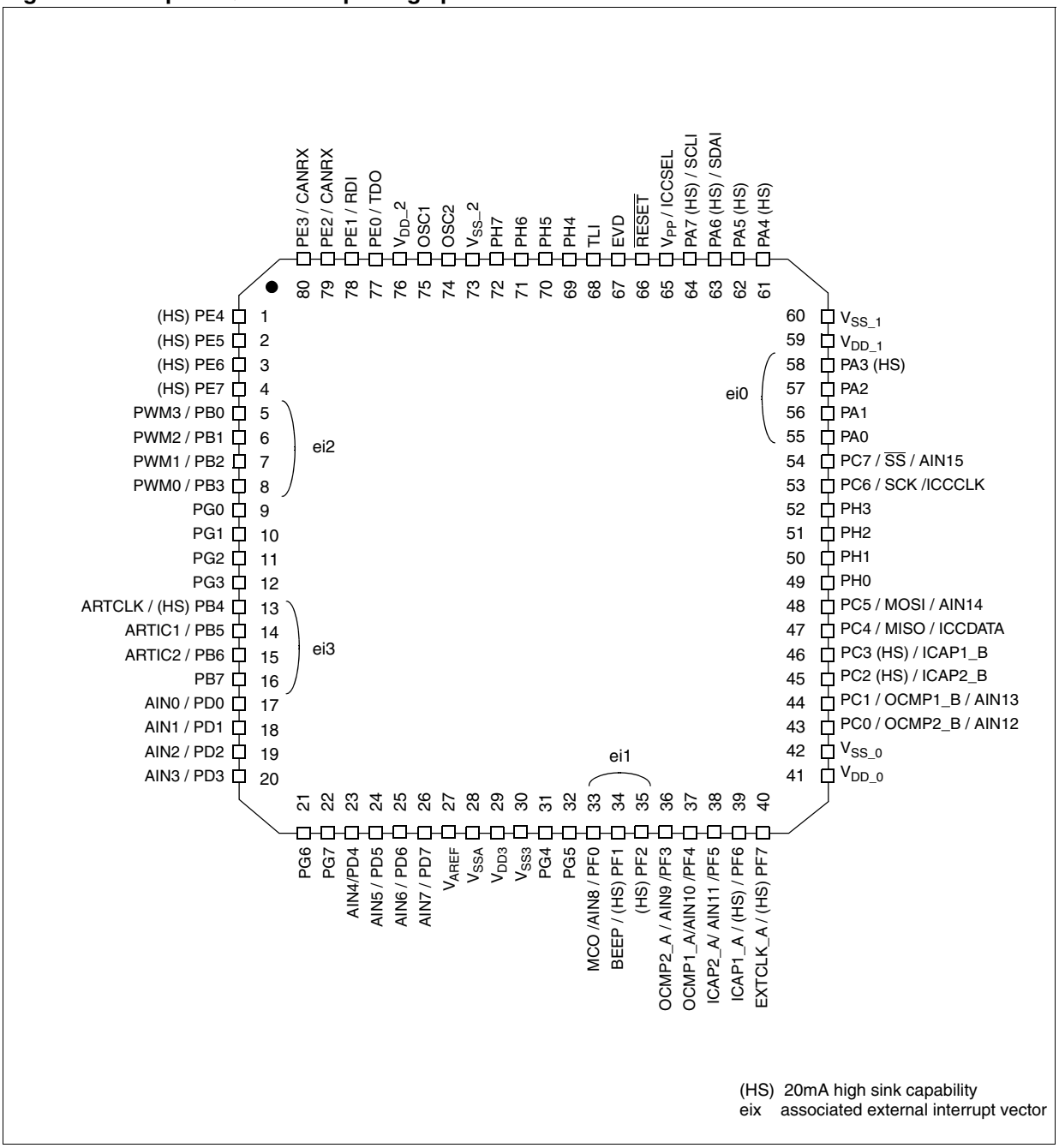
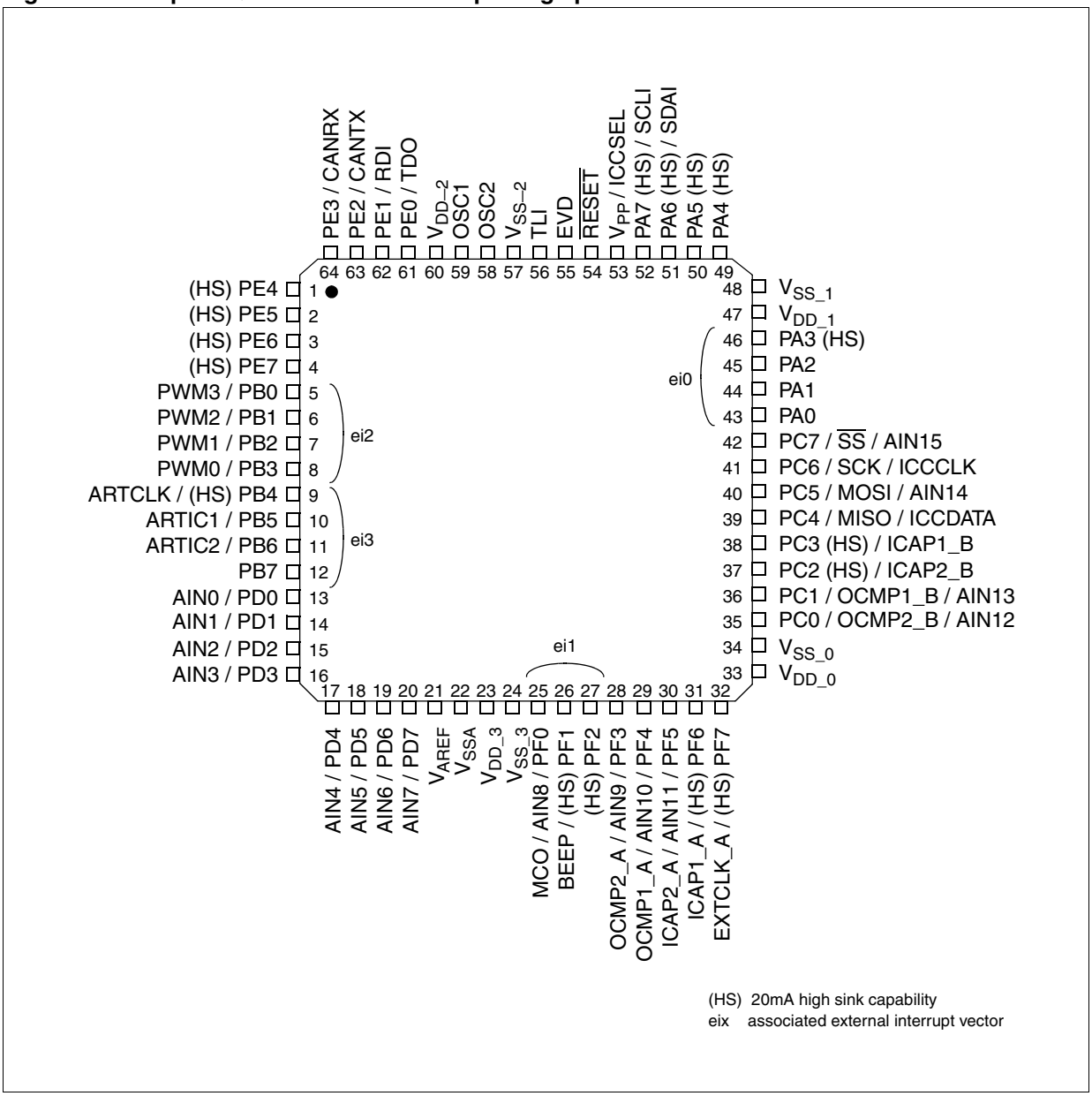


Figure 3. 64-pin LQFP 14x14 and 10x10 package pinout



For external pin connection guidelines, refer to *Section 20: Electrical characteristics*.

2.2 Pin description

In the device pin description table, the RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Refer to *Section 9: I/O ports on page 73* for more details on the software configuration of the I/O ports.

Table 3. Device pin description

Pin			Type	Level		Port						Main function (after reset)	Alternate function
No.		Name				Input				Output			
LQFP80	LQFP64			Input	Output	float	wpu	int	ana	OD	PP		
1	1	PE4 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E4	
2	2	PE5 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E5	
3	3	PE6 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E6	
4	4	PE7 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E7	
5	5	PB0/PWM3	I/O	C_T		**X**	ei2			X	X	Port B0	PWM Output 3
6	6	PB1/PWM2	I/O	C_T		**X**	ei2			X	X	Port B1	PWM Output 2
7	7	PB2/PWM1	I/O	C_T		**X**	ei2			X	X	Port B2	PWM Output 1
8	8	PB3/PWM0	I/O	C_T		**X**		ei2		X	X	Port B3	PWM Output 0
9	-(1)	PG0	I/O	T_T		**X**	X			X	X	Port G0	
10	-(1)	PG1	I/O	T_T		**X**	X			X	X	Port G1	
11	-(1)	PG2	I/O	T_T		**X**	X			X	X	Port G2	
12	-(1)	PG3	I/O	T_T		**X**	X			X	X	Port G3	
13	9	PB4 (HS)/ARTCLK	I/O	C_T	HS	**X**	ei3			X	X	Port B4	PWM-ART External Clock
14	10	PB5/ARTIC1	I/O	C_T		**X**	ei3			X	X	Port B5	PWM-ART Input Capture 1
15	11	PB6/ARTIC2	I/O	C_T		**X**	ei3			X	X	Port B6	PWM-ART Input Capture 2
16	12	PB7	I/O	C_T		**X**		ei3		X	X	Port B7	
17	13	PD0 /AIN0	I/O	C_T		**X**	X		X	X	X	Port D0	ADC Analog Input 0
18	14	PD1/AIN1	I/O	C_T		**X**	X		X	X	X	Port D1	ADC Analog Input 1
19	15	PD2/AIN2	I/O	C_T		**X**	X		X	X	X	Port D2	ADC Analog Input 2
20	16	PD3/AIN3	I/O	C_T		**X**	X		X	X	X	Port D3	ADC Analog Input 3
21	-(1)	PG6	I/O	T_T		**X**	X			X	X	Port G6	
22	-(1)	PG7	I/O	T_T		**X**	X			X	X	Port G7	

Table 3. Device pin description (continued)

Pin			Type	Level		Port						Main function (after reset)	Alternate function	
No.		Name				Input				Output				
LQFP80	LQFP64			Input	Output	float	wpu	int	ana	OD	PP			
23	17	PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4	
24	18	PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5	
25	19	PD6/AIN6	I/O	C_T		**X**	X		X	X	X	Port D6	ADC Analog Input 6	
26	20	PD7/AIN7	I/O	C_T		**X**	X		X	X	X	Port D7	ADC Analog Input 7	
27	21	V_{AREF}(2)	I									Analog Reference Voltage for ADC		
28	22	V_{SSA}(2)	S									Analog Ground Voltage		
29	23	V_{DD_3}(2)	S									Digital Main Supply Voltage		
30	24	V_{SS_3}(2)	S									Digital Ground Voltage		
31	-(1)	PG4	I/O	T_T		**X**	X			X	X	Port G4		
32	-(1)	PG5	I/O	T_T		**X**	X			X	X	Port G5		
33	25	PF0/MCO/AIN8	I/O	C_T		**X**	ei1		X	X	X	Port F0	Main clock out (f_{CPU})	ADC Analog Input 8
34	26	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
35	27	PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
36	28	PF3/OCMP2_A/AIN9	I/O	C_T		**X**	X		X	X	X	Port F3	Timer A Output Compare 2	ADC Analog Input 9
37	29	PF4/OCMP1_A/AIN10	I/O	C_T		**X**	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
38	30	PF5/ICAP2_A/AIN11	I/O	C_T		**X**	X		X	X	X	Port F5	Timer A Input Capture 2	ADC Analog Input 11
39	31	PF6 (HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
40	32	PF7 (HS)/EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
41	33	V_{DD_0}(2)	S									Digital Main Supply Voltage		
42	34	V_{SS_0}(2)	S									Digital Ground Voltage		
43	35	PC0/OCMP2_B/AIN12	I/O	C_T		**X**	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
44	36	PC1/OCMP1_B/AIN13	I/O	C_T		**X**	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13

Table 3. Device pin description (continued)

Pin			Type	Level		Port						Main function (after reset)	Alternate function	
No.		Name				Input				Output				
LQFP80	LQFP64			Input	Output	float	wpu	int	ana	OD	PP			
45	37	PC2 (HS)/ICAP2_B	I/O	C_T	HS	**X**	X			X	X	Port C2	Timer B Input Capture 2	
46	38	PC3 (HS)/ICAP1_B	I/O	C_T	HS	**X**	X			X	X	Port C3	Timer B Input Capture 1	
47	39	PC4/MISO/ICCDATA	I/O	C_T		**X**	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
48	40	PC5/MOSI/AIN14	I/O	C_T		**X**	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
49	- (1)	PH0	I/O	T_T		**X**	X			X	X	Port H0		
50	- (1)	PH1	I/O	T_T		**X**	X			X	X	Port H1		
51	- (1)	PH2	I/O	T_T		**X**	X			X	X	Port H2		
52	- (1)	PH3	I/O	T_T		**X**	X			X	X	Port H3		
53	41	PC6/SCK/ICCCLK	I/O	C_T		**X**	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output
													Caution: Negative current injection not allowed on this pin (Flash devices only)	
54	42	PC7/$\overline{SS}$/AIN15	I/O	C_T		**X**	X		X	X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
55	43	PA0	I/O	C_T		**X**	ei0			X	X	Port A0		
56	44	PA1	I/O	C_T		**X**	ei0			X	X	Port A1		
57	45	PA2	I/O	C_T		**X**	ei0			X	X	Port A2		
58	46	PA3 (HS)	I/O	C_T	HS	**X**		ei0		X	X	Port A3		
59	47	V_{DD_1} (2)	S									Digital Main Supply Voltage		
60	48	V_{SS_1} (2)	S									Digital Ground Voltage		
61	49	PA4 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A4		
62	50	PA5 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A5		
63	51	PA6 (HS)/SDAI	I/O	C_T	HS	**X**				T		Port A6	I^2C Data	
64	52	PA7 (HS)/SCLI	I/O	C_T	HS	**X**				T		Port A7	I^2C Clock	