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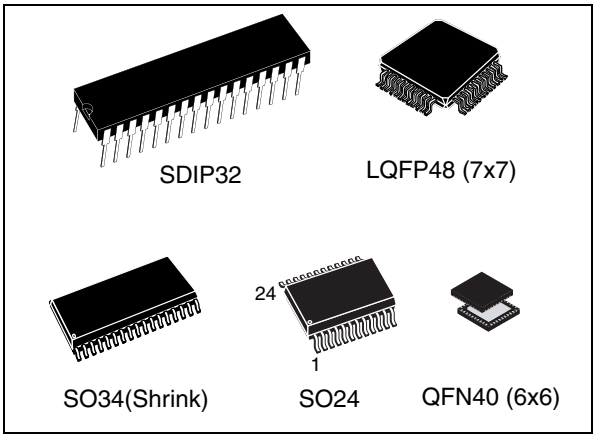
ST7263BHx ST7263BDx ST7263BKx ST7263BEx

Low speed USB 8-bit MCU family with up to 32 KB Flash/ROM, DFU capability, 8-bit ADC, WDG, timer, SCI and I²C

Features

- Memories
  - 4, 8, 16 or 32 Kbytes Program memory: high density Flash (HDFlash), or ROM with Readout and Write Protection
  - In-application Programming (IAP) and in-circuit programming (ICP)
  - 384, 512 or 1024 bytes RAM memory (128-byte stack)
- Clock, reset and supply management
  - Run, Wait, Slow and Halt CPU modes
  - 12 or 24 MHz oscillator
  - RAM retention mode
  - Optional low voltage detector (LVD)
- Universal serial bus (USB) interface
  - DMA for low speed applications compliant with USB 1.5 Mbs (version 2.0) and HID specifications (version 1.0)
  - Integrated 3.3 V voltage regulator and transceivers
  - Supports USB DFU class specification
  - Suspend and Resume operations
  - 3 endpoints with programmable In/Out configuration
- Up to 27 I/O ports
  - Up to 8 high sink I/Os (10 mA at 1.3 V)
  - 2 very high sink true open drain I/Os (25 mA at 1.5 V)
  - Up to 8 lines individually programmable as interrupt inputs
- 1 analog peripheral
  - 8-bit A/D converter with 8 or 12 channels
- 2 timers
  - Programmable watchdog
  - 16-bit timer with 2 input Captures, 2 output Compares, PWM output and clock input



- 2 communication Interfaces
  - Asynchronous serial communications interface
  - I²C multimaster interface up to 400 kHz
- Instruction set
  - 63 basic instructions
  - 17 main addressing modes
  - 8 x 8 unsigned multiply instruction
  - True bit manipulation
- Development tools
  - Versatile development tools (under Windows) including assembler, linker, C-compiler, archiver, source level debugger, software library, hardware emulator, programming boards and gang programmers, HID and DFU software layers

Table 1. Device summary

Reference	Part number
ST7263BHx	ST7263BH2, ST7263BH6
ST7263BDx	ST7263BD6
ST7263BKx	ST7263BK1, ST7263BK2, ST7263BK4, ST7263BK6
ST7263BEx	ST7263BE1, ST7263BE2, ST7263BE4, ST7263BE6

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1 Introduction

The ST7263B microcontrollers form a sub-family of the ST7 MCUs dedicated to USB applications. The devices are based on an industry-standard 8-bit core and feature an enhanced instruction set. They operate at a 24 MHz or 12 MHz oscillator frequency. Under software control, the ST7263B MCUs may be placed in either Wait or Halt modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST7263B MCUs feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The devices include an ST7 core, up to 32 Kbytes of program memory, up to 1024 bytes of RAM, 27 I/O lines and the following on-chip peripherals:

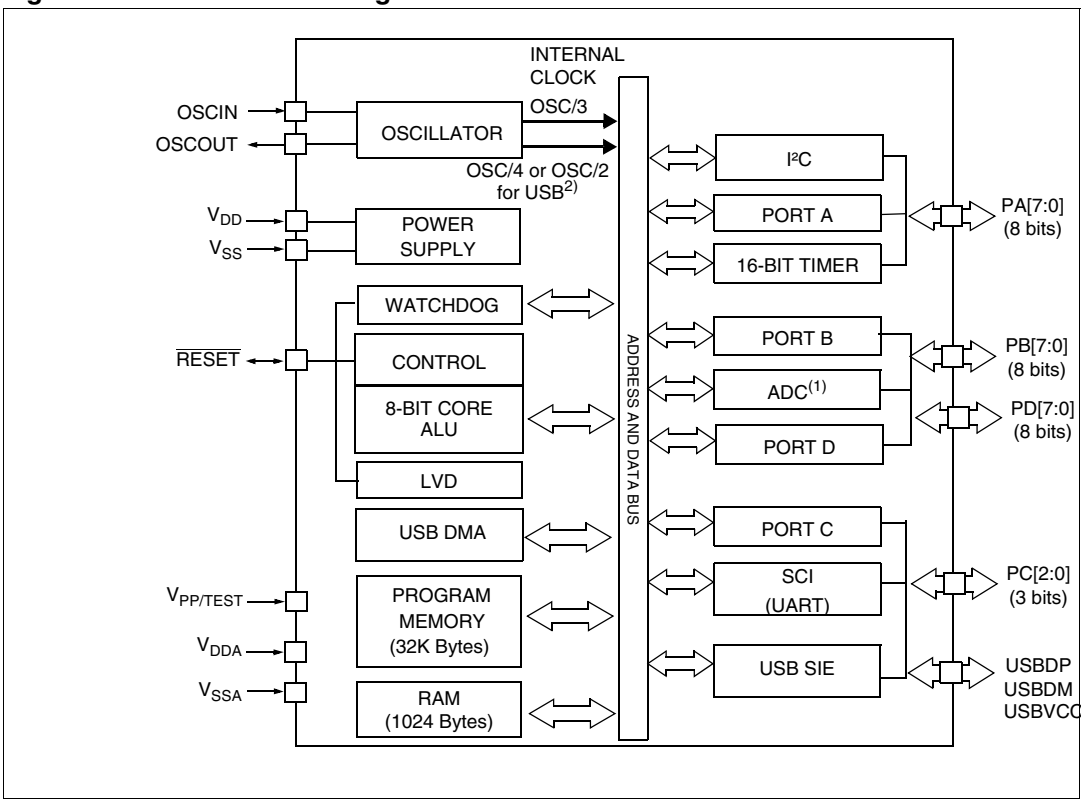
- USB low speed interface with 3 endpoints with programmable in/out configuration using the DMA architecture with embedded 3.3 V voltage regulator and transceivers (no external components are needed).
- 8-bit analog-to-digital converter (ADC) with 12 multiplexed analog inputs
- Industry standard asynchronous SCI serial interface
- Watchdog
- 16-bit Timer featuring an External clock input, 2 input Captures, 2 output Compares with Pulse Generator capabilities
- Fast I²C multimaster interface
- Low voltage reset (LVD) ensuring proper power-on or power-off of the device

The ST72F63B devices are Flash versions. They support programming in IAP mode (In-application programming) via the on-chip USB interface.

Table 2. Device overview

Features	ST7263BHx			ST7263BDx	ST7263BKx				ST7263BEx			
Program memory - Kbytes (Flash / ROM)	32	16	8	32	32	16	8	4	32	16	8	4
RAM (stack) - bytes	1024 (128)	512 (128)	384 (128)	1024 (128)	1024 (128	512 (128)	384 (128)	384 (128	1024 (128)	512 (128)	384 (128)	384 (128)
Standard Peripherals	Watchdog timer, 16-bit timer, USB											
Other Peripherals	SCI, I²C, ADC						SCI, AD	ADC	SCI, I²C			
I/Os (high current)	27 (10)				19 (10)				14 (6)			
Operating Supply	4.0 V to 5.5 V											
CPU frequency	8 MHz (with 24 MHz oscillator) or 4 MHz (with 12 MHz oscillator)											
Operating temp.	0 °C to +70 °C											
Packages	LQFP48 (7x7)			QFN40 (6x6)	SDIP32/ SO34		QFN40 (6x6)	SDIP32/ SO34	SO24			

Figure 1. General block diagram



1. ADC channels:
   12 on 48-pin devices (Port B and Port D[3:0])
   8 on 34 and 32-pin devices (Port B)
   None on 24-pin devices
2. 12 or 24 MHz OSCIN frequency required to generate 6 MHz USB clock.
3. The drive from USBVCC is sufficient to only drive an external pull-up in addition to the internal transceiver.

2 Pin description

2.1 $\overline{\text{RESET}}$ signal (bidirectional)

It is active low and forces the initialization of the MCU. This event is the top priority non maskable interrupt. This pin is switched low when the Watchdog is triggered or the V_{DD} is low. It can be used to reset external peripherals.

Note: Adding two 100 nF decoupling capacitors on the Reset pin (respectively connected to V_{DD} and V_{SS}) will significantly improve product electromagnetic susceptibility performance.

2.2 OSCIN/OSCOUT: input/output oscillator pin

These pins connect a parallel-resonant crystal, or an external source, to the on-chip oscillator.

2.3 V_{DD}/V_{SS}

Main power supply and ground voltages

Note: To enhance the reliability of operation, it is recommended that V_{DDA} and V_{DD} be connected together on the application board. This also applies to V_{SSA} and V_{SS}.

2.4 V_{DDA}/V_{SSA}

Power supply and ground voltages for analog peripherals.

Note: To enhance the reliability of operation, it is recommended that V_{DDA} and V_{DD} be connected together on the application board. This also applies to V_{SSA} and V_{SS}.

2.5 Alternate functions

Several pins of the I/O ports assume software programmable alternate functions as shown in the pin description.

Note: 1 The USBOE alternate function is mapped on Port C2 in 32/34/48 pin devices. In SO24 devices it is mapped on Port B1.

2 The timer OCMP1 alternate function is mapped on Port A6 in 32/34/48 pin devices. In SO24 devices it is not available.

Figure 2. 48-pin LQFP pinout

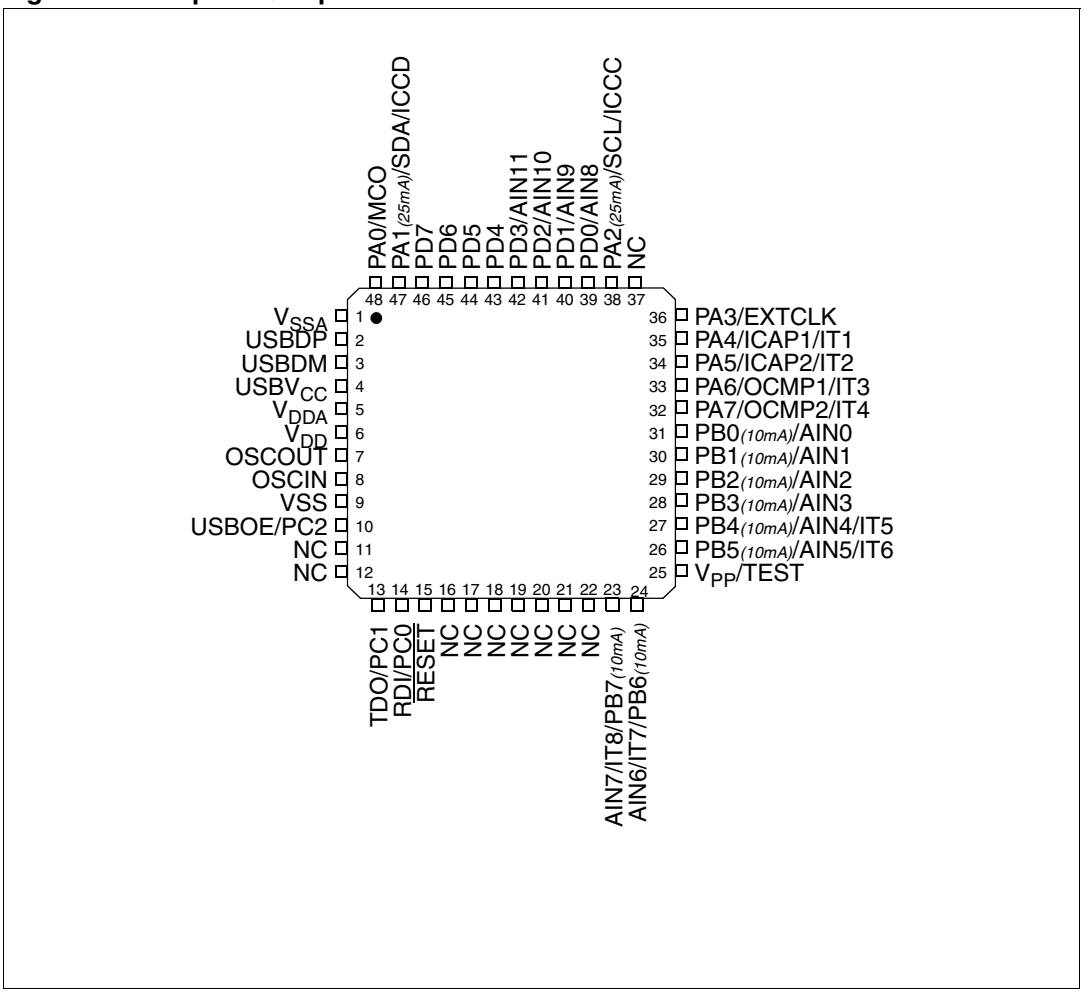
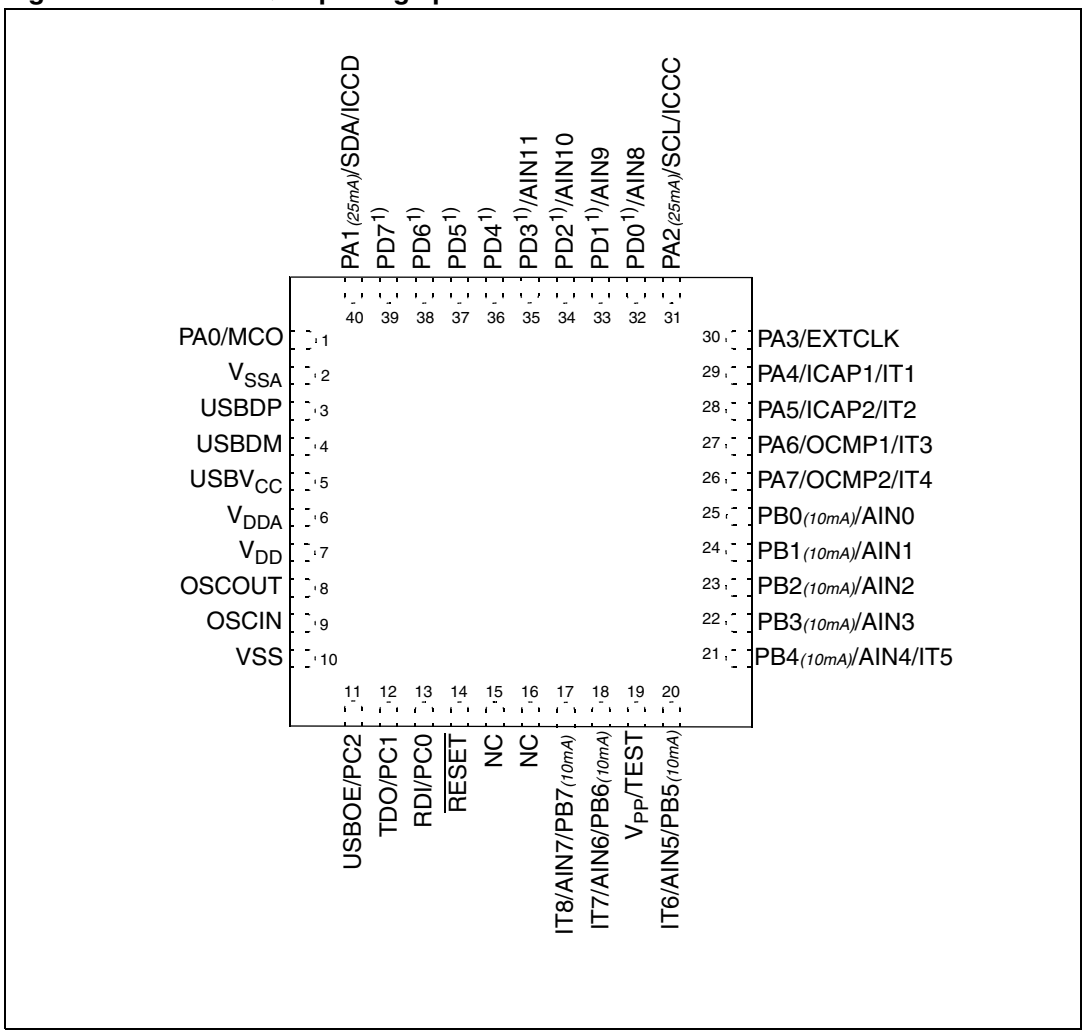


Figure 3. 40-lead QFN package pinout



1. Port D functions are not available on the 8 Kbyte version of the QFN40 package (ST7263BK2) and should not be connected.

Figure 4. 34-pin SO package pinout

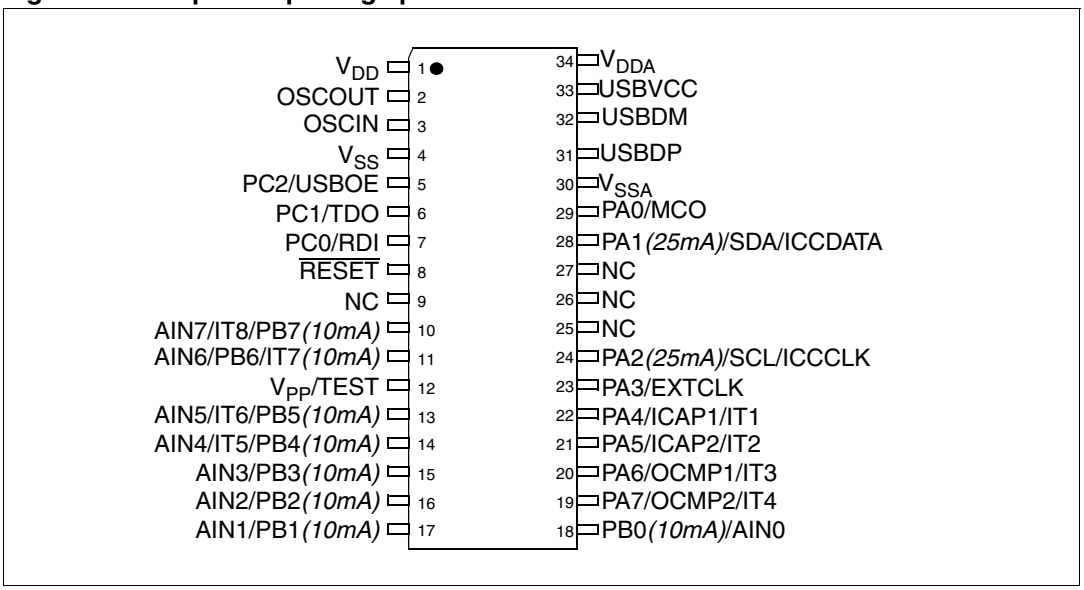


Figure 5. 32-pin SDIP package pinout

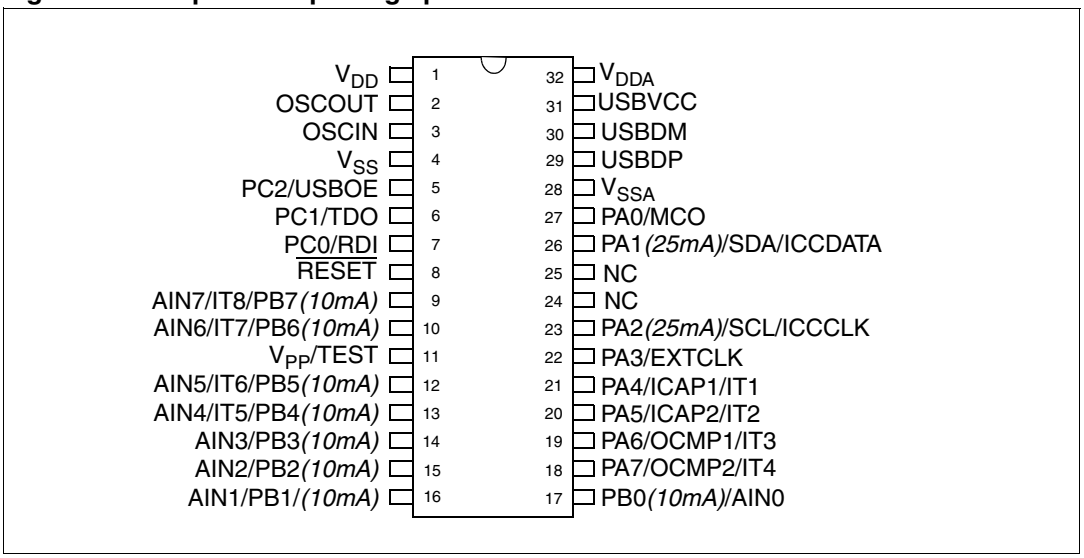
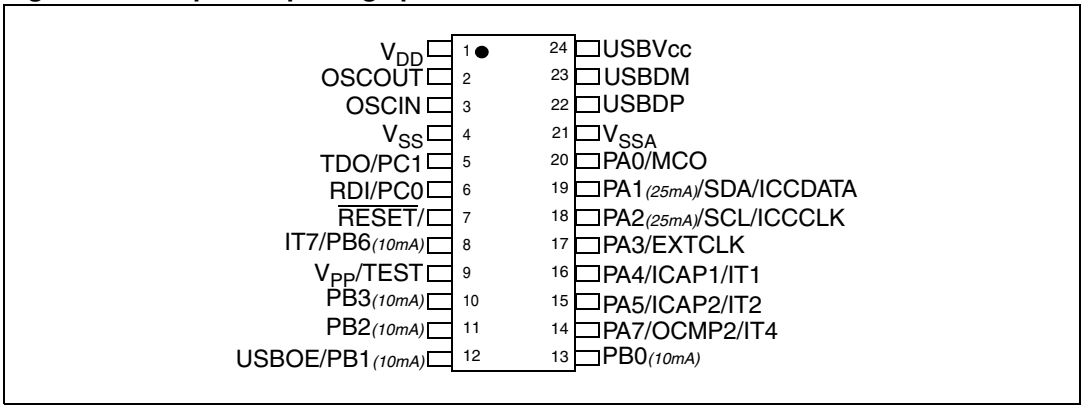


Figure 6. 24-pin SO package pinout



Legend / Abbreviations for *Table 3* and *Table 4*:

Type: I = input, O = output, S = supply

In/Output level: C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: 10 mA = 10mA high sink (Fn N-buffer only)

25 mA = 25 mA very high sink (on N-buffer only)
Port and control configuration:

- Input:float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull, T = True open drain

The RESET configuration of each pin is shown in bold. This configuration is kept as long as the device is under reset state.

Table 3. Device pin description (QFN40, LQFP48, SO34 and SDIP32)

Pin n°				Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
								Input				Output			
SDIP32	SO34	QFN40	LQFP48			Input	Output	float	wpu	int	ana	OD	PP		
1	1	7	6	V_{DD}	S									Power supply voltage (4- 5.5 V)	
2	2	8	7	OSCOUT	O									Oscillator output	
3	3	9	8	OSCIN	I									Oscillator input	
4	4	10	9	V_{SS}	S									Digital ground	
5	5	11	10	PC2/USBOE	I/O	CT			X				X	Port C2	USB output Enable
6	6	12	13	PC1/TDO	I/O	CT			X				X	Port C1	SCI Transmit Data output
7	7	13	14	PC0/RDI	I/O	CT			X				X	Port C0	SCI Receive Data input
8	8	14	15	$\overline{\text{RESET}}$	I/O				X			X		Reset	
-	9	15	16	NC	--									Not connected	
-	-	16	17	NC	--									Not connected	
-	-	-	18	NC	--									Not connected	
-	-	-	19	NC	--									Not connected	
-	-	-	20	NC	--									Not connected	
-	-	-	21	NC	--									Not connected	
-	-	-	22	NC	--									Not connected	
9	10	17	23	PB7/AIN7/IT8	I/O	CT	10mA	X		X	X		X	Port B7	ADC analog input 7
10	11	18	24	PB6/AIN6/IT7	I/O	CT	10mA	X		X	X		X	Port B6	ADC analog input 6
11	12	19	25	V_{PP}/TEST	S									Programming supply	
12	13	20	26	PB5/AIN5/IT6	I/O	CT	10mA	X		X	X		X	Port B5	ADC analog input 5
13	14	21	27	PB4/AIN4/IT5	I/O	CT	10mA	X		X	X		X	Port B4	ADC analog input 4
14	15	22	28	PB3/AIN3	I/O	CT	10mA	X			X		X	Port B3	ADC analog input 3

Table 3. Device pin description (QFN40, LQFP48, SO34 and SDIP32) (continued)

Pin n°				Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
								Input				Output			
SDIP32	SO34	QFN40	LQFP48			Input	Output	float	wpu	int	ana	OD	PP		
15	16	23	29	PB2/AIN2	I/O	CT	10mA	X			X		X	Port B2	ADC analog input 2
16	17	24	30	PB1/AIN1	I/O	CT	10mA	X			X		X	Port B1	ADC analog input 1
17	18	25	31	PB0/AIN0	I/O	CT	10mA	X			X		X	Port B0	ADC analog input 0
18	19	26	32	PA7/OCMP2/IT4	I/O	CT			X	X			X	Port A7	Timer output Compare 2
19	20	27	33	PA6/OCMP1/IT3	I/O	CT			X	X			X	Port A6	Timer output Compare 1
20	21	28	34	PA5/ICAP2/IT2	I/O	CT			X	X			X	Port A5	Timer input Capture 2
21	22	29	35	PA4/ICAP1/IT1	I/O	CT			X	X			X	Port A4	Timer input Capture 1
22	23	30	36	PA3/EXTCLK	I/O	CT			X				X	Port A3	Timer External clock
23	24	31	38	PA2/SCL/ICCCLK	I/O	C_T	25mA	X				T		Port A2	I²C serial clock, ICC clock
-	-	32	39	PD0(1)/AIN8	I/O	C_T		X			X		X	Port D0	ADC analog input 8
-	-	33	40	PD1(1)/AIN9	I/O	C_T		X			X		X	Port D1	ADC analog input 9
-	-	34	41	PD2(1)/AIN10	I/O	C_T		X			X		X	Port D2	ADC analog input 10
-	-	35	42	PD3(1)/AIN11	I/O	C_T		X			X		X	Port D3	ADC analog input 11
-	-	36	43	PD4(1)	I/O	C_T			X				X	Port D4	
-	-	37	44	PD5(1)	I/O	C_T			X				X	Port D5	
-	-	38	45	PD6(1)	I/O	C_T			X				X	Port D6	
-	-	39	46	PD7(1)	I/O	C_T			X				X	Port D7	
-	25	-	-	NC	--									Not connected	
24	26	-	-	NC	--									Not connected	
25	27	-	-	NC	--									Not connected	
26	28	40	47	PA1/SDA/ICCDATA	I/O	CT	25mA	X				T		Port A1	I²C serial data, ICC data
27	29	1	48	PA0/MCO	I/O	CT				X			X	Port A0	Main clock output
28	30	2	1	V_{SSA}	S									Analog ground	
29	31	3	2	USBDP	I/O									USB bidirectional data (data +)	
30	32	4	3	USBDM	I/O									USB bidirectional data (data -)	

Table 3. Device pin description (QFN40, LQFP48, SO34 and SDIP32) (continued)

Pin n°				Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
								Input				Output			
SDIP32	SO34	QFN40	LQFP48			Input	Output	float	wpu	int	ana	OD	PP		
31	33	5	4	USBVCC(2)	O									USB power supply 2)	
32	34	6	5	V_{DDA}	S									Analog supply voltage	

1. Port D functions are not available on the 8 Kbyte version of the QFN40 package (ST7263BK2) and should not be connected.
2. The drive from USBVcc is sufficient to only drive an external pull-up in addition to the internal transceiver.

Table 4. Device pin description (SO24)

Pin n°	Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
					Input				Output			
SO24			Input	Output	float	wpu	int	ana	OD	PP		
1	V_{DD}	S									Power supply voltage (4- 5.5 V)	
2	OSCOUT	O									Oscillator output	
3	OSCIN	I									Oscillator input	
4	V_{SS}	S									Digital ground	
5	PC1/TDO	I/O	CT			X				X	Port C1	SCI Transmit Data output
6	PC0/RDI	I/O	CT			X				X	Port C0	SCI Receive Data input
7	$\overline{\text{RESET}}$	I/O				X			X		Reset	
8	PB6/IT7	I/O	CT	10mA	X		X	X		X	Port B6	
9	V_{PP}/TEST	S									Programming supply	
10	PB3	I/O	CT	10mA	X			X		X	Port B3	
11	PB2	I/O	CT	10mA	X			X		X	Port B2	
12	PB1/USBOE	I/O	CT	10mA	X			X		X	Port B1	USB output Enable
13	PB0	I/O	CT	10mA	X			X		X	Port B0	
14	PA7/OCMP2/IT4	I/O	CT			X	X			X	Port A7	Timer output Compare 2
15	PA5/ICAP2/IT2	I/O	CT			X	X			X	Port A5	Timer input Capture 2
16	PA4/ICAP1/IT1	I/O	CT			X	X			X	Port A4	Timer input Capture 1
17	PA3/EXTCLK	I/O	CT			X				X	Port A3	Timer External clock
18	PA2/SCL/ ICCCLK	I/O	C_T	25mA	X				T		Port A2	I²C serial clock, ICC clock
19	PA1/SDA/ICCDATA	I/O	CT	25mA	X				T		Port A1	I²C serial data, ICC Data

Table 4. Device pin description (SO24) (continued)

Pin n°	Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
					Input				Output			
SO24			Input	Output	float	wpu	int	ana	OD	PP		
20	PA0/MCO	I/O	CT				X			X	Port A0	Main Clock output
21	V_{SSA}	S									Analog ground	
22	USBDP	I/O									USB bidirectional data (data +)	
23	USBDM	I/O									USB bidirectional data (data -)	
24	USBVCC	O									USB power supply	

3 Register and memory map

As shown in *Figure 7*, the MCU is capable of addressing 32 Kbytes of memories and I/O registers.

The available memory locations consist of up to 1024 bytes of RAM including 64 bytes of register locations, and up to 32K bytes of user program memory in which the upper 32 bytes are reserved for interrupt vectors. The RAM space includes up to 128 bytes for the stack from 0100h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

Caution: Memory locations noted “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 7. Memory map

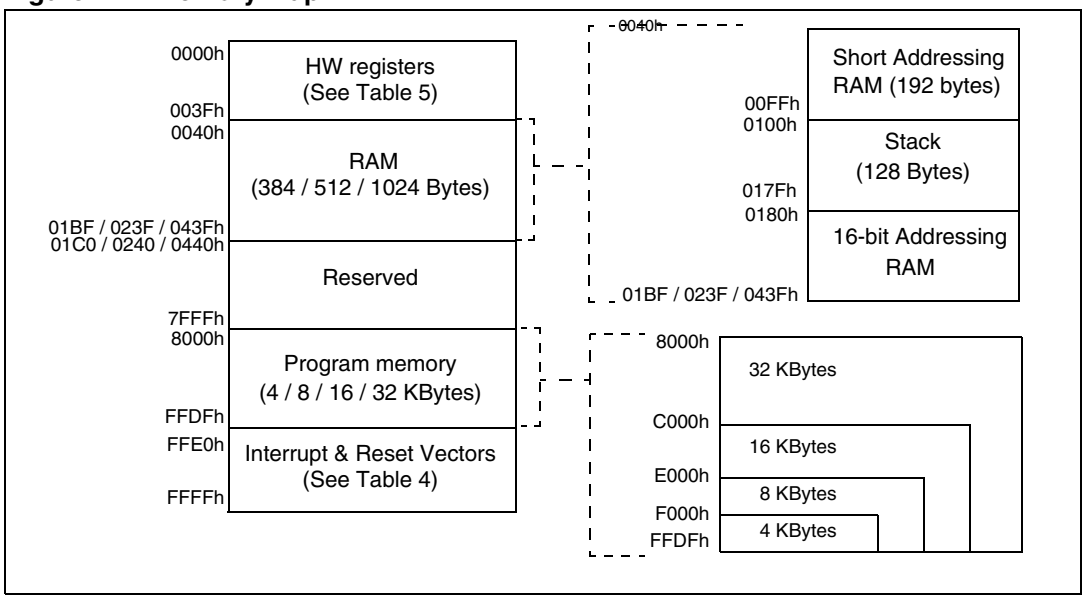


Table 5. Interrupt vector map

Vector address	Description	Masked	Remarks	Exit from Halt
FFE0h-FFEDh	Reserved area			
FFEEh-FFEFh	USB interrupt vector	I- bit	Internal interrupt	No
FFF0h-FFF1h	SCI interrupt vector	I- bit	Internal interrupt	No
FFF2h-FFF3h	I²C interrupt vector	I- bit	Internal interrupt	No
FFF4h-FFF5h	TIMER interrupt vector	I- bit	Internal interrupt	No
FFF6h-FFF7h	IT1 to IT8 interrupt vector	I- bit	External interrupt	Yes
FFF8h-FFF9h	USB End Suspend mode interrupt vector	I- bit	External interrupts	Yes
FFFAh-FFFBh	Flash start programming interrupt vector	I- bit	Internal interrupt	Yes
FFFCh-FFFDh	TRAP (software) interrupt vector	None	CPU interrupt	No
FFFEh-FFFFh	RESET vector	None		Yes

Table 6. Hardware register memory map

Address	Block	Register label	Register name	Reset status	Remarks
0000h 0001h	Port A	PADR PADDR	Port A Data register Port A Data Direction register	00h 00h	R/W R/W
0002h 0003h	Port B	PBDR PBDDR	Port B Data register Port B Data Direction register	00h 00h	R/W R/W
0004h 0005h	Port C	PCDR PCDDR	Port C Data register Port C Data Direction register	1111 x000b 1111 x000b	R/W R/W
0006h 0007h	Port D	PDDR PDDDR	Port D Data register Port D Data Direction register	00h 00h	R/W R/W
0008h	ITC	ITIFRE	Interrupt register	00h	R/W
0009h	MISC	MISCR	Miscellaneous register	00h	R/W
000Ah 000Bh	ADC	ADCDR ADCCSR	ADC Data register ADC control Status register	00h 00h	Read only R/W
000Ch	WDG	WDGCR	Watchdog Control register	7Fh	R/W
000Dh to 0010h	Reserved (4 bytes)				
0011h 0012h 0013h 0014h 0015h 0016h 0017h 0018h 0019h 001Ah 001Bh 001Ch 001Dh 001Eh 001Fh	TIM	TCR2 TCR1 TCSR TIC1HR TIC1LR TOC1HR TOC1LR TCHR TCLR TACHR TACLR TIC2HR TIC2LR TOC2HR TOC2LR	Timer Control register 2 Timer Control register 1 Timer Control/Status register Timer input Capture High register 1 Timer input Capture Low register 1 Timer output Compare High register 1 Timer output Compare Low register 1 Timer Counter High register Timer Counter Low register Timer Alternate Counter High register Timer Alternate Counter Low register Timer input Capture High register 2 Timer input Capture Low register 2 Timer output Compare High register 2 Timer output Compare Low register 2	00h 00h 00h xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read only Read only R/W R/W Read only R/W Read only R/W Read only Read only R/W R/W
0020h 0021h 0022h 0023h 0024h	SCI	SCISR SCIDR SCIBRR SCICR1 SCICR2	SCI Status register SCI Data register SCI Baud Rate register SCI Control register 1 SCI Control register 2	C0h xxh 00h x000 0000b 00h	Read only R/W R/W R/W R/W

Table 6. Hardware register memory map (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0025h	USB	USBPIDR	USB PID register	x0h	Read only
0026h		USBDMAR	USB DMA address register	xxh	R/W
0027h		USBIDR	USB Interrupt/DMA register	x0h	R/W
0028h		USBISTR	USB Interrupt Status register	00h	R/W
0029h		USBIMR	USB Interrupt Mask register	00h	R/W
002Ah		USBCTLR	USB Control register	06h	R/W
002Bh		USBDADDR	USB Device Address register	00h	R/W
002Ch		USBEP0RA	USB Endpoint 0 register A	0000 xxxxb	R/W
002Dh		USBEP0RB	USB Endpoint 0 register B	80h	R/W
002Eh		USBEP1RA	USB Endpoint 1 register A	0000 xxxxb	R/W
002Fh		USBEP1RB	USB Endpoint 1 register B	0000 xxxxb	R/W
0030h		USBEP2RA	USB Endpoint 2 register A	0000 xxxxb	R/W
0031h		USBEP2RB	USB Endpoint 2 register B	0000 xxxxb	R/W
0032h to 0036h	Reserved (5 bytes)				
0032h 0036h	Reserved (5 Bytes)				
0037h	Flash	FCSR	Flash Control /Status register	00h	R/W
0038h	Reserved (1 byte)				
0039h	I²C	I2CDR	I²C Data register	00h	R/W
003Ah			Reserved	-	
003Bh		I2COAR	I²C (7 Bits) Slave Address register	00h	R/W
003Ch		I2CCCR	I²C Clock Control register	00h	R/W
003Dh		I2CSR2	I²C 2nd Status register	00h	Read only
003Eh		I2CSR1	I²C 1st Status register	00h	Read only
003Fh		I2CCR	I²C Control register	00h	R/W

4 Flash program memory

4.1 Introduction

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a byte-by-byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (in-circuit programming) or IAP (in-application programming).

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (in-circuit programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (in-application programming). In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Readout protection
- Register access security system (RASS) to prevent accidental programming or erasing

4.3 Structure

The Flash memory is organized in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see *Table 7*). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see *Figure 8*). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 7. Sectors available in Flash devices

Flash size (Kbytes)	Available sectors
4	Sector 0
8	Sectors 0,1
> 8	Sectors 0,1, 2

4.3.1 Readout protection

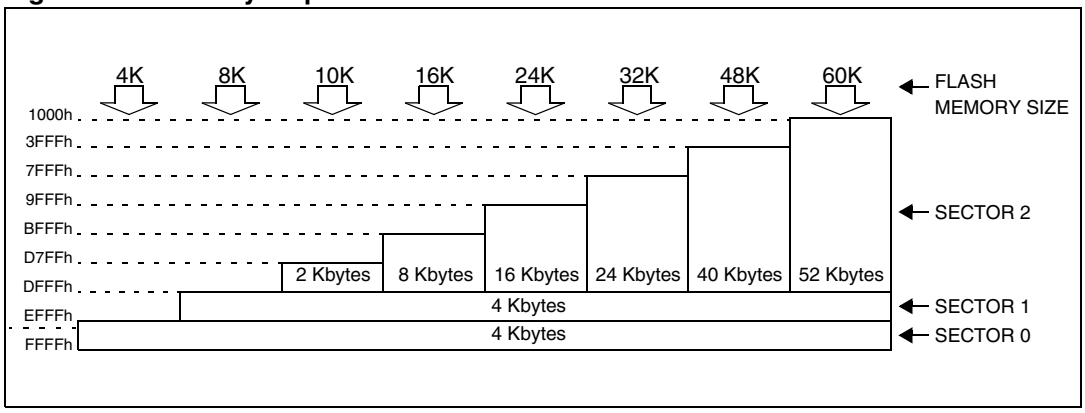
Readout protection, when selected, provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

In Flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased and the device can be reprogrammed.

Readout protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the Option List.

Figure 8. Memory map and sector address



4.4 ICC interface

ICC (In-circuit communication) needs a minimum of four and up to six pins to be connected to the programming tool (see *Figure 9*). These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input/output serial data pin
- ICCSEL/V_{PP}: programming voltage
- OSC1(or OSCIN): main clock input for external source (optional)
- V_{DD}: application board power supply (see *Figure 9*, Note 3)