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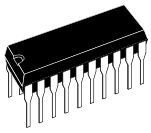
ST7LITE20F2 ST7LITE25F2 ST7LITE29F2

8-bit microcontroller with single voltage Flash memory, data EEPROM, ADC, Timers, SPI

Datasheet - production data

Features

- Memories
  - 8 Kbytes single voltage Flash Program memory with Read-out protection
  - In-circuit programming and in-application programming (ICP and IAP)
  - 10K write/erase cycles guaranteed
  - Data retention: 20 years at 55 °C
  - Temperature ranges:
  - -40 °C to +85 °C
  - -40 °C to +105 °C
  - 384 bytes RAM
- Clock, reset and supply management
  - Enhanced reset system
  - Enhanced low voltage supervisor (LVD) for main supply and an auxiliary voltage detector (AVD) with interrupt capability for implementing safe power-down procedures
  - Clock sources: internal 1% RC oscillator, crystal/ceramic resonator or external clock
  - Internal 32-MHz input clock for auto-reload timer
  - Optional x4 or x8 PLL for 4 or 8 MHz internal clock
  - Five power saving modes: Halt, Active-halt, Wait and Slow, Auto-wakeup from Halt
- I/O ports
  - Up to 15 multifunctional bidirectional I/O lines
  - 7 high sink outputs
- 4 timers
  - Configurable watchdog timer
  - Two 8-bit Lite timers with prescaler
  - 1 real-time base and 1 input capture
  - One 12-bit auto-reload timer with 4 PWM outputs, input capture and output compare functions



DIP20

SO20 300”

- 1 communication interface
  - SPI synchronous serial interface.
- Interrupt management
  - 10 interrupt vectors plus TRAP and RESET
  - 15 external interrupt lines (on 4 vectors)
- A/D converter
  - 7 input channels
  - Fixed gain op-amp
  - 13-bit resolution for 0 to 430 mV (@ 5 V V_{DD})
  - 10-bit resolution for 430 mV to 5 V (@ 5 V V_{DD})
- Instruction set
  - 8-bit data manipulation
  - 63 basic instructions with illegal opcode detection
  - 17 main addressing modes
  - 8 x 8 unsigned multiply instructions
- Development tools
  - Full hardware/software development package
  - DM (debug module)

Contents

1 **Description 13**

2 **Pin description 15**

3 **Register & memory map 18**

4 **Flash program memory 21**

4.1 Introduction 21

4.2 Main features 21

4.3 Programming modes 21

4.3.1 In-circuit programming (ICP) 21

4.3.2 In-application programming (IAP) 22

4.4 ICC interface 22

4.5 Memory protection 23

4.5.1 Read-out protection 23

4.5.2 Flash write/erase protection 23

4.6 Related documentation 24

4.7 Register description 24

5 **Data EEPROM 25**

5.1 Introduction 25

5.2 Main features 25

5.3 Memory access 25

5.4 Power saving modes 27

5.5 Access error handling 27

5.6 Data EEPROM Read-out protection 28

5.7 Register description 28

6 **Central processing unit 30**

6.1 Introduction 30

6.2 Main features 30

6.3 CPU registers 30

7 Supply, reset and clock management 34

7.1 Internal RC oscillator adjustment 34

7.2 Phase locked loop (PLL) 35

7.3 Register description 36

7.4 Multi-oscillator (MO) 37

7.5 Reset sequence manager (RSM) 39

7.5.1 Introduction 39

7.5.2 Asynchronous external $\overline{\text{RESET}}$ pin 40

7.5.3 External power-on RESET 40

7.5.4 Internal low voltage detector (LVD) RESET 40

7.5.5 Internal watchdog RESET 41

7.6 System integrity management (SI) 41

7.6.1 Low voltage detector (LVD) 41

7.6.2 Auxiliary Voltage Detector (AVD) 43

7.6.3 Low power modes 44

7.6.4 Register description 45

8 Interrupts 47

8.1 Non maskable software interrupt 47

8.2 External interrupts 47

8.3 Peripheral interrupts 48

9 Power saving modes 53

9.1 Introduction 53

9.2 SLOW mode 53

9.3 WAIT mode 54

9.4 HALT mode 55

9.4.1 HALT mode recommendations 57

9.5 ACTIVE-HALT mode 58

9.6 Auto-wakeup from HALT mode 60

9.6.1 Register description 62

10 I/O ports 64

10.1 Introduction 64

10.2 Functional description 64

10.2.1 Input modes . . . 64
10.2.2 Output modes . . . 65
10.2.3 Alternate functions . . . 66
10.3 I/O port implementation . . . 68
10.4 Unused I/O pins . . . 69
10.5 Low power modes . . . 69
10.6 Interrupts . . . 69
10.7 Device-specific I/O port configuration . . . 69

11 On-chip peripherals . . . 72
11.1 Watchdog timer (WDG) . . . 72
11.1.1 Introduction . . . 72
11.1.2 Main features . . . 72
11.1.3 Functional description . . . 72
11.1.4 Hardware watchdog option . . . 73
11.1.5 Interrupts . . . 73
11.1.6 Register description . . . 74
11.2 12-bit autoreload timer 2 (AT2) . . . 74
11.2.1 Introduction . . . 74
11.2.2 Main features . . . 75
11.2.3 Functional description . . . 75
11.2.4 Low power modes . . . 79
11.2.5 Interrupts . . . 79
11.2.6 Register description . . . 80
11.3 Lite timer 2 (LT2) . . . 86
11.3.1 Introduction . . . 86
11.3.2 Main features . . . 86
11.3.3 Functional description . . . 87
11.3.4 Low power modes . . . 88
11.3.5 Interrupts . . . 88
11.3.6 Register description . . . 88
11.4 Serial peripheral interface (SPI) . . . 91
11.4.1 Introduction . . . 91
11.4.2 Main features . . . 91
11.4.3 General description . . . 91
11.4.4 Clock phase and clock polarity . . . 95

11.4.5 Error Flags . . . 96
11.4.6 Low power modes . . . 99
11.4.7 Interrupts . . . 100
11.4.8 Register description . . . 100
11.5 10-bit A/D converter (ADC) . . . 103
11.5.1 Introduction . . . 103
11.5.2 Main features . . . 104
11.5.3 Functional description . . . 104
11.5.4 Low power modes . . . 106
11.5.5 Interrupts . . . 106
11.5.6 Register Description . . . 106

12 Instruction set . . . 110
12.1 ST7 addressing modes . . . 110
12.1.1 Inherent . . . 111
12.1.2 Immediate . . . 112
12.1.3 Direct . . . 112
12.1.4 Indexed (no offset, short, long) . . . 112
12.1.5 Indirect (short, long) . . . 113
12.1.6 Indirect indexed (short, long) . . . 113
12.1.7 Relative mode (direct, indirect) . . . 114
12.2 Instruction groups . . . 114
12.2.1 Illegal opcode reset . . . 115

13 Electrical characteristics . . . 118
13.1 Parameter conditions . . . 118
13.1.1 Minimum and maximum values . . . 118
13.1.2 Typical values . . . 118
13.1.3 Typical curves . . . 118
13.1.4 Loading capacitor . . . 118
13.1.5 Pin input voltage . . . 118
13.2 Absolute maximum ratings . . . 119
13.3 Operating conditions . . . 121
13.3.1 General operating conditions . . . 121
13.3.2 Operating conditions with low voltage detector (LVD) . . . 121
13.3.3 Auxiliary voltage detector (AVD) thresholds . . . 123
13.3.4 Internal RC oscillator and PLL . . . 123

13.4 Supply current characteristics . . . 127
13.5 Clock and timing characteristics . . . 130
13.5.1 Crystal and ceramic resonator oscillators . . . 131
13.6 Memory characteristics . . . 133
13.7 EMC characteristics . . . 134
13.7.1 Functional EMS (Electro Magnetic Susceptibility) . . . 134
13.7.2 Electro Magnetic Interference (EMI) . . . 135
13.7.3 Absolute maximum ratings (Electrical sensitivity) . . . 136
13.8 I/O port pin characteristics . . . 137
13.9 Control pin characteristics . . . 143
13.10 Communication interface characteristics . . . 145
13.10.1 Serial peripheral interface (SPI) . . . 145
13.11 10-Bit ADC characteristics . . . 147
13.11.1 Amplifier output offset variation . . . 150

14 Package characteristics . . . 151
14.1 Package mechanical data . . . 151
14.2 Soldering information . . . 153

15 Device configuration . . . 154
15.1 Option bytes . . . 154
15.1.1 Option byte 0 . . . 154
15.1.2 Option byte 1 . . . 156
15.2 Device ordering information and transfer of customer code . . . 157
15.3 Development tools . . . 160
15.4 Application notes . . . 161

16 Important notes . . . 165
16.1 Execution of BTJX instruction . . . 165
16.2 ADC conversion spurious results . . . 165
16.3 A/D converter accuracy for first conversion . . . 165
16.4 Negative injection impact on ADC accuracy . . . 165
16.5 Clearing active interrupts outside interrupt routine . . . 165
16.6 Using PB4 as external interrupt . . . 166
16.7 Timebase 2 interrupt in slow mode . . . 166

17 Revision history 167

List of tables

Table 1. Device summary . . . 13
Table 2. Device pin description . . . 16
Table 3. Hardware register map . . . 19
Table 4. Row definition . . . 27
Table 5. DATA EEPROM register map and reset values . . . 29
Table 6. Predefined calibration values . . . 34
Table 7. ST7 clock sources . . . 38
Table 8. CPU clock cycle delay . . . 39
Table 9. Effect of low power modes on SI . . . 44
Table 10. Interrupt control bits . . . 44
Table 11. Flag description . . . 45
Table 12. Interrupt mapping . . . 49
Table 13. Interrupt sensitivity bits . . . 50
Table 14. External interrupt I/O pin ei3[1:0] selection . . . 51
Table 15. External interrupt I/O pin ei2[1:0] selection . . . 51
Table 16. External interrupt I/O pin ei1[1:0] selection . . . 52
Table 17. External interrupt I/O pin ei0[1:0] selection . . . 52
Table 18. ACTIVE-HALT mode . . . 58
Table 19. AWU prescaler . . . 63
Table 20. AWU register map and reset values . . . 63
Table 21. DR value and output pin status . . . 65
Table 22. I/O port mode options . . . 67
Table 23. I/O configurations . . . 67
Table 24. Effect of low power modes on I/O ports . . . 69
Table 25. I/O port interrupt control/wake-up capability . . . 69
Table 26. Ports PA7:0, PB6:0 . . . 69
Table 27. Port configuration (standard ports) . . . 70
Table 28. Port configuration (Interrupt ports) . . . 70
Table 29. Ports where the external interrupt capability selected using the EISR register . . . 70
Table 30. I/O port register map and reset values . . . 70
Table 31. Watchdog timing . . . 73
Table 32. Watchdog timer register map and reset values . . . 74
Table 33. Effect of low power modes . . . 79
Table 34. Interrupts events . . . 79
Table 35. Counter clock selection . . . 80
Table 36. Register map and reset values . . . 84
Table 37. Effect of low power modes on Lite timer . . . 88
Table 38. TBxF and ICF interrupt events . . . 88
Table 39. Lite timer register map and reset values . . . 90
Table 40. WAIT and HALT mode description . . . 99
Table 41. Interrupt events . . . 100
Table 42. SPI master mode SCK frequency . . . 101
Table 43. SPI register map and reset values . . . 103
Table 44. Low power modes effects . . . 106
Table 45. Channel selection bits . . . 106
Table 46. ADC clock speed selection . . . 108
Table 47. ADC register map and reset values . . . 109
Table 48. Addressing mode groups . . . 110

Table 49. ST7 addressing mode overview . . . 110
Table 50. Inherent instructions . . . 111
Table 51. Immediate instructions . . . 112
Table 52. Long and short instructions supporting direct, indexed, indirect and indirect indexed addressing modes . . . 113
Table 53. Short instructions supporting direct, indexed, indirect and indirect indexed addressing modes . . . 114
Table 54. Relative direct and indirect instructions and functions . . . 114
Table 55. Instruction groups . . . 114
Table 56. Instruction set overview . . . 116
Table 57. Voltage characteristics . . . 119
Table 58. Current characteristics . . . 119
Table 59. Thermal characteristics . . . 120
Table 60. General operating conditions . . . 121
Table 61. Power on/power down operating conditions . . . 121
Table 62. AVD thresholds . . . 123
Table 63. Internal RC oscillator and PLL . . . 123
Table 64. RC oscillator and PLL characteristics (tested for TA = -40 to +85°C) @ VDD = 4.5 to 5.5 V . . . 124
Table 65. 32 MHz PLL . . . 127
Table 66. Supply current . . . 128
Table 67. On-chip peripherals . . . 130
Table 68. General timings . . . 130
Table 69. Auto Wakeup from Halt Oscillator (AWU) . . . 131
Table 70. Resonator characteristics . . . 132
Table 72. Resonator performances . . . 133
Table 73. RAM and hardware registers . . . 133
Table 74. Flash program memory . . . 133
Table 75. EEPROM data memory . . . 134
Table 76. Test results . . . 135
Table 77. Emission test . . . 136
Table 78. Absolute maximum ratings . . . 136
Table 79. Electrical sensitivities . . . 137
Table 80. General characteristics . . . 137
Table 81. Output driving current . . . 139
Table 82. Asynchronous $\overline{\text{RESET}}$ Pin . . . 143
Table 83. Serial peripheral interface (SPI) . . . 145
Table 84. 10-bit ADC characteristics . . . 147
Table 85. ADC accuracy with V_{DD} = 5.0V . . . 148
Table 86. ADC characteristics . . . 150
Table 87. Typical offset variation over temperature . . . 150
Table 88. Small outline package characteristics . . . 151
Table 89. Dual in-line package characteristics . . . 152
Table 90. Thermal characteristics . . . 153
Table 91. Soldering compatibility (wave and reflow soldering process) . . . 153
Table 92. Option bytes values . . . 154
Table 93. Size definition . . . 155
Table 94. Option byte default values . . . 155
Table 95. LVD threshold configuration . . . 156
Table 96. List of valid option combinations . . . 157
Table 97. Supported part numbers . . . 158
Table 98. ST7LITE2 FASTROM microcontroller option list . . . 159

Table 99. STMicroelectronics development tools 161
Table 100. ST7 application notes 161
Table 101. Revision history 167

List of figures

Figure 1. General block diagram . . . 14
Figure 2. 20-pin SO package pinout . . . 15
Figure 3. 20-pin DIP package pinout . . . 15
Figure 4. Memory map . . . 18
Figure 5. Typical ICC interface . . . 23
Figure 6. EEPROM block diagram . . . 25
Figure 7. Data EEPROM programming flowchart . . . 26
Figure 8. Data EEPROM Write operation . . . 27
Figure 9. Data EEPROM programming cycle . . . 28
Figure 10. CPU registers . . . 30
Figure 11. Stack manipulation example . . . 33
Figure 12. PLL output frequency timing diagram . . . 35
Figure 13. Clock management block diagram . . . 37
Figure 14. RESET sequence phases . . . 39
Figure 15. Reset block diagram . . . 40
Figure 16. RESET sequences . . . 41
Figure 17. Low voltage detector vs. Reset . . . 42
Figure 18. Reset and supply management block diagram . . . 43
Figure 19. Using the AVD to monitor VDD . . . 44
Figure 20. Interrupt processing flowchart . . . 48
Figure 21. Power saving mode transitions . . . 53
Figure 22. SLOW mode clock transition . . . 54
Figure 23. WAIT mode flowchart . . . 55
Figure 24. HALT timing overview . . . 56
Figure 25. HALT mode flowchart . . . 57
Figure 26. ACTIVE-HALT timing overview . . . 59
Figure 27. ACTIVE-HALT mode Flow-chart . . . 59
Figure 28. AWUF mode block diagram . . . 60
Figure 29. AWUF halt timing diagram . . . 61
Figure 30. AWUF mode flowchart . . . 61
Figure 31. I/O port general block diagram . . . 66
Figure 32. Interrupt I/O port state transitions . . . 69
Figure 33. Watchdog block diagram . . . 72
Figure 34. Block diagram . . . 75
Figure 35. PWM inversion diagram . . . 76
Figure 36. PWM function . . . 77
Figure 37. PWM signal from 0% to 100% duty cycle . . . 77
Figure 38. Block diagram of break function . . . 78
Figure 39. Input capture timing diagram . . . 79
Figure 40. Lite timer 2 block diagram . . . 86
Figure 41. Input capture timing diagram . . . 87
Figure 42. Serial peripheral interface block diagram . . . 92
Figure 43. Single master/ single slave application . . . 93
Figure 44. Generic SS timing diagram . . . 93
Figure 45. Hardware/software slave select management . . . 94
Figure 46. Data clock timing diagram . . . 96
Figure 47. Clearing the WCOL bit (write collision flag) software sequence . . . 98
Figure 48. Single master / multiple slave configuration . . . 99

Figure 49. ADC block diagram . . . 104
Figure 50. Pin loading conditions . . . 118
Figure 51. Pin input voltage . . . 119
Figure 52. fCPU maximum operating frequency versus V_{DD} supply voltage . . . 121
Figure 53. RC Osc Freq vs VDD @ TA= 25°C (calibrated with RCCR1: 3V @ 25°C) . . . 125
Figure 54. RC Osc Freq vs VDD (calibrated with RCCR0: 5V@ 25°C) . . . 126
Figure 55. Typical RC oscillator Accuracy vs temperature @ VDD=5V (calibrated with RCCR0: 5V @ 25°C) . . . 126
Figure 56. RC Osc Freq vs VDD and RCCR Value . . . 126
Figure 57. PLL DfCPU/fCPU versus time . . . 126
Figure 58. PLLx4 Output vs CLKIN frequency . . . 127
Figure 59. PLLx8 Output vs CLKIN frequency . . . 127
Figure 60. Tipical IDD in RUN vs. fCPU . . . 128
Figure 61. Typical IDD in SLOW vs. fCPU . . . 129
Figure 62. Typical IDD in WAIT vs. fCPU . . . 129
Figure 63. Typical IDD in SLOW-WAIT vs. fCPU . . . 129
Figure 64. Typical IDD in AWUF mode at TA = 25°C . . . 129
Figure 65. Typical IDD vs. temperature at VDD = 5V and fCPU = 8MHz . . . 130
Figure 66. Typical application with a crystal or ceramic resonator . . . 133
Figure 67. Two typical applications with unused I/O Pin . . . 138
Figure 68. Typical I_{PU} vs. V_{DD} with V_{IN} =VSS . . . 138
Figure 69. Typical VOL at VDD = 2.4V (standard) . . . 139
Figure 70. Typical V_{OL} at V_{DD} = 2.7V (standard) . . . 140
Figure 71. Typical VOL at VDD = 3.3V (standard) . . . 140
Figure 72. Typical VOL at VDD = 5V (standard) . . . 140
Figure 73. Typical VOL at VDD = 2.4V (high-sink) . . . 140
Figure 74. Typical VOL at VDD = 5V (high-sink) . . . 141
Figure 75. Typical VOL at VDD = 3V (high-sink) . . . 141
Figure 76. Typical VDD-VOH at VDD = 2.4V . . . 141
Figure 77. Typical VDD-VOH at VDD = 2.7V . . . 141
Figure 78. Typical VDD-VOH at VDD = 3V . . . 142
Figure 79. Typical VDD-VOH at VDD = 4V . . . 142
Figure 80. Typical VDD-VOH at VDD = 5V . . . 142
Figure 81. VOL vs. VDD (standard I/Os) . . . 142
Figure 82. Typical VOL vs. VDD (high-sink I/Os) . . . 143
Figure 83. Typical VDD-VOH vs. VDD . . . 143
Figure 84. RESET pin protection when LVD is enabled . . . 144
Figure 85. RESET pin protection when LVD is disabled . . . 144
Figure 86. SPI slave timing diagram with CPHA = 0(1) . . . 146
Figure 87. SPI slave timing diagram with CPHA = 1(1) . . . 146
Figure 88. SPI master timing diagram(1) . . . 147
Figure 89. Typical application with ADC . . . 148
Figure 90. ADC accuracy characteristics with amplifier disabled . . . 149
Figure 91. ADC accuracy characteristics with amplifier enabled . . . 149
Figure 92. Amplifier noise vs voltage . . . 150
Figure 93. 20-pin plastic small outline package, 300-mil width . . . 151
Figure 94. 20-pin plastic dual in-line package, 300-mil width . . . 152

1 Description

ST7LITE20F2, ST7LITE25F2 and ST7LITE29F2 are referred to as ST7LITE2. The ST7LITE2 is a member of the ST7 microcontroller family. All ST7 devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

The ST7LITE2 features FLASH memory with byte-by-byte In-Circuit Programming (ICP) and In-Application Programming (IAP) capability.

Under software control, the ST7LITE2 device can be placed in WAIT, SLOW, or HALT mode, reducing power consumption when the application is in idle or standby state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

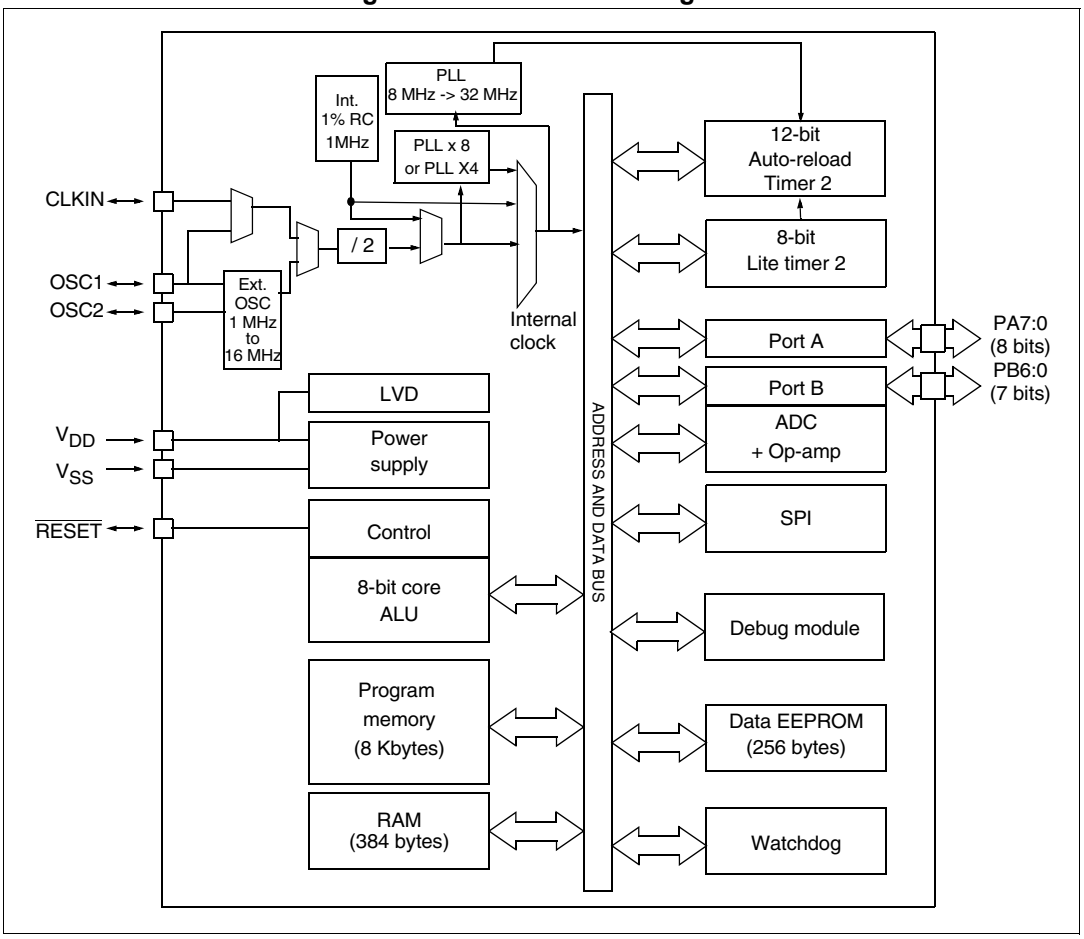
For easy reference, all parametric data are located in *Section 15: Device configuration*.

The devices feature an on-chip Debug Module (DM) to support in-circuit debugging (ICD). For a description of the DM registers, refer to the ST7 ICC Protocol Reference Manual.

Table 1. Device summary

Features	ST7LITE20F2	ST7LITE25F2	ST7LITE29F2
Program memory - bytes	8 Kbyte		
RAM (stack) - bytes	384 (128)		
Data EEPROM - bytes	–	–	256
Peripherals	Lite timer with Watchdog, autoreload timer, SPI, 10-bit ADC with Op-Amp	Lite timer with watchdog, autoreload timer with 32-MHz input clock, SPI, 10-bit ADC with op-amp	
Operating supply	2.4V to 5.5V		
CPU frequency	Up to 8 MHz (w/ ext OSC up to 16 MHz)	Up to 8 MHz (w/ ext OSC up to 16 MHz and int 1MHz RC 1% PLLx8/4 MHz)	
Operating temperature	–40 °C to +85 °C	–40 °C to +85 °C	–40 °C to +85 °C –40 °C to +105 °C
Packages	SO20 300”, DIP20		

Figure 1. General block diagram



2 Pin description

Figure 2. 20-pin SO package pinout

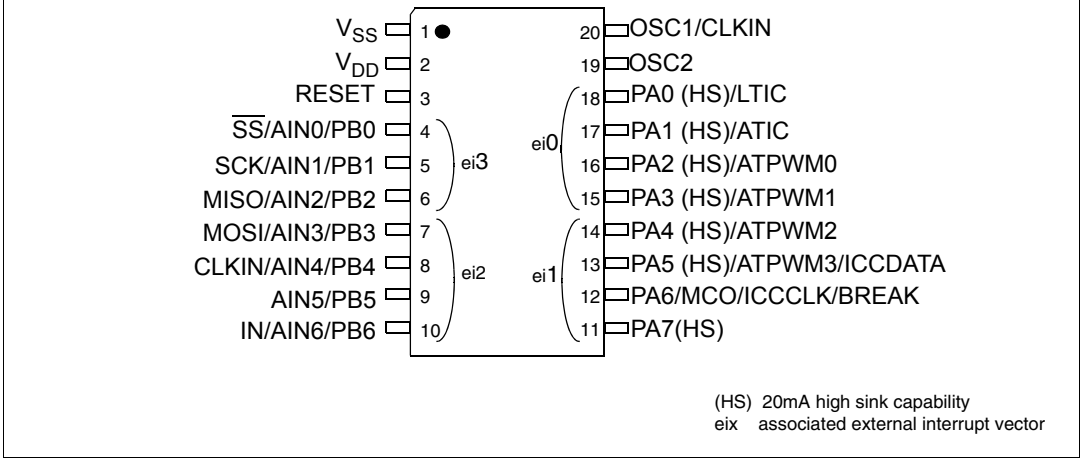
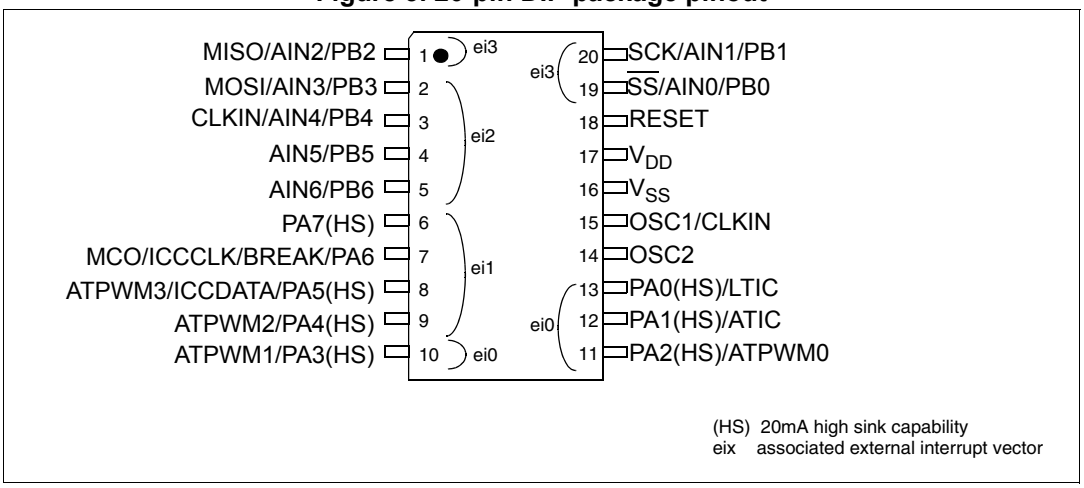


Figure 3. 20-pin DIP package pinout



Legend and abbreviations for device pin description (see *Table 2* below):

- Type:
  - I = input
  - O = output
  - S = supply
- In/Output level:
  - C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
- Output level:
  - HS = 20mA high sink (on N-buffer only)

Port and control configuration:

- Input:
  - float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output:
  - OD = open drain
  - PP = push-pull

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 2. Device pin description

Pin No.		Pin name	Type	Level		Port / Control						Main function (after reset)	Alternate function
						Input				Output			
SO20	DIP20			Input	Output	float	wpu	int	ana	OD	PP		
1	16	V_{SS}	S	-	-	-	-	-	-	-	-	Ground	
2	17	V_{DD}	S	-	-	-	-	-	-	-	-	Main power supply	
3	18	$\overline{RESET}$	I/O	C_T	-	-	X	-	-	X	-	Top priority non maskable interrupt (active low)	
4	19	PB0/AIN0/$\overline{SS}$	I/O	C_T		**X**	ei3		X	X	X	**Port B0**	ADC analog input 0 or SPI Slave Select (active low)(1)
5	20	PB1/AIN1/SCK	I/O	C_T		**X**			X	X	X	**Port B1**	ADC analog input 1 or SPI Serial Clock(1)
6	1	PB2/AIN2/MISO	I/O	C_T		**X**			X	X	X	**Port B2**	ADC analog input 2 or SPI Master in/ Slave out data
7	2	PB3/AIN3/MOSI	I/O	C_T		**X**	ei2		X	X	X	**Port B3**	ADC analog input 3 or SPI Master out / Slave in data
8	3	PB4/AIN4/CLKIN	I/O	C_T		**X**			X	X	X	**Port B4**	ADC analog input 4 or external clock input
9	4	PB5/AIN5	I/O	C_T		**X**			X	X	X	**Port B5**	ADC analog input 5
10	5	PB6/AIN6	I/O	C_T		**X**			X	X	X	**Port B6**	ADC analog input 6
11	6	PA7	I/O	C_T	HS	**X**	ei1		-	X	X	**Port A7**	-
12	7	PA6 /MCO/ ICCCLK/BREAK	I/O	C_T		X	ei1		-	X	X	**Port A6**	Main clock output or in circuit communication clock or external BREAK(2)
13	8	PA5 /ATPWM3/ ICCDATA	I/O	C_T	HS	**X**	ei1		-	X	X	**Port A5**	Auto-reload timer PWM3 or In circuit communication data
14	9	PA4/ATPWM2	I/O	C_T	HS	**X**			-	X	X	**Port A4**	Auto-reload timer PWM2

Table 2. Device pin description (continued)

Pin No.		Pin name	Type	Level		Port / Control						Main function (after reset)	Alternate function
						Input				Output			
SO20	DIP20			Input	Output	float	wpu	int	ana	OD	PP		
15	10	PA3/ATPWM1	I/O	C_T	HS	**X**	ei0		-	X	X	**Port A3**	Auto-reload timer PWM1
16	11	PA2/ATPWM0	I/O	C_T	HS	**X**			-	X	X	**Port A2**	Auto-reload timer PWM0
17	12	PA1/ATIC	I/O	C_T	HS	**X**			-	X	X	**Port A1**	Auto-reload timer input capture
18	13	PA0/LTIC	I/O	C_T	HS	**X**			-	X	X	**Port A0**	Lite timer input capture
19	14	OSC2	O	–	–	-	-	-	-	-	-	Resonator oscillator inverter output	
20	15	OSC1/CLKIN	I	–	–	-	-	-	-	-	-	Resonator oscillator inverter input or external clock input	

1. No negative current injection allowed on this pin. For details (refer to *Table 58: Current characteristics*).
2. During normal operation this pin must be pulled- up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

3 Register & memory map

As shown in *Figure 4*, the MCU is able of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, 384 bytes of RAM, 256 bytes of data EEPROM and 8 Kbytes of user program memory. The RAM space includes up to 128 bytes for the stack from 180h to 1FFh.

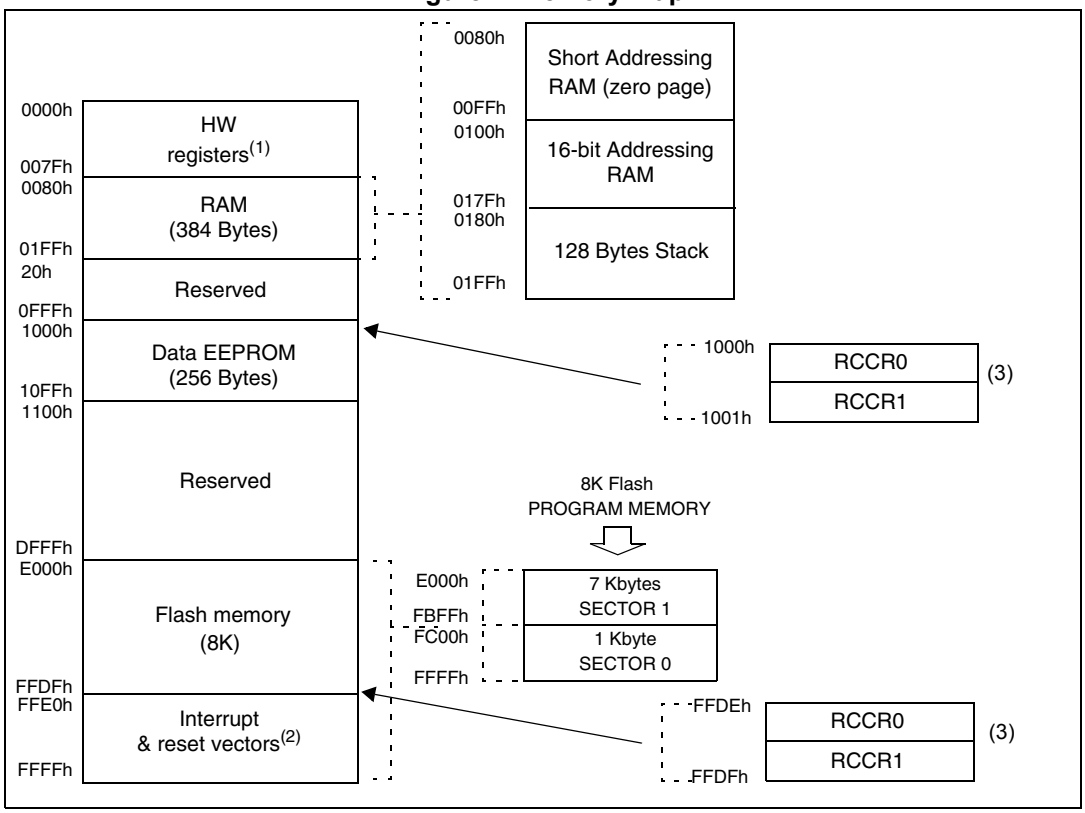
The highest address bytes contain the user reset and interrupt vectors.

The Flash memory contains two sectors (see *Figure 4*) mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

The size of Flash Sector 0 and other device options are configurable by Option byte (refer to *Section 15: Device configuration*).

Note: Memory locations marked as "Reserved" must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 4. Memory map



1. See *Table 3: Hardware register map*
2. See *Table 12: Interrupt mapping*
3. See *Section 7.1: Internal RC oscillator adjustment*

Table 3. Hardware register map(1)

Address	Block	Register label	Register name	Reset status	Remarks
0000h	Port A	PADR	Port A Data Register	FFh(2)	R/W
0001h		PADDR	Port A Data Direction Register	00h	R/W
0002h		PAOR	Port A Option Register	40h	R/W
0003h	Port B	PBDR	Port B Data Register	FFh(2)	R/W
0004h		PBDDR	Port B Data Direction Register	00h	R/W
0005h		PBOR	Port B Option Register	00h	R/W(3)
0006h 0007h	Reserved area (2 bytes)				
0008h	Lite TIMER 2	LTCSR2	Lite Timer Control/Status Register 2	00h	R/W
0009h		LTARR	Lite Timer Auto-reload Register	00h	R/W
000Ah		LTCNTR	Lite Timer Counter Register	00h	Read only
000Bh		LTCSR1	Lite Timer Control/Status Register 1	0X00 0000h	R/W
000Ch		LTICR	Lite Timer Input Capture Register	00h	Read only
000Dh	Auto-reload TIMER 2	ATCSR	Timer Control/Status Register	0X00 0000h	R/W
000Eh		CNTRH	Counter Register High	00h	Read only
000Fh		CNTRL	Counter Register Low	00h	Read only
0010h		ATRH	Auto-Reload Register High	00h	R/W
0011h		ATRL	Auto-Reload Register Low	00h	R/W
0012h		PWMCR	PWM Output Control Register	00h	R/W
0013h		PWM0CSR	PWM 0 Control/Status Register	00h	R/W
0014h		PWM1CSR	PWM 1 Control/Status Register	00h	R/W
0015h		PWM2CSR	PWM 2 Control/Status Register	00h	R/W
0016h		PWM3CSR	PWM 3 Control/Status Register	00h	R/W
0017h		DCR0H	PWM 0 Duty Cycle Register High	00h	R/W
0018h		DCR0L	PWM 0 Duty Cycle Register Low	00h	R/W
0019h		DCR1H	PWM 1 Duty Cycle Register High	00h	R/W
001Ah		DCR1L	PWM 1 Duty Cycle Register Low	00h	R/W
001Bh		DCR2H	PWM 2 Duty Cycle Register High	00h	R/W
001Ch		DCR2L	PWM 2 Duty Cycle Register Low	00h	R/W
001Dh		DCR3H	PWM 3 Duty Cycle Register High	00h	R/W
001Eh		DCR3L	PWM 3 Duty Cycle Register Low	00h	R/W
001Fh		ATICRH	Input Capture Register High	00h	Read only
0020h		ATICRL	Input Capture Register Low	00h	Read only
0021h		TRANCR	Transfer Control Register	01h	R/W
0022h		BREAKCR	Break Control Register	00h	R/W
0023h to 002Dh	Reserved area (11 bytes)				
002Eh	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
0002Fh	Flash	FCSR	Flash Control/Status Register	00h	R/W
00030h	EEPROM	EECSR	Data EEPROM Control/Status Register	00h	R/W
0031h	SPI	SPIDR	SPI Data I/O Register	xxh	R/W
0032h		SPICR	SPI Control Register	0xh	R/W
0033h		SPICSR	SPI Control Status Register	00h	R/W
0034h	ADC	ADCCSR	A/D Control Status Register	00h	R/W
0035h		ADCDRH	A/D Data Register High	xxh	Read Only
0036h		ADCDRL	A/D Amplifier Control/Data Low Register	0xh	R/W

Table 3. Hardware register map(1) (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0037h	ITC	EICR	External Interrupt Control Register	00h	R/W
0038h	MCC	MCCSR	Main Clock Control/Status Register	00h	R/W
0039h 003Ah	Clock and Reset	RCCR SICSR	RC oscillator Control Register System Integrity Control/Status Register	FFh 0000 0XX0h	R/W R/W
003Bh	Reserved area (1 byte)				
003Ch	ITC	EISR	External Interrupt Selection Register	0Ch	R/W
003Dh to 0048h	Reserved area (12 bytes)				
0049h 004Ah	AWU	AWUPR AWUCSR	AWU Prescaler Register AWU Control/Status Register	FFh 00h	R/W R/W
004Bh 004Ch 004Dh 004Eh 004Fh 0050h	DM(4)	DMCR DMSR DMBK1H DMBK1L DMBK2H DMBK2L	DM Control Register DM Status Register DM Breakpoint Register 1 High DM Breakpoint Register 1 Low DM Breakpoint Register 2 High DM Breakpoint Register 2 Low	00h 00h 00h 00h 00h 00h	R/W R/W R/W R/W R/W R/W
0051h to 007Fh	Reserved area (47 bytes)				

1. Legend: x = undefined, R/W = read/write.
2. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
3. The bits associated with unavailable pins must always keep their reset value.
4. For a description of the Debug Module registers, see ICC reference manual.

4 Flash program memory

4.1 Introduction

The ST7 single voltage extended Flash (XFlash) is a non-volatile memory that can be electrically erased and programmed either on a byte-by-byte basis or up to 32 bytes in parallel.

The XFlash devices can be programmed off-board (plugged in a programming tool) or on-board using in-circuit programming or in-application programming.

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- ICP (in-circuit programming)
- IAP (in-application programming)
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Sector 0 size configurable by option byte
- Read-out and write protection

4.3 Programming modes

The ST7 can be programmed in three different ways:

- Insertion in a programming tool. In this mode, Flash sectors 0 and 1, option byte row and data EEPROM (if present) can be programmed or erased.
- In-circuit programming. In this mode, Flash sectors 0 and 1, option byte row and data EEPROM (if present) can be programmed or erased without removing the device from the application board.
- In-application programming. In this mode, sector 1 and data EEPROM (if present) can be programmed or erased without removing the device from the application board and while the application is running.

4.3.1 In-circuit programming (ICP)

ICP uses a protocol called ICC (in-circuit communication) which allows an ST7 plugged on a printed circuit board (PCB) to communicate with an external programming device connected via cable. ICP is performed in three steps:

1. Switch the ST7 to ICC mode (in-circuit communications). This is done by driving a specific signal sequence on the ICCCLK/DATA pins while the RESET pin is pulled low. When the ST7 enters ICC mode, it fetches a specific RESET vector which points to the ST7 System Memory containing the ICC protocol routine. This routine enables the ST7 to receive bytes from the ICC interface.
2. Download ICP driver code in RAM from the ICCDATA pin.
3. Execute ICP driver code in RAM to program the Flash memory.

Depending on the ICP driver code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection of the serial communication interface for downloading).

4.3.2 In-application programming (IAP)

This mode uses an IAP driver program previously programmed in Sector 0 by the user (in ICP mode).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored etc.).
IAP mode can be used to program any memory areas except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.4 ICC interface

ICP needs a minimum of 4 and up to 6 pins to be connected to the programming tool. These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input serial data pin
- CLKIN/PB4: main clock input for external source
- V_{DD}: application board power supply (optional).

If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

During the ICP session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1K). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R>1 kΩ or a reset management IC with open drain output and pull-up resistor > 1 kΩ, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

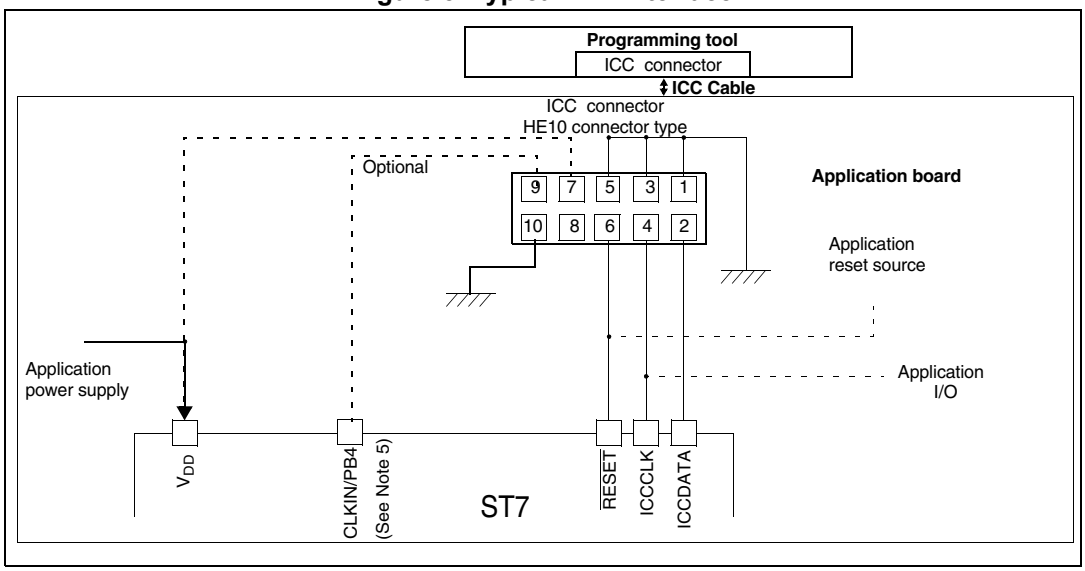
The use of Pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

Pin 9 has to be connected to the CLKIN/PB4 pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC1 and OSC2 grounded in this case.

With any programming tool, while the ICP option is disabled, the external clock has to be provided on PB4.

Caution: During normal operation the ICCCLK pin must be pulled up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

Figure 5. Typical ICC interface



4.5 Memory protection

There are two different types of memory protection: Read-Out Protection and Write/Erase Protection which can be applied individually.

4.5.1 Read-out protection

Read-out protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller. Both program and data E^2 memory are protected.

In flash devices, this protection is removed by reprogramming the option. In this case, both program and data E^2 memory are automatically erased and the device can be reprogrammed.

Read-out protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the Option List.

4.5.2 Flash write/erase protection

Write/erase protection, when set, makes it impossible to both overwrite and erase program memory. It does not apply to E^2 data. Its purpose is to provide advanced security to applications and prevent any change being made to the memory content.

Caution: Once set, Write/erase protection can never be removed. A write-protected flash device is no longer reprogrammable.

Write/erase protection is enabled through the FMP_W bit in the option byte.

4.6 Related documentation

For details on Flash programming and ICC protocol, refer to the ST7 Flash Programming Reference Manual and to the ST7 ICC Protocol Reference Manual.

4.7 Register description

Flash control/status register (FCSR)

Read / Write

Reset value: 0000 0000 (00h)

1st RASS Key: 0101 0110 (56h)

2nd RASS Key: 1010 1110 (AEh)

7							0
0	0	0	0	0	OPT	LAT	PGM

Note: This register is reserved for programming using ICP, IAP or other programming methods. It controls the XFlash programming and erasing operations.

When an EPB or another programming tool is used (in socket or ICP mode), the RASS keys are sent automatically.

5 Data EEPROM

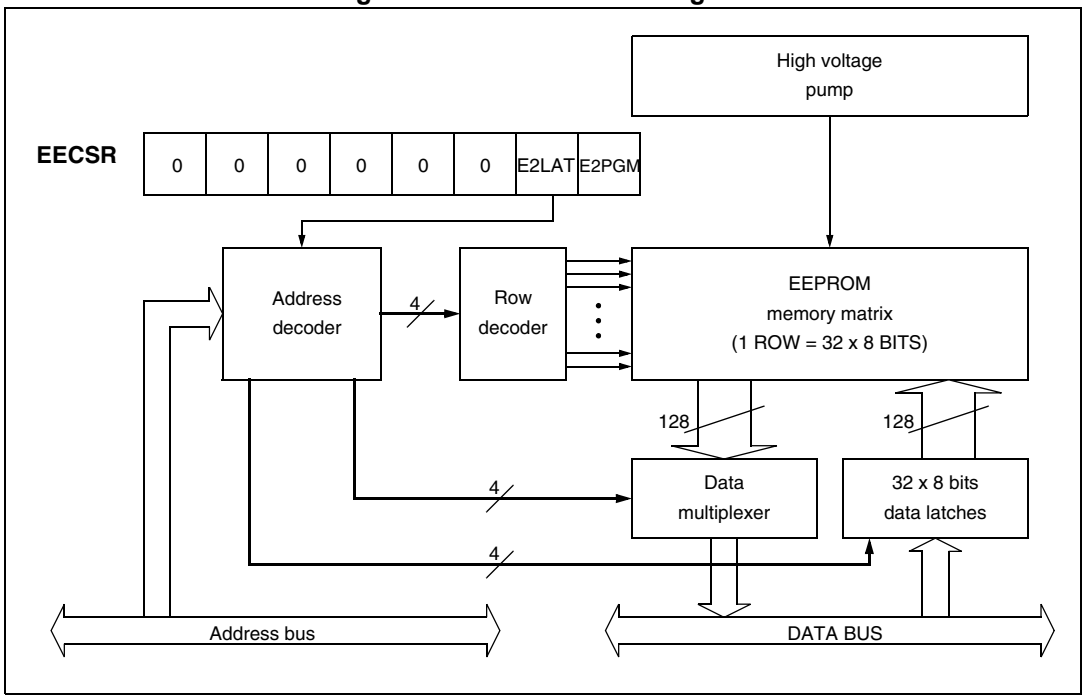
5.1 Introduction

The Electrically Erasable Programmable Read Only Memory can be used as a non-volatile backup for storing data. Using the EEPROM requires a basic access protocol described in this chapter.

5.2 Main features

- Up to 32 bytes programmed in the same cycle
- EEPROM mono-voltage (charge pump)
- Chained erase and programming cycles
- Internal control of the global programming cycle duration
- WAIT mode management
- Read-out protection

Figure 6. EEPROM block diagram



5.3 Memory access

The Data EEPROM memory read/write access modes are controlled by the E2LAT bit of the EEPROM Control/Status register (EECSR). The flowchart in *Figure 7* describes these different memory access modes.