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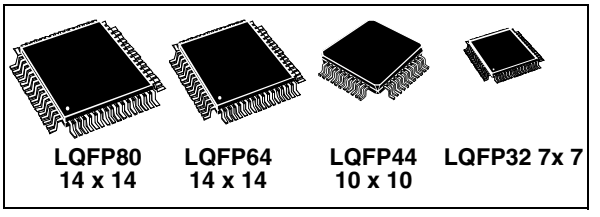
ST7MC1xx/ST7MC2xx

8-bit MCU with nested interrupts, Flash, 10-bit ADC, brushless motor control, five timers, SPI, LINSCI™

Features

- **Memories**
  - 8K to 60K dual voltage Flash Program memory or ROM with read-out protection capability, In-application programming and In-circuit programming.
  - 384 to 1.5K RAM
  - HDFlash endurance: 100 cycles, data retention: 40 years at 85°C
- **Clock, reset and supply management**
  - Enhanced reset system
  - Enhanced low voltage supervisor (LVD) for main supply and auxiliary voltage detector (AVD) with interrupt capability
  - Clock sources: crystal/ceramic resonator oscillators and by-pass for external clock, clock security system.
  - Four power saving modes: Halt, Active-halt, Wait and Slow
- **Interrupt management**
  - Nested interrupt controller
  - 14 interrupt vectors plus TRAP and RESET
  - MCES top level interrupt pin
  - 16 external interrupt lines (on 3 vectors)
- **Up to 60 I/O ports**
  - up to 60 multifunctional bidirectional I/O lines
  - up to 41 alternate function lines
  - up to 12 high sink outputs
- **5 timers**
  - Main clock controller with: Real-time base, Beep and clock-out capabilities
  - Configurable window watchdog timer
  - Two 16-bit timers with: 2 input captures, 2 output compares, external clock input, PWM and pulse generator modes
  - 8-bit PWM Auto-reload timer with: 2 input captures, 4 PWM outputs, output compare and time base interrupt, external clock with event detector



- **2 Communication interfaces**
  - SPI synchronous serial interface
  - LINSCI™ asynchronous serial interface
- **Brushless motor control peripheral**
  - 6 high sink PWM output channels for sine-wave or trapezoidal inverter control
  - Motor safety including asynchronous emergency stop and write-once registers
  - 4 analog inputs for rotor position detection (sensorless/hall/tacho/encoder)
  - Permanent magnet motor coprocessor including multiplier, programmable filters, blanking windows and event counters
  - Operational amplifier and comparator for current/voltage mode regulation and limitation
- **Analog peripheral**
  - 10-bit ADC with 16 input pins
- **In-circuit Debug**
- **Instruction set**
  - 8-bit data manipulation
  - 63 basic instructions with illegal opcode detection
  - 17 main Addressing modes
  - 8 x 8 unsigned multiply instruction
  - True bit manipulation
- **Development tools**
  - Full hardware/software development package

Table 1. Device summary

Features	ST7MC1K2 / ST7MC1K4		ST7MC2N6 [1] / ST7MC2S4 / ST7MC2S6 / ST7MC2S7 / ST7MC2S9 / ST7MC2R6 / ST7MC2R7 / ST7MC2R9 / ST7MC2M9			
Program memory - bytes	8K	16K	16K	32K	48K	60K
RAM (stack) - bytes	384 (256)	768 (256)	768 (256)	1024 (256)	1536 (256)	
Peripherals	Watchdog, 16-bit Timer A, LINSCI™, 10-bit ADC, MTC, 8-bit PWM ART, ICD					
	-		SPI, 16-bit Timer B			
Operating Supply vs. Frequency	4.5 to 5.5V with $f_{CPU} \leq 8MHz$					
Temperature Range	-40°C to +85°C /-40°C to +125°C	-40°C to +85°C	-40°C to +85°C -40°C to +125°C	-40°C to +85 °C		-40°C to +125°C
Package	LQFP32	LQFP32	LQFP44	SDIP56[1]/LQFP64	LQFP64/44	LQFP80/64	LQFP44

Note 1: For development only. No production

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please check at www.st.com>products>technical literature>datasheet

Please also pay special attention to the Section “IMPORTANT NOTES” on page 299.

1 INTRODUCTION

The ST7MCx device is member of the ST7 microcontroller family designed for mid-range applications with a Motor Control dedicated peripheral.

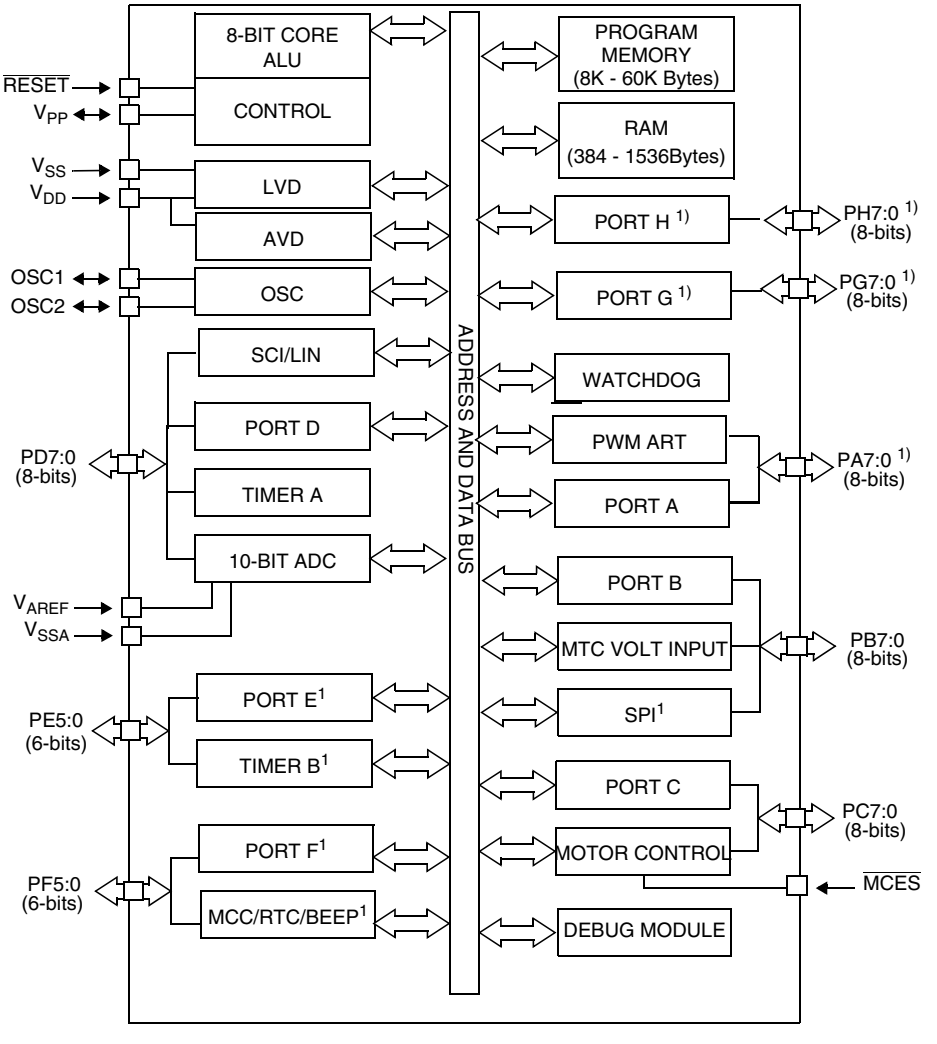
All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with FLASH, ROM or FASTROM program memory.

Under software control, all devices can be placed in Wait, Slow, Active-halt or Halt mode, reducing power consumption when the application is in idle or stand-by state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

The devices feature an on-chip Debug Module (DM) to support in-circuit debugging (ICD). For a description of the DM registers, refer to the ST7 ICC Protocol Reference Manual.

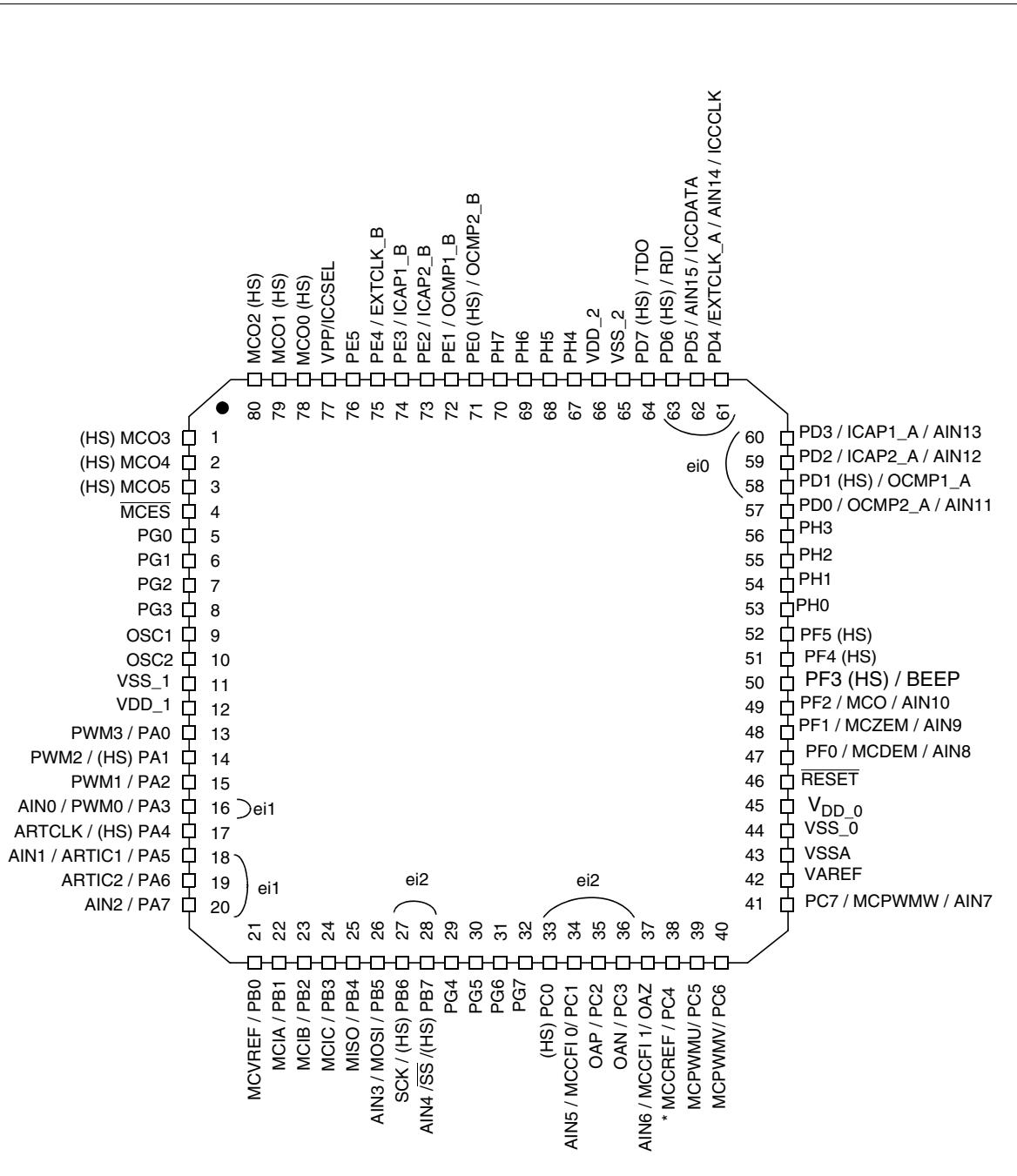
Figure 1. Device Block Diagram



On some devices only, see Table 1, “ST7MC Device Pin Description,” on page 12

2 PIN DESCRIPTION

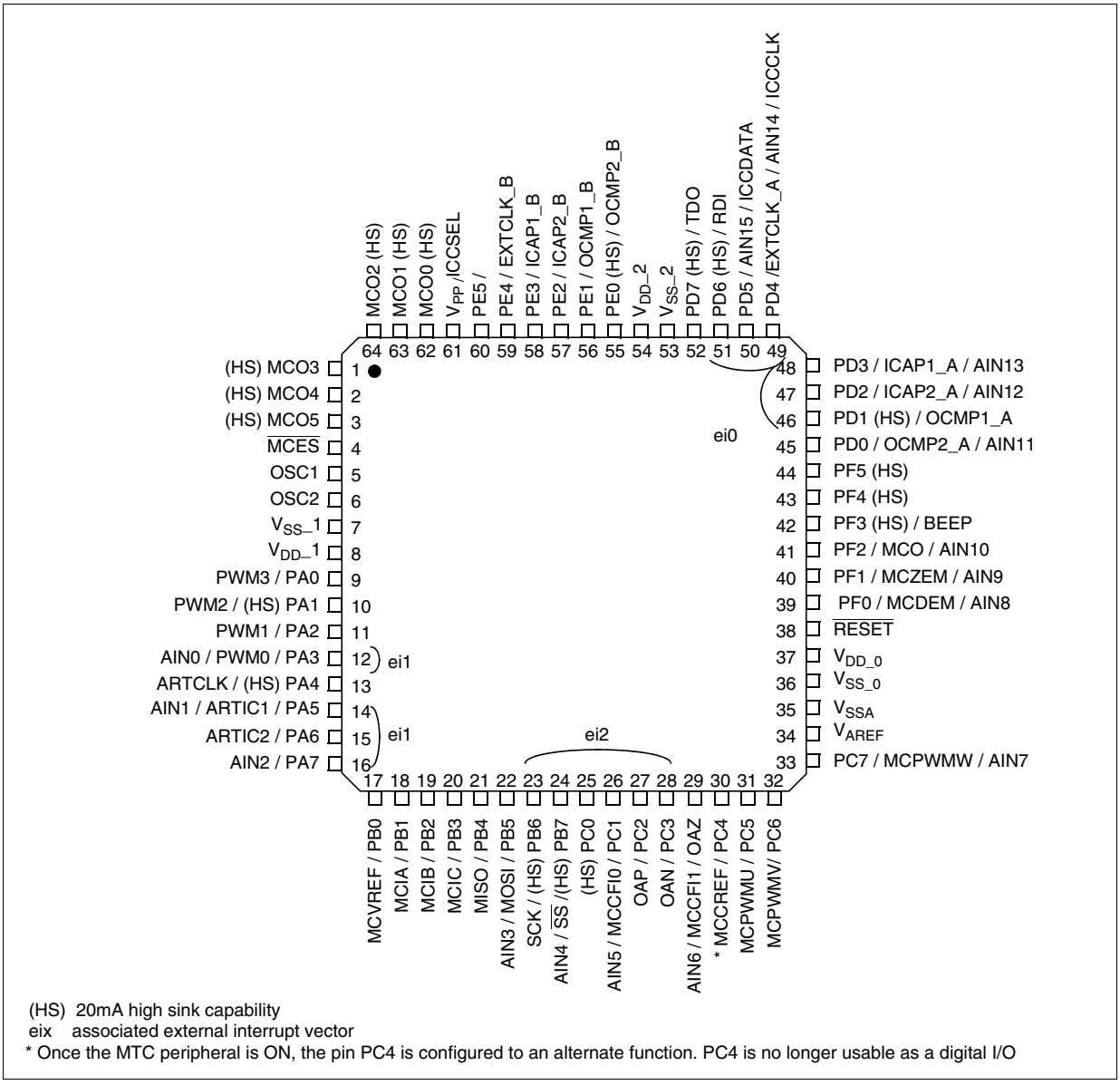
Figure 2. 80-Pin LQFP 14x14 Package Pinout



(HS) 20mA high sink capability
eix associated external interrupt vector
* Once the MTC peripheral is ON, the pin PC4 is configured to an alternate function. PC4 is no longer usable as a digital I/O

PIN DESCRIPTION (Cont'd)

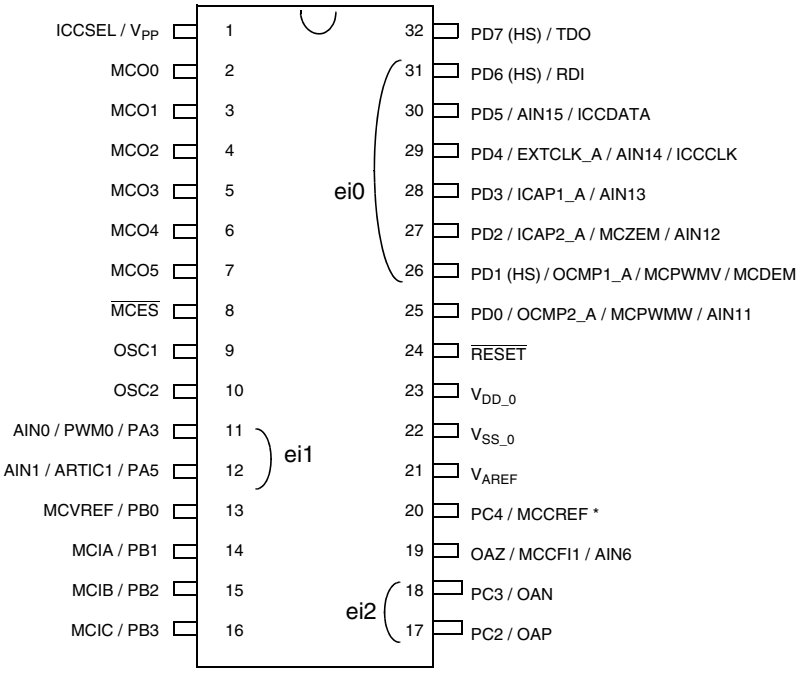
Figure 3. 64-Pin LQFP 14x14 Package Pinout



(HS) 20mA high sink capability
eix associated external interrupt vector
* Once the MTC peripheral is ON, the pin PC4 is configured to an alternate function. PC4 is no longer usable as a digital I/O

PIN DESCRIPTION (Cont'd)

Figure 4. 32-Pin SDIP Package Pinouts



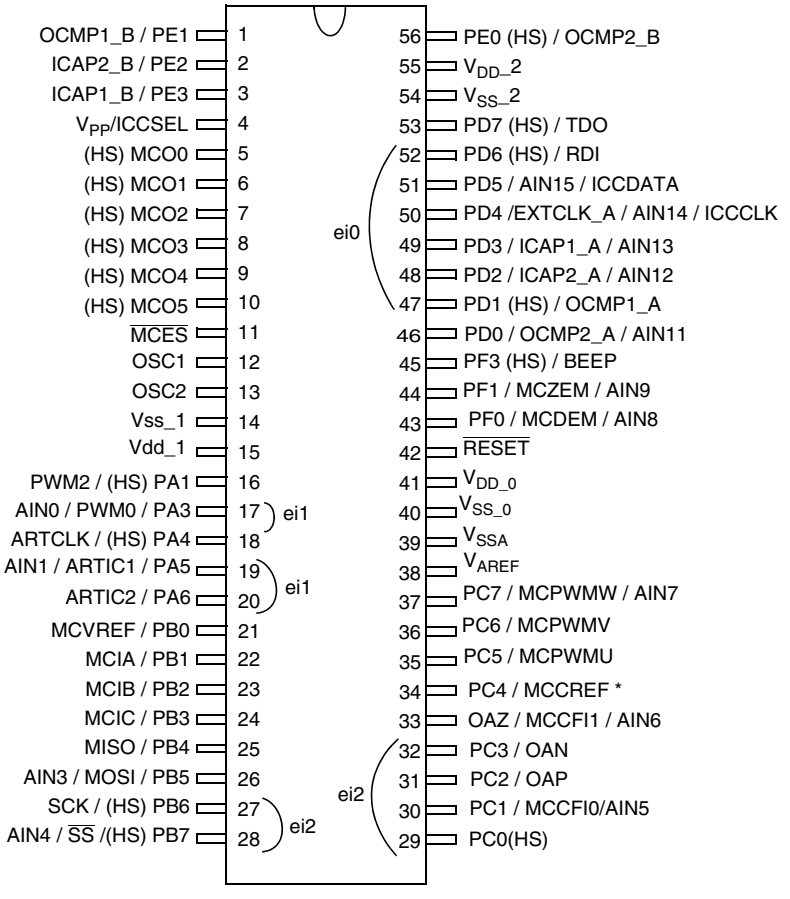
(HS) 20mA high sink capability

eix associated external interrupt vector

* Once the MTC peripheral is ON, the pin PC4 is configured to an alternate function. PC4 is no longer usable as a digital I/O

PIN DESCRIPTION (Cont'd)

Figure 5. 56-Pin SDIP Package Pinouts

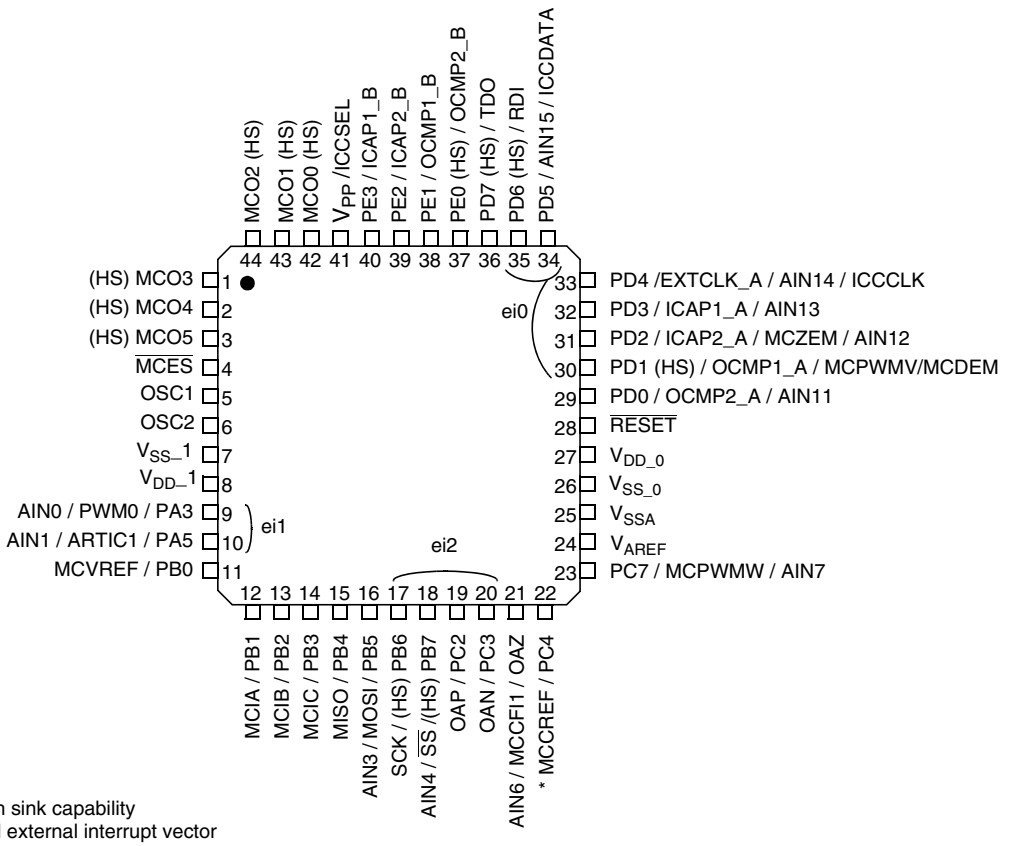


(HS) 20mA high sink capability
eix associated external interrupt vector

* Once the MTC peripheral is ON, the pin PC4 is configured to an alternate function. PC4 is no longer usable as a digital I/O

PIN DESCRIPTION (Cont'd)

Figure 6. 44-Pin LQFP Package Pinouts

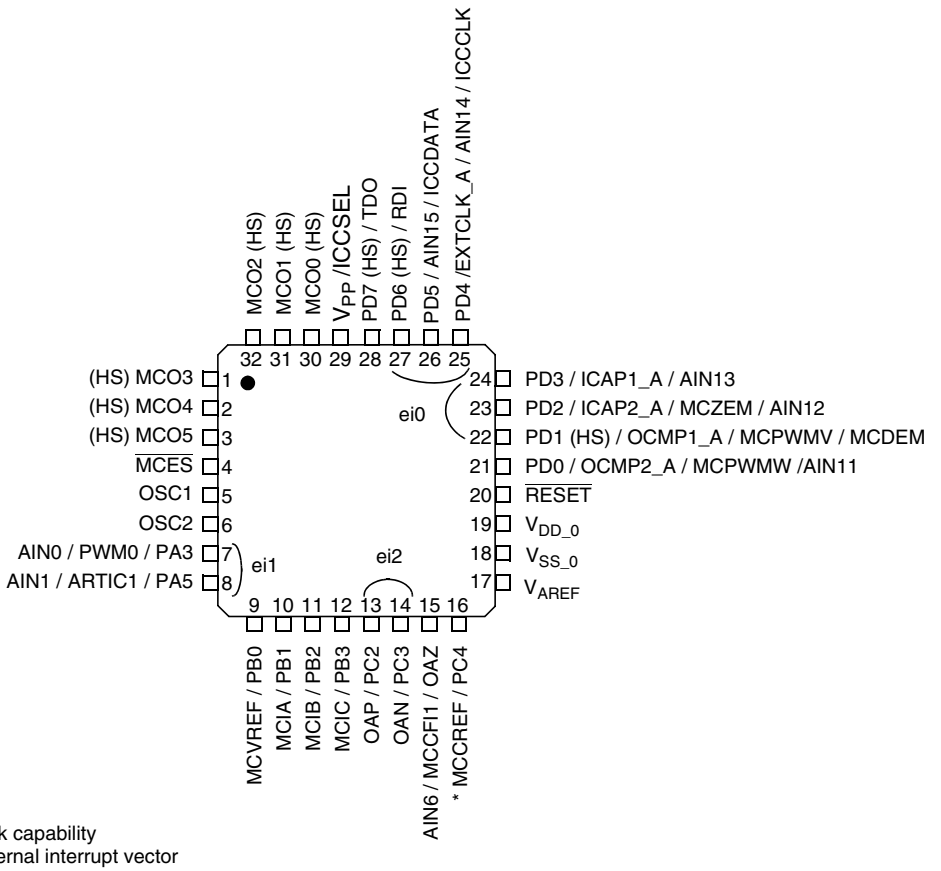


(HS) 20mA high sink capability
eix associated external interrupt vector

* Once the MTC peripheral is ON, the pin PC4 is configured to an alternate function. PC4 is no longer usable as a digital I/O

PIN DESCRIPTION (Cont'd)

Figure 7. 32-Pin LQFP 7x7 Package Pinout



(HS) 20mA high sink capability
eix associated external interrupt vector

* Once the MTC peripheral is ON, the pin PC4 is configured to an alternate function. PC4 is no longer usable as a digital I/O

PIN DESCRIPTION (Cont'd)

For external pin connection guidelines, See "ELECTRICAL CHARACTERISTICS" on page 247.

Legend / Abbreviations for Table 1:

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with Schmitt trigger

T_T= Refer to the G&H ports Characteristics in section 12.8.1 on page 264

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, wpd = weak pull-down, int = interrupt [1], ana = analog

– Output: OD = open drain, PP = push-pull

Refer to "I/O PORTS" on page 54 for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 1. ST7MC Device Pin Description

Pin n°						Pin Name	Type	Level		Port						Main function (after reset)	Alternate function [2]	
										Input [1]				Output				
LQFP80	LQFP64	SDIP56	LQFP44	SDIP32	LQFP32			Input	Output	float	wpu	int	ana	OD	PP			
1	1	8	1	5	1	MCO3 (HS)	O		HS						X	Motor Control Output 3		
2	2	9	2	6	2	MCO4 (HS)	O		HS						X	Motor Control Output 4		
3	3	10	3	7	3	MCO5 (HS)	O		HS						X	Motor Control Output 5		
4	4	11	4	8	4	$\overline{MCES}$ [3]	I	C_T		**X**						MTC Emergency Stop		
5	-	-	-	-	-	PG0	I/O	T_T		**X**	X			X	X	Port G0		
6	-	-	-	-	-	PG1	I/O	T_T		**X**	X			X	X	Port G1		
7	-	-	-	-	-	PG2	I/O	T_T		**X**	X			X	X	Port G2		
8	-	-	-	-	-	PG3	I/O	T_T		**X**	X			X	X	Port G3		
9	5	12	5	9	5	OSC1 [4]	I									External clock input or Resonator oscillator inverter input		
10	6	13	6	10	6	OSC2 [4]	I/O									Resonator oscillator inverter output		
11	7	14	7	-	-	V_{ss_1} [5]	S									Digital Ground Voltage		
12	8	15	8	-	-	V_{dd_1} [5]	S									Digital Main Supply Voltage		
13	9	-	-	-	-	PA0/PWM3	I/O	C_T		**X**	X			X	X	Port A0	PWM Output 3	
14	10	16	-	-	-	PA1/PWM2	I/O	C_T	HS	**X**	X			X	X	Port A1	PWM Output 2	
15	11	-	-	-	-	PA2PWM1	I/O	C_T		**X**	X			X	X	Port A2	PWM Output 1	
16	12	17	9	11	7	PA3/PWM0/ AIN0	I/O	C_T		**X**	ei1		X	X	X	Port A3	PWM Output 0	ADC Analog Input 0
17	13	18	-	-	-	PA4 (HS)/ARTCLK	I/O	C_T	HS	**X**	X			X	X	Port A4	PWM-ART External Clock	
18	14	19	10	12	8	PA5 / ARTIC1/ AIN1	I/O	C_T		**X**		ei1	X	X	X	Port A5	PWM-ART Input Capture 1	ADC Analog Input 1
19	15	20	-	-	-	PA6 / ARTIC2	I/O	C_T		**X**	ei1			X	X	Port A6	PWM-ART Input Capture 2	
20	16	-	-	-	-	PA7/AIN2	I/O	C_T		**X**		ei1	X	X	X	Port A7	ADC Analog Input 2	

Table 1. ST7MC Device Pin Description

Pin n°						Pin Name	Type	Level		Port						Main function (after reset)	Alternate function [2]	
										Input [1]				Output				
LQFP80	LQFP64	SDIP56	LQFP44	SDIP32	LQFP32			Input	Output	float	wpu	int	ana	OD	PP			
21	17	21	11	13	9	PB0/MCVREF	I/O	C_T		**X**	X		X	X	X	Port B0	MTC Voltage Reference	
22	18	22	12	14	10	PB1/MCIA	I/O	C_T		**X**	X		X	X	X	Port B1	MTC Input A	
23	19	23	13	15	11	PB2/MCIB	I/O	C_T		**X**	X		X	X	X	Port B2	MTC Input B	
24	20	24	14	16	12	PB3/MCIC	I/O	C_T		**X**	X		X	X	X	Port B3	MTC Input C	
25	21	25	15	-	-	PB4/MISO	I/O	C_T		**X**	X			X	X	Port B4	SPI Master In / Slave Out Data	
26	22	26	16	-	-	PB5/MOSI/ AIN3	I/O	C_T		**X**	X			X	X	Port B5	SPI Master Out / Slave In Data	ADC Analog Input 3
27	23	27	17	-	-	PB6/SCK	I/O	C_T	HS	**X**	ei2			X	X	Port B6	SPI Serial Clock	
28	24	28	18	-	-	PB7/$\overline{SS}$/AIN4	I/O	C_T	HS	**X**		ei2		X	X	Port B7	SPI Slave Select (active low)	ADC Analog Input 4
29	-	-	-	-	-	PG4	I/O	T_T		**X**	X			X	X	Port G4		
30	-	-	-	-	-	PG5	I/O	T_T		**X**	X			X	X	Port G5		
31	-	-	-	-	-	PG6	I/O	T_T		**X**	X			X	X	Port G6		
32	-	-	-	-	-	PG7	I/O	T_T		**X**	X			X	X	Port G7		
33	25	29	-	-	-	PC0	I/O	C_T	HS	**X**		ei2		X	X	Port C0		
34	26	30	-	-	-	PC1/MCCFI0[6] /AIN5	I/O	C_T		**X**	ei2		X	X	X	Port C1	MTC Current Feedback Input 0[6]	ADC Analog Input 5
35	27	31	19	17	13	PC2/OAP	I/O	C_T		**X**		ei2	X	X	X	Port C2	OPAMP Positive Input	
36	28	32	20	18	14	PC3/OAN	I/O	C_T		**X**	X	ei2	X	X	X	Port C3	OPAMP Negative Input	
37	29	33	21	19	15	OAZ/ MCCFI1[6]/ AIN6	I/O						X			Opamp Output	MTC Current Feedback Input 1[6]	ADC analog Input 6
38	30	34	22	20	16	PC4/MCCREF	I/O	C_T		**X**	X		X	X	X	Port C4	MTC Current Feedback Reference [9]	
39	31	35	-	-	-	PC5/MCPWMU	I/O	C_T		**X**	X			X	X	Port C5	MTC PWM Output U	
40	32	36	-	-	-	PC6/ MCPWMV[8]	I/O	C_T		**X**	X			X	X	Port C6	MTC PWM Output V[8]	
41	33	37	23	-	-	PC7/ MCPWMW[8]/ AIN7	I/O	C_T		**X**	X		X	X	X	Port C7	MTC PWM Output W[8]	ADC Analog Input 7
42	34	38	24	21	17	V_{AREF}	I									Analog Reference Voltage for ADC		
43	35	39	25	-	-	V_{SSA}[5]	S									Analog Ground Voltage		
44	36	40	26	22	18	V_{SS_0}[5]	S									Digital Ground Voltage		
45	37	41	27	23	19	V_{DD_0}[5]	S									Digital Main Supply Voltage		
46	38	42	28	24	20	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt		

Table 1. ST7MC Device Pin Description

Pin n°						Pin Name	Type	Level		Port						Main function (after reset)	Alternate function [2]	
										Input [1]				Output				
LQFP80	LQFP64	SDIP56	LQFP44	SDIP32	LQFP32			Input	Output	float	wpu	int	ana	OD	PP			
47	39	43	-	-	-	PF0/ MCDEM[7]/ AIN8	I/O	C_T		**X**	X		X	X	X	Port F0	MTC Demagnetization Output[7]	ADC Analog Input 8
48	40	44	-	-	-	PF1/MCZEM[7]/ AIN9	I/O	C_T		**X**	X		X	X	X	Port F1	MTC BEMF Output[7]	ADC Analog Input 9
49	41	-	-	-	-	PF2/MCO/ AIN10	I/O	C_T		**X**	X		X	X	X	Port F2	Main Clock Out (f_{osc}/2)	ADC Analog Input 10
50	42	45	-	-	-	PF3/BEEP	I/O	C_T	HS	**X**	X			X	X	Port F3	Beep Signal Output	
51	43	-	-	-	-	PF4	I/O	C_T	HS	**X**	X			X	X	Port F4		
52	44	-	-	-	-	PF5	I/O	C_T	HS	**X**	X			X	X	Port F5		
53	-	-	-	-	-	PH0	I/O	T_T		**X**	X			X	X	Port H0		
54	-	-	-	-	-	PH1	I/O	T_T		**X**	X			X	X	Port H1		
55	-	-	-	-	-	PH2	I/O	T_T		**X**	X			X	X	Port H2		
56	-	-	-	-	-	PH3	I/O	T_T		**X**	X			X	X	Port H3		
57	45	46	29	25	21	PD0/ OCMP2_A/ MCPWMW[8]/ AIN11	I/O	C_T		**X**			X	X	X	Port D0	Timer A Output Compare 2 MTC PWM Output W[8] ADC Analog Input 11	
58	46	47	30	26	22	PD1 (HS)/ OCMP1_A/ MCPWMV[8]/ MCDEM[7]	I/O	C_T	HS	**X**		ei0		X	X	Port D1	Timer A Output Compare 1 MTC PWM Output V[8] MTC Demagnetization[7]	
59	47	48	31	27	23	PD2/ICAP2_A/ MCZEM[7] / AIN12	I/O	C_T		**X**	ei0		X	X	X	Port D2	Timer A Input Capture 2 MTC BEMF[7] ADC Analog Input 12	
60	48	49	32	28	24	PD3/ICAP1_A/ AIN13	I/O	C_T		**X**		ei0	X	X	X	Port D3	Timer A Input Capture 1	ADC Analog Input 13
61	49	50	33	29	25	PD4/ EXTCLK_A/ICCCLK/AIN14	I/O	C_T		**X**	ei0		X	X	X	Port D4	Timer A External Clock source ICC Clock Output ADC Analog Input 14	
62	50	51	34	30	26	PD5/ICCDATA/AIN15	I/O	C_T		**X**	ei0		X	X	X	Port D5	ICC Data Input ADC Analog Input 15	
63	51	52	35	31	27	PD6/RDI	I/O	C_T	HS	**X**		ei0		X	X	Port D6	SCI Receive Data In	
64	52	53	36	32	28	PD7/TDO	I/O	C_T	HS	**X**	X			X	X	Port D7	SCI Transmit Data Output	
65	53	54	-	-	-	V_{SS_2}	S									Digital Ground Voltage		
66	54	55	-	-	-	V_{DD_2}	S									Digital Main Supply Voltage		
67	-	-	-	-	-	PH4	I/O	T_T		**X**	X			X	X	Port H4		
68	-	-	-	-	-	PH5	I/O	T_T		**X**	X			X	X	Port H5		

Table 1. ST7MC Device Pin Description

Pin n°						Pin Name	Type	Level		Port						Main function (after reset)	Alternate function [2]
										Input [1]				Output			
LQFP80	LQFP64	SDIP56	LQFP44	SDIP32	LQFP32			Input	Output	float	wpu	int	ana	OD	PP		
69	-	-	-	-	-	PH6	I/O	T_T		**X**	X			X	X	Port H6	
70	-	-	-	-	-	PH7	I/O	T_T		**X**	X			X	X	Port H7	
71	55	56	37	-	-	PE0/ OCMP2_B	I/O	C_T	HS	**X**	X			X	X	Port E0	Timer B Output Compare 2
72	56	1	38	-	-	PE1/ OCMP1_B	I/O	C_T		**X**	X		X	X	X	Port E1	Timer B Output Compare 1
73	57	2	39	-	-	PE2/ICAP2_B	I/O	C_T		**X**	X			X	X	Port E2	Timer B Input Capture 2
74	58	3	40	-	-	PE3/ICAP1_B/	I/O	C_T		**X**	X		X	X	X	Port E3	Timer B Input Capture 1
75	59	-	-	-	-	PE4/ EXTCLK_B	I/O	C_T		**X**	X			X	X	Port E4	Timer B External Clock source
76	60	-	-	-	-	PE5	I/O	C_T		**X**	X		X	X	X	Port E5	
77	61	4	41	1	29	V_{PP}/ICCSEL	I									Must be tied low. In the programming mode when available, this pin acts as the programming voltage input V_{PP}./ ICC mode pin. See section 12.9.2 on page 269	
78	62	5	42	2	30	MCO0 (HS)	O		HS						X	MTC Output Channel 0	
79	63	6	43	3	31	MCO1 (HS)	O		HS						X	MTC Output Channel 1	
80	64	7	44	4	32	MCO2 (HS)	O		HS						X	MTC Output Channel 2	

Notes:
1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input

2. If two alternate function outputs are enabled at the same time on a given pin (for instance, MCPWMV and MCDEM on PD1 on LQFP32), the two signals will be ORed on the output pin.

3. $\overline{\text{MCES}}$ is a floating input. To disable this function, a pull-up resistor must be used.

4. OSC1 and OSC2 pins connect a crystal/ceramic resonator or an external source to the on-chip oscillator; see Section 1 INTRODUCTION and Section 12.5 CLOCK AND TIMING CHARACTERISTICS for more details.

5. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.

6. MCCFI can be mapped on 2 different pins on 80 ,64 and 56-pin packages. This allows:

- either to use PC1 as a standard I/O and map MCCFI on OAZ (MCCFI1) with or without using the operational amplifier (selected case after reset),

- or to map MCCFI on PC1 (MCCFI0) and use the amplifier for another function.

The mapping can be selected in MREF register of motor control cell. See section MOTOR CONTROL for more details.

7. MCZEM is mapped on PF1 on 80, 64 and 56-pin packages and on PD2 on 44 and 32-pins.
MCDEM is mapped on PF0 on 80, 64 and 56-pin packages and on PD1 on 44 and 32-pin packages.

8. MCPWMV is mapped on PC6 on 80 and 64-pin packages and on PD1 on 44,and 32-pins packages.
MCPWMW is mapped on PC7 on 80, 64 and 44-pin packages and on PD0 on 32-pins package.

9. Once the MTC peripheral is ON (bits CKE=1 or DAC=1 in the register MCRA), the pin PC4 is configured

to an alternate function. PC4 is no longer usable as a digital I/O.l

10. On the chip, each I/O port has 8 pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption. Refer to section 15.7 on page 303

3 REGISTER & MEMORY MAP

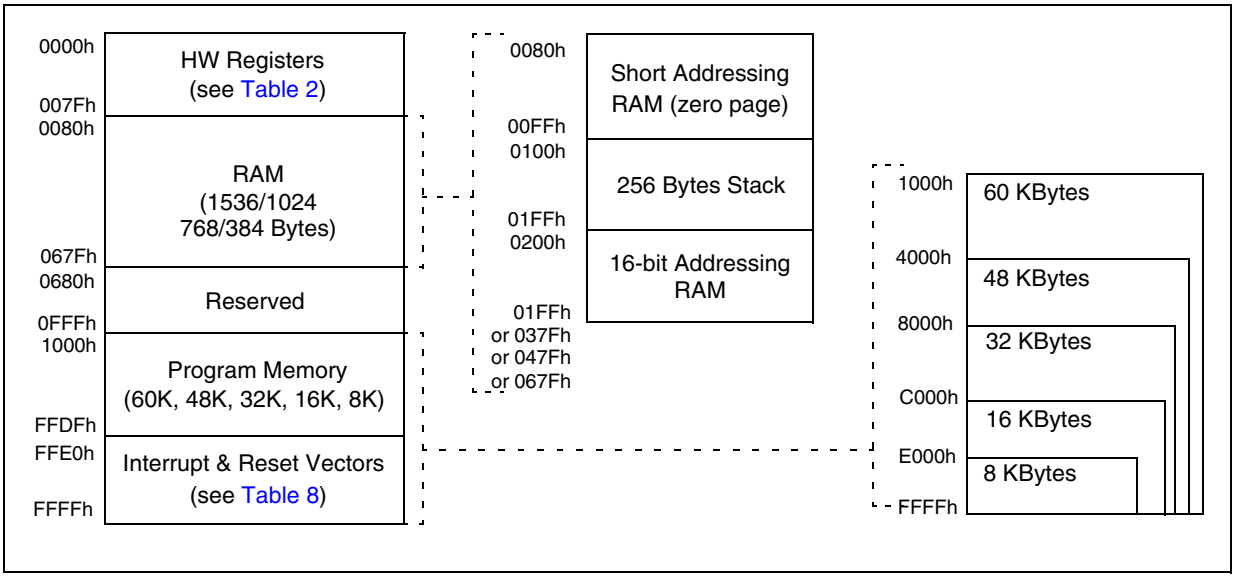
As shown in Figure 8, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, up to 2Kbytes of RAM and up to 60Kbytes of user program memory. The RAM space includes up to 256 bytes for the stack from 0100h to 01FFh.

The highest address bytes contain the user reset and interrupt vectors.

IMPORTANT: Memory locations marked as “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 8. Memory Map



As shown in Figure 9, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, up to 1536 bytes of RAM and up to 60 Kbytes of user program memory. The RAM space includes up to 256 bytes for the stack from 0100h to 01FFh.

The highest address bytes contain the user reset and interrupt vectors.

Table 2. Hardware Register Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h	Port A	PADR	Port A Data Register	00h[1]	R/W
0001h		PADDR	Port A Data Direction Register	00h	R/W
0002h		PAOR	Port A Option Register	00h	R/W[2]
0003h	Port B	PBDR	Port B Data Register	00h[1]	R/W
0004h		PBDDR	Port B Data Direction Register	00h	R/W
0005h		PBOR	Port B Option Register	00h	R/W
0006h	Port C	PCDR	Port C Data Register	00h[1]	R/W
0007h		PCDDR	Port C Data Direction Register	00h	R/W
0008h		PCOR	Port C Option Register	00h	R/W
0009h	Port D	PDDR	Port D Data Register	00h[1]	R/W
000Ah		PDDDR	Port D Data Direction Register	00h	R/W
000Bh		PDOR	Port D Option Register	00h	R/W
000Ch	Port E	PEDR	Port E Data Register	00h[1]	R/W
000Dh		PEDDR	Port E Data Direction Register	00h	R/W[2]
000Eh		PEOR	Port E Option Register	00h	R/W[2]
000Fh	Port F	PFDR	Port F Data Register	00h[1]	R/W
0010h		PFDDR	Port F Data Direction Register	00h	R/W
0011h		PFOR	Port F Option Register	00h	R/W
0012h	Port G	PGDR	Port G Data Register	00h[1]	R/W
0013h		PGDDR	Port G Data Direction Register	00h	R/W
0014h		PGOR	Port G Option Register	00h	R/W
0015h	Port H	PHDR	Port H Data Register	00h[1]	R/W
0016h		PHDDR	Port H Data Direction Register	00h	R/W
0017h		PHOR	Port H Option Register	00h	R/W
0018h	LINSCI™	SCISR	SCI Status Register	C0h	Read Only
0019h		SCIDR	SCI Data Register	xxh	R/W
001Ah		SCIBRR	SCI Baud Rate Register	00h	R/W
001Bh		SCICR1	SCI Control Register 1	xxh	R/W
001Ch		SCICR2	SCI Control Register 2	00h	R/W
001Dh		SCICR3	SCI Control Register 3	00h	R/W
001Eh		SCIERPR	SCI Extended Receive Prescaler Register	00h	R/W
001Fh		SCIETPR	SCI Extended Transmit Prescaler Register	00h	R/W
0020h	Reserved Area (1 Byte)				
0021h	SPI	SPIDR	SPI Data I/O Register	xxh	R/W
0022h		SPICR	SPI Control Register	0xh	R/W
0023h		SPICSR	SPI Control/Status Register	00h	R/W

Table 2. Hardware Register Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0024h	ITC	ITSPR0	Interrupt Software Priority Register 0	FFh	R/W
0025h		ITSPR1	Interrupt Software Priority Register 1	FFh	R/W
0026h		ITSPR2	Interrupt Software Priority Register 2	FFh	R/W
0027h		ITSPR3	Interrupt Software Priority Register 3	FFh	R/W
0028h		EICR	External Interrupt Control Register	00h	R/W
0029h	FLASH	FSCR	Flash Control/Status Register	00h	R/W
002Ah	WATCHDOG	WDGCR	Window Watchdog Control Register	7Fh	R/W
002Bh		WDGWR	Window Watchdog Window Register	7Fh	R/W
002Ch	MCC	MCCSR	Main Clock Control / Status Register	00h	R/W
002Dh		MCCBCR	Main Clock Controller: Beep Control Register	00h	R/W
002Eh	ADC	ADCCSR	Control/Status Register	00h	R/W
002Fh		ADCDRMSB	Data Register MSB	00h	Read Only
0030h		ADCDRLSB	Data Register LSB	00h	Read Only
0031h	TIMER A	TACR2	Timer A Control Register 2	00h	R/W
0032h		TACR1	Timer A Control Register 1	00h	R/W
0033h		TACSR	Timer A Control/Status Register	xxh	R/W
0034h		TAIC1HR	Timer A Input Capture 1 High Register	xxh	Read Only
0035h		TAIC1LR	Timer A Input Capture 1 Low Register	xxh	Read Only
0036h		TAOC1HR	Timer A Output Compare 1 High Register	80h	R/W
0037h		TAOC1LR	Timer A Output Compare 1 Low Register	00h	R/W
0038h		TACHR	Timer A Counter High Register	FFh	Read Only
0039h		TACLR	Timer A Counter Low Register	FCh	Read Only
003Ah		TAACHR	Timer A Alternate Counter High Register	FFh	Read Only
003Bh		TAACLR	Timer A Alternate Counter Low Register	FCh	Read Only
003Ch		TAIC2HR	Timer A Input Capture 2 High Register	xxh	Read Only
003Dh		TAIC2LR	Timer A Input Capture 2 Low Register	xxh	Read Only
003Eh		TAOC2HR	Timer A Output Compare 2 High Register	80h	R/W
003Fh		TAOC2LR	Timer A Output Compare 2 Low Register	00h	R/W
0040h	SIM	SICSR	System Integrity Control/Status Register	000x000x b	R/W
0041h	TIMER B	TBCR2	Timer B Control Register 2	00h	R/W
0042h		TBCR1	Timer B Control Register 1	00h	R/W
0043h		TBCSR	Timer B Control/Status Register	xxh	R/W
0044h		TBIC1HR	Timer B Input Capture 1 High Register	xxh	Read Only
0045h		TBIC1LR	Timer B Input Capture 1 Low Register	xxh	Read Only
0046h		TBOC1HR	Timer B Output Compare 1 High Register	80h	R/W
0047h		TBOC1LR	Timer B Output Compare 1 Low Register	00h	R/W
0048h		TBCHR	Timer B Counter High Register	FFh	Read Only
0049h		TBCLR	Timer B Counter Low Register	FCh	Read Only
004Ah		TBACHR	Timer B Alternate Counter High Register	FFh	Read Only
004Bh		TBACLR	Timer B Alternate Counter Low Register	FCh	Read Only
004Ch		TBIC2HR	Timer B Input Capture 2 High Register	xxh	Read Only
004Dh		TBIC2LR	Timer B Input Capture 2 Low Register	xxh	Read Only
004Eh		TBOC2HR	Timer B Output Compare 2 High Register	80h	R/W
004Fh		TBOC2LR	Timer B Output Compare 2 Low Register	00h	R/W

Table 2. Hardware Register Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0050h	MTC (page 0)	MTIM	Timer Counter High Register	00h	R/W
0051h		MTIML	Timer Counter Low Register	00h	R/W
0052h		MZPRV	Capture Z_{n-1} Register	00h	R/W
0053h		MZREG	Capture Z_n Register	00h	R/W
0054h		MCOMP	Compare C_{n+1} Register	00h	R/W
0055h		MDREG	Demagnetization Register	00h	R/W
0056h		MWGHT	A_n Weight Register	00h	R/W
0057h		MPRSR	Prescaler & Sampling Register	00h	R/W
0058h		MIMR	Interrupt Mask Register	00h	R/W
0059h		MISR	Interrupt Status Register	00h	R/W
005Ah		MCRA	Control Register A	00h	R/W
005Bh		MCRB	Control Register B	00h	R/W
005Ch		MCRC	Control Register C	00h	R/W
005Dh		MPHST	Phase State Register	00h	R/W
005Eh		MDFR	D event Filter Register	0Fh	R/W
005Fh		MCFR	Current feedback Filter Register	00h	R/W
0060h		MREF	Reference Register	00h	R/W
0061h		MPCR	PWM Control Register	00h	R/W
0062h		MREP	Repetition Counter Register	00h	R/W
0063h		MCPWH	Compare Phase W Preload Register High	00h	R/W
0064h		MCPWL	Compare Phase W Preload Register Low	00h	R/W
0065h		MCPVH	Compare Phase V Preload Register High	00h	R/W
0066h		MCPVL	Compare Phase V Preload Register Low	00h	R/W
0067h		MCPUH	Compare Phase U Preload Register High	00h	R/W
0068h		MCPUL	Compare Phase U Preload Register Low	00h	R/W
0069h		MCP0H	Compare Phase 0 Preload Register High	0Fh	R/W
006Ah		MCP0L	Compare Phase 0 Preload Register Low	FFh	R/W
0050h	MTC (page 1)	MDTG	Dead Time Generator Enable	FFh	see MTC description
0051h		MPOL	Polarity Register	3Fh	
0052h		MPWME	PWM Register	00h	
0053h		MCONF	Configuration Register	02h	
0054h		MPAR	Parity Register	00h	
0055h		MZRF	Z event Filter Register	0Fh	
0056h		MSCR	Sampling Clock Register	00h	
0057h to 006Ah		Reserved Area (4 Bytes)			
006Bh	DM	DMCR	Debug Control Register	00h	R/W
006Ch		DMSR	Debug Status Register	10h	Read Only
006Dh		DMBK1H	Debug Breakpoint 1 MSB Register	FFh	R/W
006Eh		DMBK1L	Debug Breakpoint 1 LSB Register	FFh	R/W
006Fh		DMBK2H	Debug Breakpoint 2 MSB Register	FFh	R/W
0070h		DMBK2L	Debug Breakpoint 2 LSB Register	FFh	R/W

Table 2. Hardware Register Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0074h	PWM ART	PWMDCR3	PWM AR Timer Duty Cycle Register 3	00h	R/W
0075h		PWMDCR2	PWM AR Timer Duty Cycle Register 2	00h	R/W
0076h		PWMDCR1	PWM AR Timer Duty Cycle Register 1	00h	R/W
0077h		PWMDCR0	PWM AR Timer Duty Cycle Register 0	00h	R/W
0078h		PWMCR	PWM AR Timer Control Register	00h	R/W
0079h		ARTCSR	Auto-Reload Timer Control/Status Register	00h	R/W
007Ah		ARTCAR	Auto-Reload Timer Counter Access Register	00h	R/W
007Bh		ARTARR	Auto-Reload Timer Auto-Reload Register	00h	R/W
007Ch		ARTICCSR	AR Timer Input Capture Control/Status Reg.	00h	R/W
007Dh		ARTICR1	AR Timer Input Capture Register 1	00h	Read Only
007Eh		ARTICR2	AR Timer Input Capture Register 2	00h	Read Only
007Fh	OPAMP	OACSR	OPAMP Control/Status Register	00h	R/W

Legend: x=undefined, R/W=read/write

Notes:

1. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.

2. The bits associated with unavailable pins must always keep their reset value.

4 FLASH PROGRAM MEMORY

4.1 INTRODUCTION

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a Byte-by-Byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (In-Circuit Programming) or IAP (In-Application Programming).

The array matrix organisation allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 MAIN FEATURES

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (In-Circuit Programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (In-Application Programming) In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (In-Circuit Testing) for downloading and executing user application test patterns in RAM
- Read-out protection
- Register Access Security System (RASS) to prevent accidental programming or erasing

4.3 STRUCTURE

The Flash memory is organised in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see Table 3). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see Figure 9). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 3. Sectors available in Flash devices

Flash Size (bytes)	Available Sectors
4K	Sector 0
8K	Sectors 0,1
> 8K	Sectors 0,1, 2

4.3.1 Read-out Protection

Read-out protection, when selected, provides a protection against Program Memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

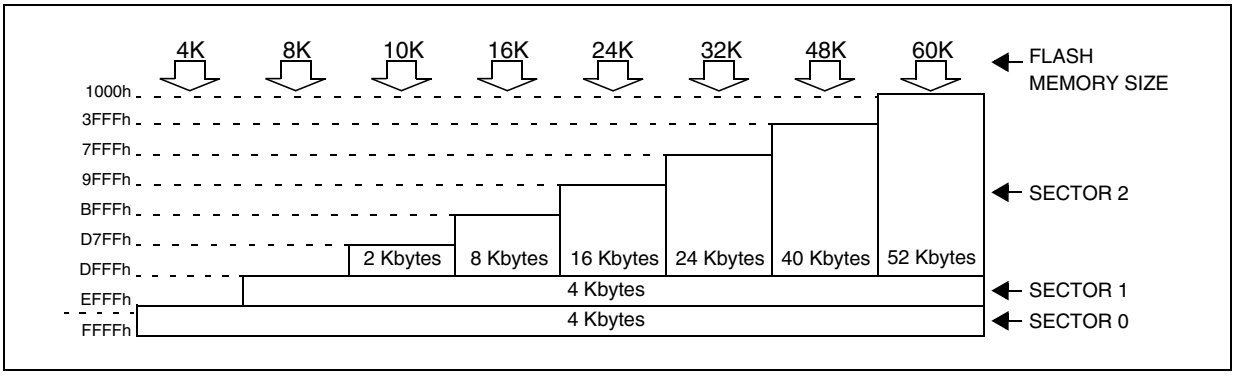
In Flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased and the device can be reprogrammed.

Read-out protection selection depends on the device type:

– In Flash devices it is enabled and removed through the FMP_R bit in the option byte.

– In ROM devices it is enabled by mask option specified in the Option List.

Figure 9. Memory Map and Sector Address



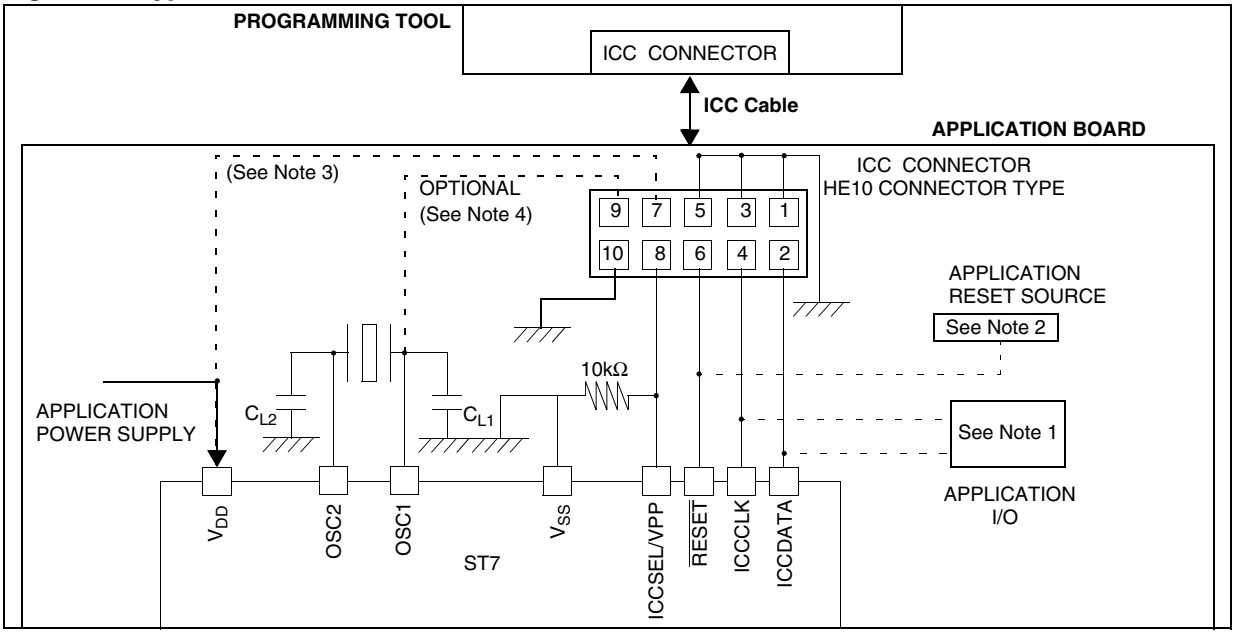
FLASH PROGRAM MEMORY (Cont'd)

4.4 ICC INTERFACE

ICC (In-Circuit Communication) needs a minimum of four and up to six pins to be connected to the programming tool (see Figure 10). These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input/output serial data pin
- ICCSEL/V_{PP}: programming voltage
- OSC1(or OSCIN): main clock input for external source (optional)
- V_{DD}: application board power supply (see Figure 10, Note 3)

Figure 10. Typical ICC Interface



Notes:

1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2. During the ICC session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1K). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R > 1K or a reset management IC with open drain output and pull-up resistor > 1K, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

3. The use of Pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4. Pin 9 has to be connected to the OSC1 or OSCIN pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC2 grounded in this case.

FLASH PROGRAM MEMORY (Cont'd)

4.5 ICP (IN-CIRCUIT PROGRAMMING)

To perform ICP the microcontroller must be switched to ICC (In-Circuit Communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see Figure 10). For more details on the pin locations, refer to the device pinout description.

4.6 IAP (IN-APPLICATION PROGRAMMING)

This mode uses a BootLoader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored, etc.). For example, it is possible to download code from the SPI, SCI or other type of serial interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.7 RELATED DOCUMENTATION

For details on Flash programming and ICC protocol, refer to the *ST7 Flash Programming Reference Manual* and to the *ST7 ICC Protocol Reference Manual*.

4.8 REGISTER DESCRIPTION

FLASH CONTROL/STATUS REGISTER (FCSR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	0	0

This register is reserved for use by Programming Tool software. It controls the Flash programming and erasing operations.

5 CENTRAL PROCESSING UNIT

5.1 INTRODUCTION

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

5.2 MAIN FEATURES

- Enable executing 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes (with indirect addressing mode)
- Two 8-bit index registers
- 16-bit stack pointer
- Low power Halt and Wait modes
- Priority maskable hardware interrupts
- Non-maskable software/hardware interrupts

5.3 CPU REGISTERS

The six CPU registers shown in Figure 11 are not present in the memory mapping and are accessed by specific instructions.

Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

Index Registers (X and Y)

These 8-bit registers are used to create effective addresses or as temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures.

Program Counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (Program Counter Low which is the LSB) and PCH (Program Counter High which is the MSB).

Figure 11. CPU Registers