



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





ST7SCR1E4, ST7SCR1R4

8-bit low-power, full-speed USB MCU with 16-Kbyte Flash, 768-byte RAM, smartcard interface and timer

Datasheet – production data

Features

Memories

- Up to 16 Kbytes of ROM or High Density Flash (HDFlash) program memory with read/write protection, HDFlash In-Circuit and In-Application Programming. 100 write/erase cycles guaranteed, data retention: 40 years at 55°C
- Up to 768 bytes of RAM including up to 128 bytes stack and 256 bytes USB buffer

Clock, reset and supply management

- Low voltage reset
- 2 power saving modes: Halt and Wait modes
- PLL for generating 48 MHz USB clock using a 4 MHz crystal

Interrupt management

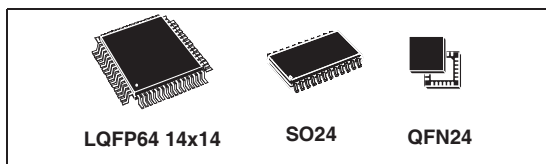
- Nested Interrupt controller

USB (Universal Serial Bus) interface

- 256-byte buffer for full speed bulk, control and interrupt transfer types compliant with USB specification (version 2.0)
- On-Chip 3.3V USB voltage regulator and transceivers with software power-down
- 7 USB endpoints:
 - One 8-byte Bidirectional Control Endpoint
 - One 64-byte In Endpoint,
 - One 64-byte Out Endpoint
 - Four 8-byte In Endpoints

35 or 4 I/O ports

- Up to 4 LED outputs with software programmable constant current (3 or 7 mA).
- 2 General purpose I/Os programmable as interrupts
- Up to 8 line inputs programmable as interrupts
- Up to 20 outputs
- 1 line assigned by default as static input after reset



ISO7816-3 UART interface

- 4 MHz clock generation
- Synchronous/Asynchronous protocols (T=0, T=1)
- Automatic retry on parity error
- Programmable baud rate from 372 clock pulses up to 11.625 clock pulses (D=32/F=372)
- Card Insertion/Removal Detection

Smartcard power supply

- Selectable card V_{CC} 1.8V, 3V, and 5V
- Internal step-up converter for 5V supplied Smartcards (with a current of up to 55mA) using only two external components.
- Programmable Smartcard Internal Voltage Regulator (1.8V to 3.0V) with current overload protection and 4 KV ESD protection (Human Body Model) for all Smartcard Interface I/Os

One 8-bit timer

- Time Base Unit (TBU) for generating periodic interrupts.

Development tools

- Full hardware/software development package

ECOPACK® packages

Table 1. Device summary

Reference	Part number
ST7SCR1R4	ST7FSCR1T1, ST7SCR1T1
ST7SCR1E4	ST7FSCR1M1, ST7SCR1M1, ST7SCR1U1

Contents

1	Description	8
2	Pin description	10
3	Register and memory map	16
4	Flash program memory	19
4.1	Introduction	19
4.2	Main features	19
4.3	Structure	19
4.4	ICP (In-circuit programming)	20
4.5	IAP (In-application programming)	20
4.6	Program memory read-out protection	21
4.7	Related documentation	21
4.8	Register description	22
5	Central processing unit	23
5.1	Introduction	23
5.2	Main features	23
5.3	CPU registers	23
6	Supply, reset and clock management	27
6.1	Clock system	27
6.1.1	General description	27
6.1.2	External clock	28
6.2	Reset sequence manager (RSM)	28
6.2.1	Introduction	28
6.2.2	Functional description	28
7	Interrupts	30
7.1	Introduction	30
7.2	Masking and processing flow	30
7.3	Interrupts and low power modes	33

7.4	Concurrent and nested management	33
7.5	Interrupt register description	34
8	Power saving modes	37
8.1	Introduction	37
8.2	Wait mode	37
8.3	Halt mode	38
9	I/O ports	40
9.1	Introduction	40
9.2	Functional description	40
9.3	I/O port implementation	41
9.3.1	Port A	41
9.3.2	Ports B and D	42
9.3.3	Port C	43
9.4	Register description	43
10	Miscellaneous registers	47
11	LEDs	50
12	On-chip peripherals	51
12.1	Watchdog timer (WDG)	51
12.1.1	Introduction	51
12.1.2	Main features	51
12.1.3	Functional description	51
12.1.4	Software watchdog option	52
12.1.5	Hardware watchdog option	52
12.1.6	Low power modes	52
12.1.7	Interrupts	53
12.1.8	Register description	53
12.2	Time base unit (TBU)	53
12.2.1	Introduction	53
12.2.2	Main features	54
12.2.3	Functional description	54
12.2.4	Programming example	54

12.2.5	Low power modes	55
12.2.6	Interrupts	55
12.2.7	Register description	55
12.3	USB interface (USB)	56
12.3.1	Introduction	56
12.3.2	Main features	56
12.3.3	Functional description	57
12.3.4	Register description	58
12.4	Smartcard interface (CRD)	69
12.4.1	Introduction	69
12.4.2	Main features	70
12.4.3	Functional description	70
12.4.4	Register description	77
13	Instruction set	88
13.1	CPU addressing modes	88
13.1.1	Inherent	89
13.1.2	Immediate	90
13.1.3	Direct	90
13.1.4	Indexed (No Offset, Short, Long)	90
13.1.5	Indirect (Short, Long)	90
13.1.6	Indirect indexed (Short, Long)	91
13.1.7	Relative mode (Direct, Indirect)	92
13.2	Instruction groups	92
14	Electrical characteristics	96
14.1	Absolute maximum ratings	96
14.2	Recommended operating conditions	97
14.3	Supply and reset characteristics	99
14.4	Clock and timing characteristics	100
14.4.1	General timings	100
14.4.2	External clock source	100
14.4.3	Crystal resonator oscillators	101
14.5	Memory characteristics	102
14.5.1	RAM and hardware registers	102
14.5.2	FLASH memory	102

14.6	Smartcard supply supervisor electrical characteristics	103
14.7	EMC characteristics	105
14.7.1	Functional EMS (Electro magnetic susceptibility)	105
14.7.2	Electro magnetic interference (EMI)	106
14.7.3	Absolute maximum ratings (electrical sensitivity)	106
14.8	Communication interface characteristics	107
14.8.1	USB - Universal bus interface	107
15	Package characteristics	109
15.1	Package mechanical data	109
15.2	Recommended reflow oven profile	110
16	Device configuration and ordering information	111
16.0.1	Option bytes	111
16.1	Device ordering information and transfer of customer code	112
16.2	Development tools	114
16.3	ST7 Application notes	115
16.4	Important notes	118
16.4.1	Unexpected reset fetch	118
16.4.2	Flash devices only	118
16.4.3	Smart card UART automatic repetition and retry	119
17	Revision history	120

List of tables

Table 1.	Device summary	1
Table 2.	Detailed device summary	8
Table 3.	Pin description	11
Table 4.	Hardware register memory map	17
Table 5.	Sectors available in FLASH devices	19
Table 6.	Recommended values for 4 MHz crystal resonator	28
Table 7.	Interrupt software priority levels	31
Table 8.	Current interrupt software priority	34
Table 9.	Interrupt vectors and corresponding bits	35
Table 10.	Dedicated interrupt instruction set	35
Table 11.	Interrupt mapping	36
Table 12.	I/O pin functions	40
Table 13.	Port A description	41
Table 14.	Port B and D description	42
Table 15.	Port C description	43
Table 16.	I/O ports register map	45
Table 17.	Register map and reset values	49
Table 18.	Watchdog timing (fCPU = 8 MHz)	51
Table 19.	Transmission status encoding	64
Table 20.	Reception status encoding	64
Table 21.	Transmission status encoding	66
Table 22.	Reception status encoding	67
Table 23.	USB register map and reset values	68
Table 24.	Register map and reset values	86
Table 25.	CPU addressing mode overview	88
Table 26.	Instructions supporting direct, indexed, indirect and indirect indexed addressing modes	91
Table 27.	Instruction set overview	93
Table 28.	Thermal characteristics	97
Table 29.	Current injection on i/o port and control pins	97
Table 30.	I/O port pins	98
Table 31.	LED pins	99
Table 32.	Low voltage detector and supervisor (LVDS)	99
Table 33.	Typical crystal resonator	101
Table 34.	Dual voltage flash memory	102
Table 35.	Smartcard supply supervisor	103
Table 36.	Absolute maximum ratings	106
Table 37.	Electrical sensitivities	107
Table 38.	USB DC electrical characteristics	107
Table 39.	USB: Full speed electrical characteristics	108
Table 40.	Ordering information	113
Table 41.	Development tools	114
Table 42.	ST7 Application notes	115
Table 43.	Device identification	118
Table 44.	Document revision history	120

List of figures

Figure 1.	ST7SCR block diagram	9
Figure 2.	64-pin LQFP package pinout	10
Figure 3.	24-Pin SO package pinout	10
Figure 4.	24-lead QFN package pinout	11
Figure 5.	Smartcard interface reference application - 24-pin SO package	14
Figure 6.	Smartcard interface reference application - 64-Pin LQFP package	15
Figure 7.	Memory map	16
Figure 8.	Memory map and sector address	20
Figure 9.	Typical ICP interface	21
Figure 10.	CPU registers	24
Figure 11.	Stack manipulation example	26
Figure 12.	Clock, reset and supply block diagram	27
Figure 13.	External clock source connections	28
Figure 14.	Crystal resonator	28
Figure 15.	LVD RESET sequence	29
Figure 16.	Watchdog RESET sequence	29
Figure 17.	Interrupt processing flowchart	31
Figure 18.	Priority decision process	31
Figure 19.	Concurrent interrupt management	33
Figure 20.	Nested interrupt management	34
Figure 21.	WAIT mode flow chart	38
Figure 22.	HALT mode flow chart	39
Figure 23.	PA0, PA1, PA2, PA3, PA4, PA5 configuration	42
Figure 24.	PA6 configuration	42
Figure 25.	Port B and D configuration	43
Figure 26.	Port C configuration	43
Figure 27.	Watchdog block diagram	52
Figure 28.	TBU block diagram	54
Figure 29.	USB block diagram	57
Figure 30.	Endpoint buffer size	58
Figure 31.	Smartcard interface block diagram	70
Figure 32.	Compensation mode	72
Figure 33.	Waiting time counter example	73
Figure 34.	Card detection block diagram	74
Figure 35.	Card deactivation sequence	75
Figure 36.	Card voltage selection and power OFF block diagram	76
Figure 37.	Power off timing diagram	76
Figure 38.	Card clock selection block diagram	77
Figure 39.	Smartcard I/O pin structure	81
Figure 40.	Typical application with an external clock source	100
Figure 41.	Typical application with a crystal resonator	101
Figure 42.	Two typical applications with VPP pin1)	102
Figure 43.	USB: Data signal rise and fall time	107
Figure 44.	64-pin low profile quad flat package (14x14)	109
Figure 45.	24-pin plastic small outline package, 300-mil width	109
Figure 46.	Sales type coding rules	112
Figure 47.	ST7SCR microcontroller option list	114
Figure 48.	Revision marking on box label and device marking	119

1 Description

The ST7SCR and ST7FSCR devices are members of the ST7 microcontroller family designed for USB applications. All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

The ST7SCR ROM devices are factory-programmed and are not reprogrammable.

The ST7FSCR versions feature dual-voltage Flash memory with Flash Programming capability.

They operate at a 4 MHz external oscillator frequency.

Under software control, all devices can be placed in WAIT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

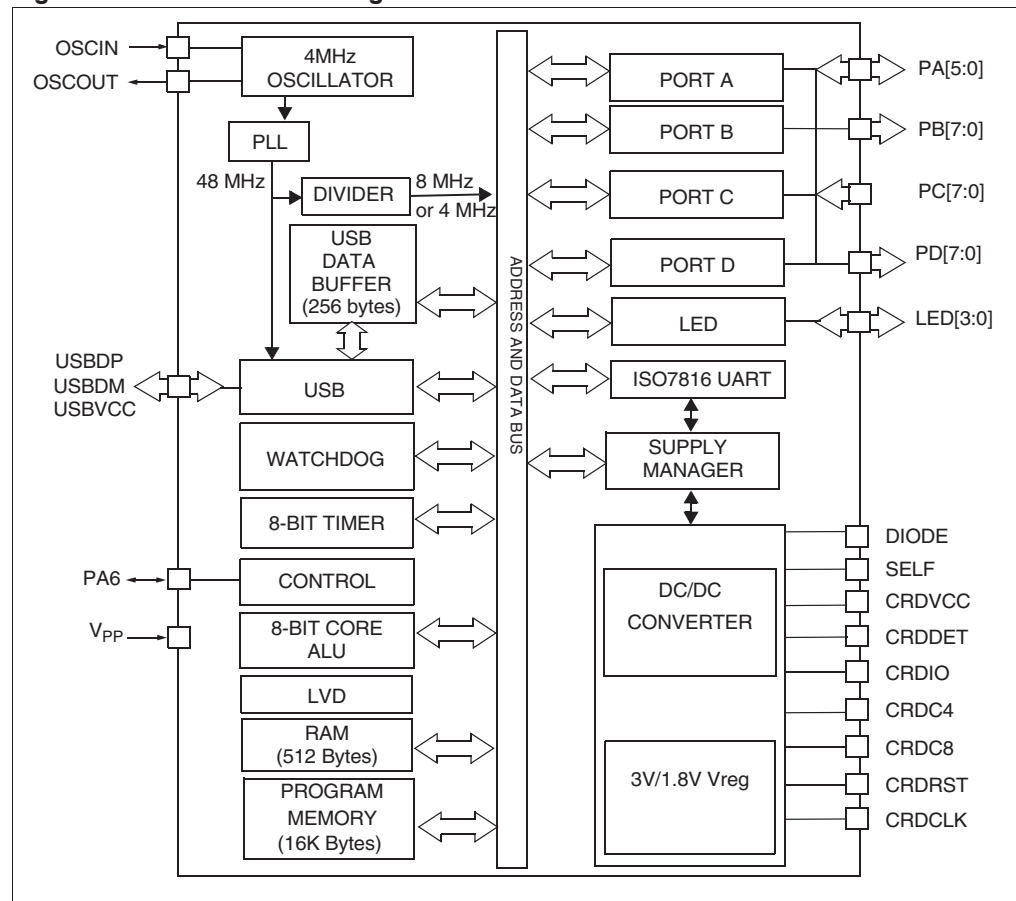
The devices include an ST7 core, up to 16 Kbytes of program memory, up to 512 bytes of user RAM, up to 35 I/O lines and the following on-chip peripherals:

- USB full speed interface with 7 endpoints, programmable in/out configuration and embedded 3.3V voltage regulator and transceivers (no external components are needed).
- ISO7816-3 UART interface with programmable baud rate from 372 clock pulses up to 11.625 clock pulses
- Smartcard Supply Block able to provide programmable supply voltage and I/O voltage levels to the smartcards
- Low voltage reset ensuring proper power-on or power-off of the device (selectable by option)
- Watchdog timer
- 8-bit timer (TBU)

Table 2. Detailed device summary

Features	ST7SCR1R4		ST7SCR1E4		
	ST7FSCR1T1	ST7SCR1T1	ST7FSCR1M1	ST7SCR1M1	ST7SCR1U1
Program memory	16 Kbytes FLASH	16 Kbytes ROM	16 Kbytes FLASH	16 Kbytes ROM	16 Kbytes ROM
User RAM (stack) bytes	768 (128)				
Peripherals	USB full-speed (7 Ep), TBU, Watchdog timer, ISO7816-3 interface				
Operating supply	4.0 to 5.5V				
CPU frequency	4 or 8 MHz				
Operating temperature	0°C to +70°C				
Package	LQFP64		SO24		QFN24

Figure 1. ST7SCR block diagram



2 Pin description

Figure 2. 64-pin LQFP package pinout

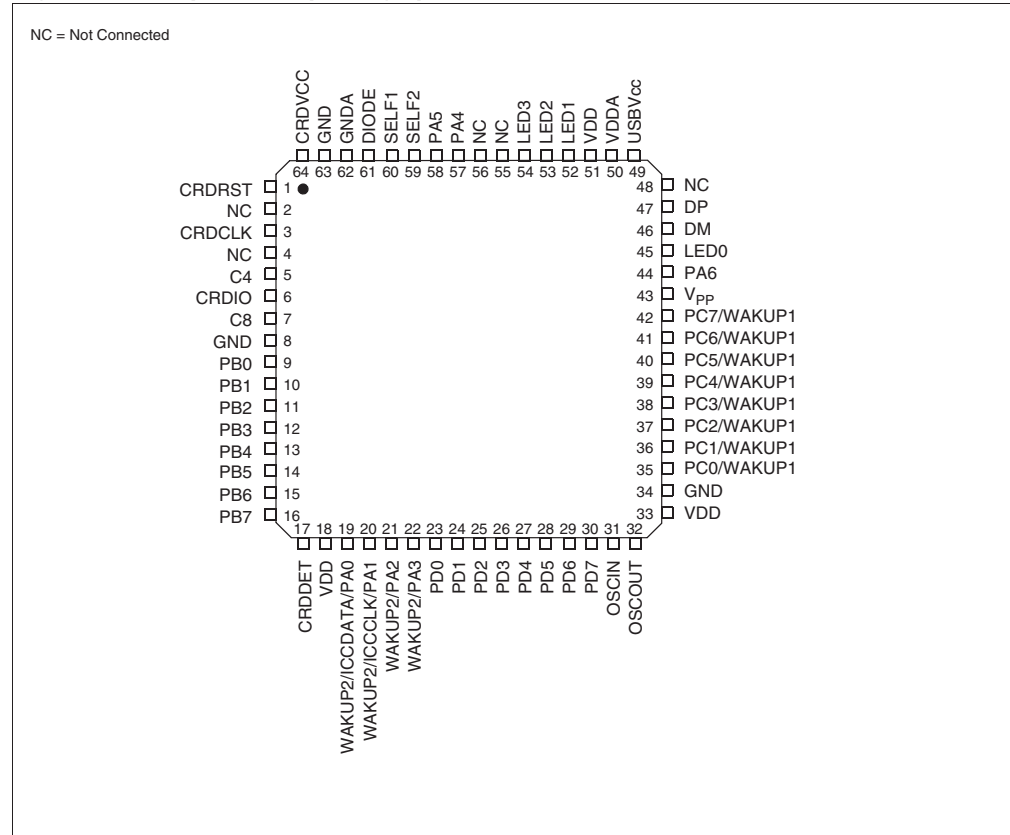


Figure 3. 24-Pin SO package pinout

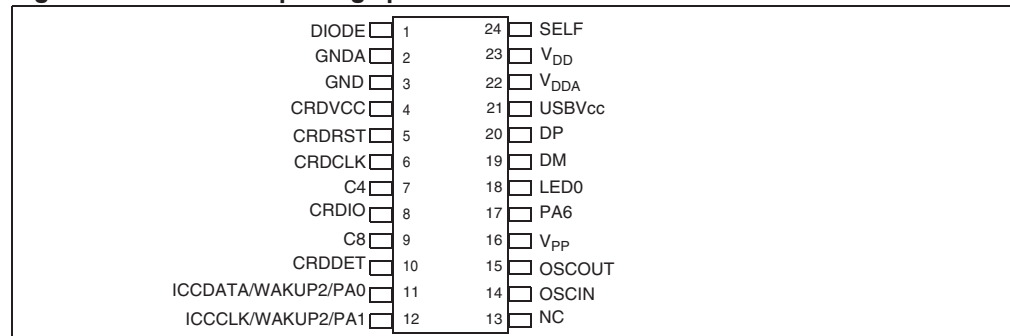
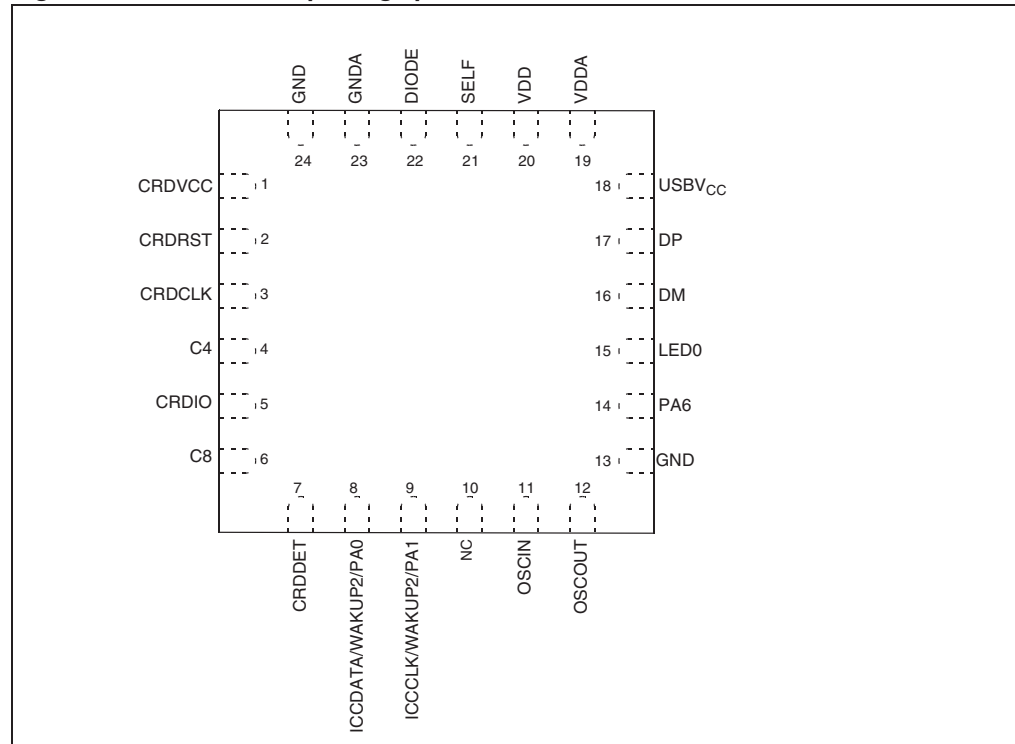


Figure 4. 24-lead QFN package pinout



Legend / Abbreviations:

Type: I = input, O = output, S = supply

In/Output level: $C_T = \text{CMOS } 0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 10mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull

Refer to [“I/O ports” on page 40](#) for more details on the software configuration of the I/O ports.

Table 3. Pin description

Pin n°			Pin name	Type	Level		V _{CARD} supplied	Port / Control				Main function (after reset)	Alternate function
LQFP64	QFN24	SO24			Input	Output		Input		Output			
								wpu	int	OD	PP		
1	2	5	CRDRST	O		C _T	X				X	Smartcard Reset	
2			NC									Not Connected	
3	3	6	CRDCLK	O		C _T	X				X	Smartcard Clock	

Table 3. Pin description (continued)

Pin n°			Pin name	Type	Level		V _{CARD} supplied	Port / Control				Main function (after reset)	Alternate function
LQFP64	QFN24	S024			Input	Output		Input		Output			
								wpu	int	OD	PP		
4			NC									Not Connected	
5	4	7	C4	O		C _T	X				X	Smartcard C4	
6	5	8	CRDIO	I/O	C _T		X	X		X		Smartcard I/O	
7	6	9	C8	O		C _T	X				X	Smartcard C8	
8		3	GND	S								Ground	
9			PB0	O		C _T				X	X	Port B0 ⁽¹⁾	
10			PB1	O		C _T				X	X	Port B1 ⁽¹⁾	
11			PB2	O		C _T				X	X	Port B2 ⁽¹⁾	
12			PB3	O		C _T				X	X	Port B3 ⁽¹⁾	
13			PB4	O		C _T				X	X	Port B4 ⁽¹⁾	
14			PB5	O		C _T				X	X	Port B5 ⁽¹⁾	
15			PB6	O		C _T				X	X	Port B6 ⁽¹⁾	
16			PB7	O		C _T				X	X	Port B7 ⁽¹⁾	
17	7	10	CRDDET	I	C _T			X				Smartcard Detection	
18			VDD	S								Power Supply voltage 4V-5.5V	
19	8	11	PA0/WAKUP2/ ICCDATA	I/O	C _T			X	X	X	X	Port A0	Interrupt, In-Circuit Communication Data Input
20	9	12	PA1/WAKUP2/ ICCCLK	I/O	C _T			X	X	X	X	Port A1	Interrupt, In-Circuit Communication Clock Input
21			PA2/WAKUP2	I/O	C _T			X	X	X	X	Port A2 ⁽¹⁾	Interrupt
22			PA3/WAKUP2	I/O	C _T			X	X	X	X	Port A3 ⁽¹⁾	Interrupt
23			PD0	O		C _T				X	X	Port D0 ⁽¹⁾	
24			PD1	O		C _T				X	X	Port D1 ⁽¹⁾	
25			PD2	O		C _T				X	X	Port D2 ⁽¹⁾	
26			PD3	O		C _T				X	X	Port D3 ⁽¹⁾	
27			PD4	O		C _T				X	X	Port D4 ⁽¹⁾	
28			PD5	O		C _T				X	X	Port D5 ⁽¹⁾	
29			PD6	O		C _T				X	X	Port D6 ⁽¹⁾	
30			PD7	O		C _T				X	X	Port D7 ⁽¹⁾	
31	11	14	OSCIN		C _T							Input/Output Oscillator pins. These pins connect a 4MHz parallel-resonant crystal, or an external source to the on-chip oscillator.	
32	12	15	OSCOUT			C _T							
33			VDD	S								Power Supply voltage 4V-5.5V	

Table 3. Pin description (continued)

Pin n°			Pin name	Type	Level		V _{CARD} supplied	Port / Control				Main function (after reset)	Alternate function
LQFP64	QFN24	S024			Input	Output		Input		Output			
								wpu	int	OD	PP		
34			GND	S								Ground	
35			PC0/WAKUP1	I	C _T			X	X			PC0 ⁽¹⁾	External interrupt
36			PC1/WAKUP1	I	C _T			X	X			PC1 ⁽¹⁾	External interrupt
37			PC2/WAKUP1	I	C _T			X	X			PC2 ⁽¹⁾	External interrupt
38			PC3/WAKUP1	I	C _T			X	X			PC3 ⁽¹⁾	External interrupt
39			PC4/WAKUP1	I	C _T			X	X			PC4 ⁽¹⁾	External interrupt
40			PC5/WAKUP1	I	C _T			X	X			PC5 ⁽¹⁾	External interrupt
41			PC6/WAKUP1	I	C _T			X	X			PC6 ⁽¹⁾	External interrupt
42			PC7/WAKUP1	I	C _T			X	X			PC7 ⁽¹⁾	External interrupt
43		16	V _{PP}	S								Flash programming voltage. Must be held low in normal operating mode.	
	13		GND	S								Must be held low in normal operating mode.	
44	14	17	PA6	I	C _T							PA6	
45	15	18	LED0	O		HS				X		Constant Current Output	
46	16	19	DM	I/O	C _T							USB Data Minus line	
47	17	20	DP	I/O	C _T							USB Data Plus line	
48			NC									Not Connected	
49	18	21	USBVCC	O		C _T						3.3 V Output for USB	
50	19	22	V _{DDA}	S								power Supply voltage 4V-5.5V	
51	20	23	V _{DD}	S								power Supply voltage 4V-5.5V	
52			LED1	O		HS				X		Constant Current Output	
53			LED2	O		HS				X		Constant Current Output	
54			LED3	O		HS				X		Constant Current Output	
55			NC									Not Connected	
56			NC									Not Connected	
57			PA4	I/O	C _T			X	X	X	X	Port A4	
58			PA5	I/O	C _T			X	X	X	X	Port A5	
59	21	24	SELF2	O		C _T						An External inductance must be connected to these pins for the step up converter (refer to Figure 5 to choose the right capacitance)	
60	21	24	SELF1	O		C _T							
61	22	1	DIODE	S		C _T						An External diode must be connected to this pin for the step up converter (refer to Figure 5 to choose the right component)	

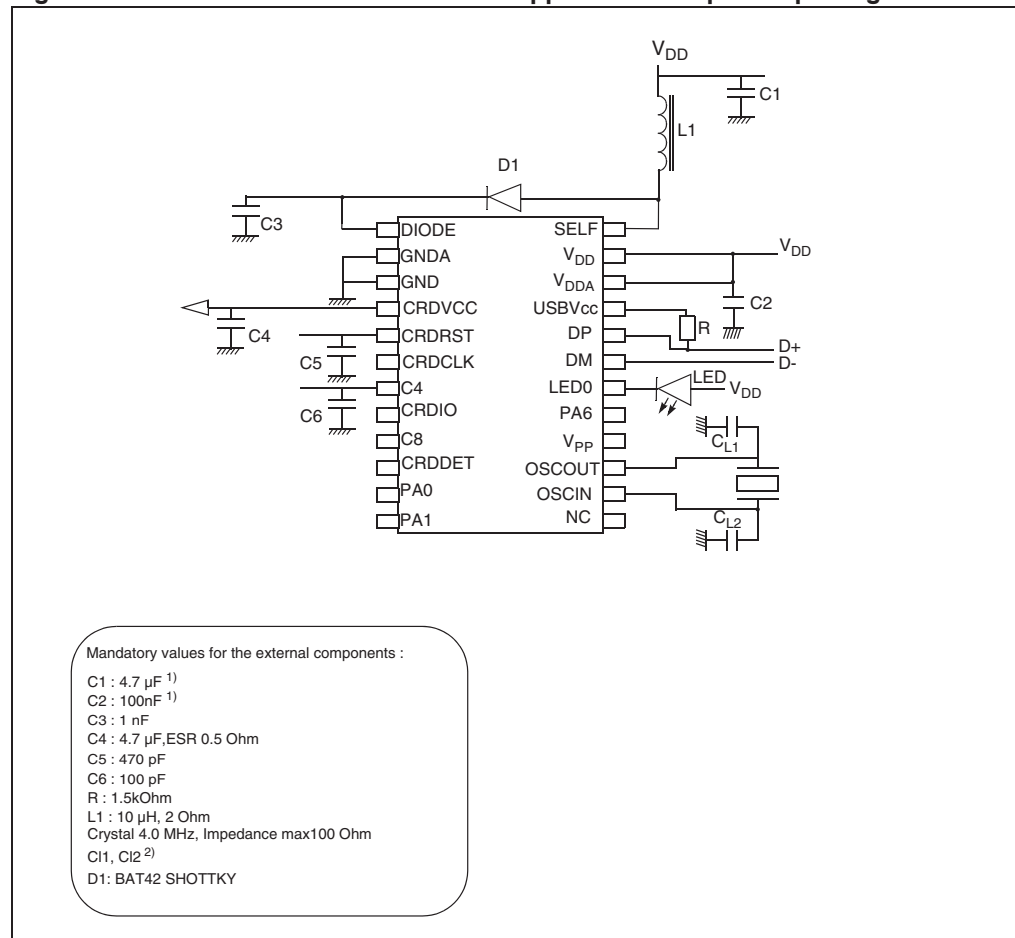
Table 3. Pin description (continued)

Pin n°			Pin name	Type	Level		V _{CARD} supplied	Port / Control				Main function (after reset)	Alternate function
LQFP64	QFN24	SO24			Input	Output		Input		Output			
								wpu	int	OD	PP		
62	23	2	GNDA	S								Ground	
63	24	3	GND	S									
64	1	4	CRDVCC	O		C _T	X					Smartcard Supply pin	

1. Keyboard interface

Note: It is mandatory to connect all available VDD and VDDA pins to the supply voltage and all VSS and VSSA pins to ground.

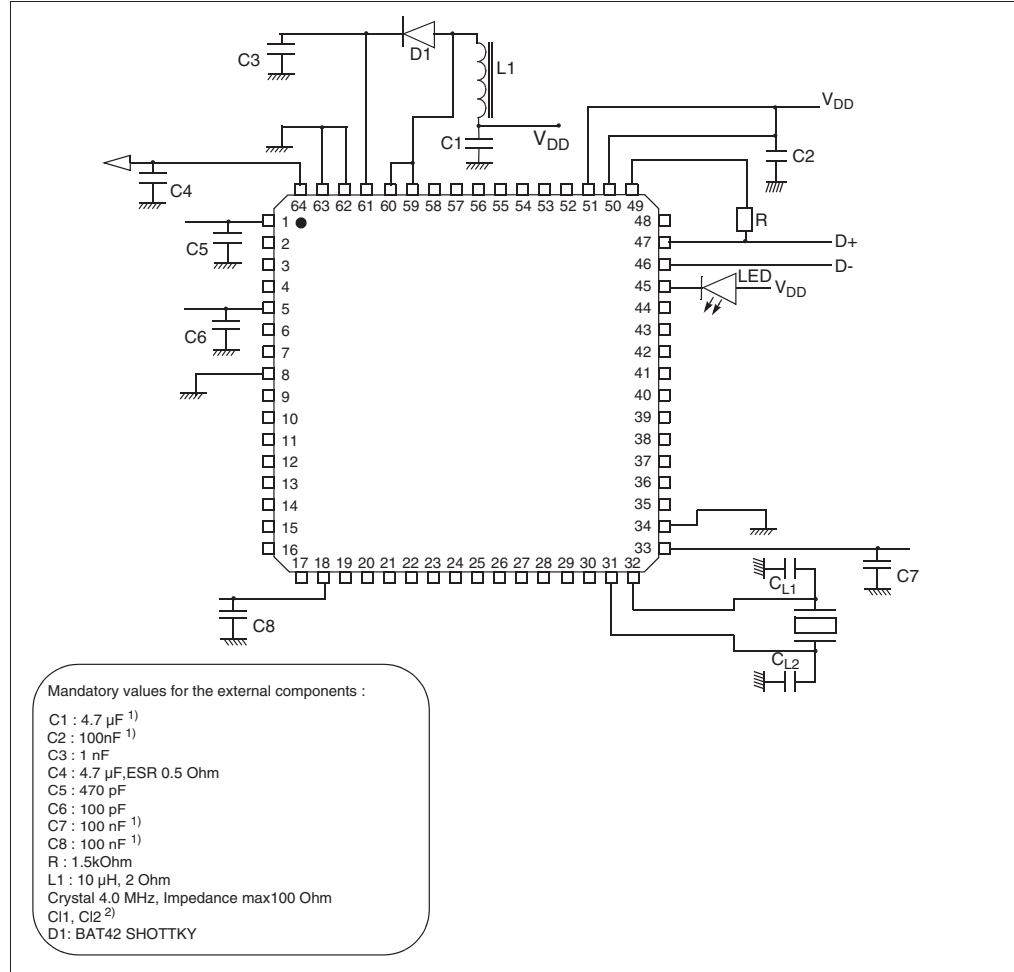
Figure 5. Smartcard interface reference application - 24-pin SO package



Note: C1 and C2 must be located close to the chip.

Refer to [Section 6: Supply, reset and clock management](#) & [Section 14.4.3 Crystal resonator oscillators](#).

Figure 6. Smartcard interface reference application - 64-Pin LQFP package



Note: C1, C2, C7 and C8 must be located close to the chip.

Refer to [Section 6: Supply, reset and clock management](#) and [Section 14.4.3 Crystal resonator oscillators](#).

3 Register and memory map

As shown in [Figure 7](#), the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 40 bytes of register locations, up to 512 bytes of RAM and up to 16K bytes of user program memory. The RAM space includes up to 128 bytes for the stack from 0100h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

IMPORTANT: Memory locations noted “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 7. Memory map

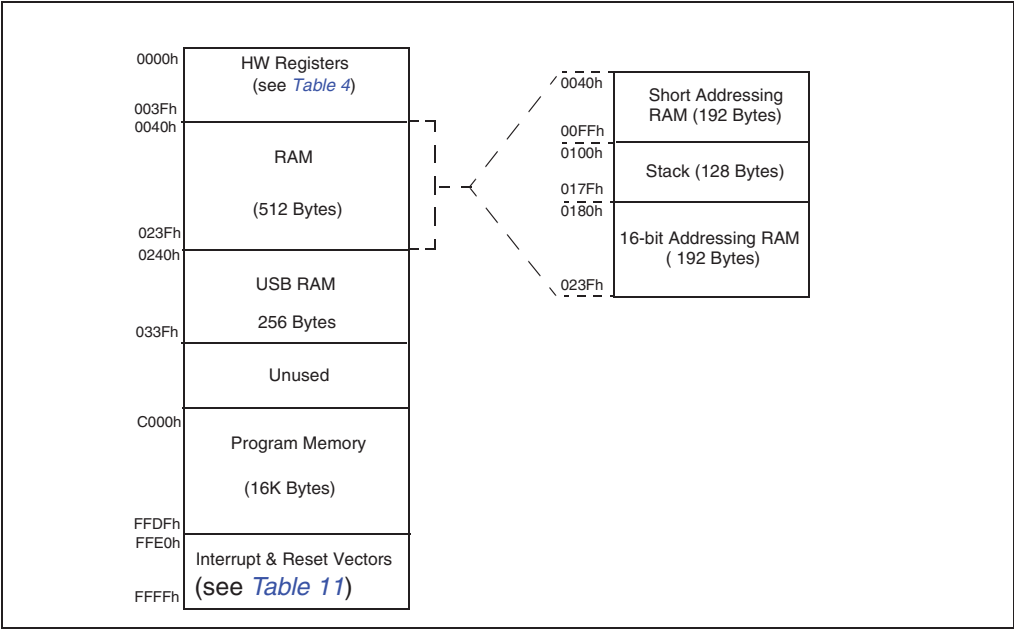


Table 4. Hardware register memory map

Address	Block	Register label	Register name	Reset status	Remarks
0000h	CRD	CRDCR	Smartcard Interface Control Register	00h	R/W
0001h		CRDSR	Smartcard Interface Status Register	80h	R/W
0002h		CRDCCR	Smartcard Contact Control Register	xxh	R/W
0003h		CRDETU1	Smartcard Elementary Time Unit 1	01h	R/W
0004h		CRDETU0	Smartcard Elementary Time Unit 0	74h	R/W
0005h		CRDGT1	Smartcard Guard time 1	00h	R/W
0006h		CRDGT0	Smartcard Guard time 0	0Ch	R/W
0007h		CRDWT2	Smartcard Character Waiting Time 2	00h	R/W
0008h		CRDWT1	Smartcard Character Waiting Time 1	25h	R/W
0009h		CRDWT0	Smartcard Character Waiting Time 0	80h	R/W
000Ah		CRDIER	Smartcard Interrupt Enable Register	00h	R/W
000Bh		CRDIPR	Smartcard Interrupt Pending Register	00h	R
000Ch		CRDTXB	Smartcard Transmit Buffer Register	00h	R/W
000Dh		CRDRXB	Smartcard Receive Buffer Register	00h	R
000Eh	Watchdog	WDGCR	Watchdog Control Register	00h	R/W
0011h	Port A	PADR	Port A Data Register	00h	R/W
0012h		PADDR	Port A Data Direction Register	00h	R/W
0013h		PAOR	Option Register	00h	R/W
0014h		PAPUCR	Pull up Control Register	00h	R/W
0015h	Port B	PBDR	Port B Data Register	00h	R/W
0016h		PBOR	Option Register	00h	R/W
0017h		PBPUCR	Pull up Control Register	00h	R/W
0018h	Port C	PCDR	Port C Data Register	00h	R/W
0019h	Port D	PDDR	Port D Data Register	00h	R/W
001Ah		PDOR	Option Register	00h	R/W
001Bh		PDPUCR	Pull up Control Register	00h	R/W
001Ch	MISC	MISCR1	Miscellaneous Register 1	00h	R/W
001Dh		MISCR2	Miscellaneous Register 2	00h	R/W
001Eh		MISCR3	Miscellaneous Register 3	00h	R/W
001Fh		MISCR4	Miscellaneous Register 4	00h	R/W

Table 4. Hardware register memory map (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0020h	USB	USBISTR	USB Interrupt Status Register	00h	R/W
0021h		USBIMR	USB Interrupt Mask Register	00h	R/W
0022h		USBCTLR	USB Control Register	06h	R/W
0023h		DADDR	Device Address Register	00h	R/W
0024h		USBSR	USB Status Register	00h	R/W
0025h		EPOR	Endpoint 0 Register	0xh	R/W
0026h		CNT0RXR	EP 0 Reception Counter Register	00h	R/W
0027h		CNT0TXR	EP 0 Transmission Counter Register	00h	R/W
0028h		EP1TXR	EP 1 Transmission Register	00h	R/W
0029h		CNT1TXR	EP 1 Transmission Counter Register	00h	R/W
002Ah		EP2RXR	EP 2 Reception Register	00h	R/W
002Bh		CNT2RXR	EP 2 Reception Counter Register	0xh	R/W
002Ch		EP2TXR	EP 2 Transmission Register	00h	R/W
002Dh		CNT2TXR	EP 2 Transmission Counter Register	00h	R/W
002Eh		EP3TXR	EP 3 Transmission Register	00h	R/W
002Fh		CNT3TXR	EP 3 Transmission Counter Register	00h	R/W
0030h		EP4TXR	EP 4 Transmission Register	00h	R/W
0031h		CNT4TXR	EP 4 Transmission Counter Register	00h	R/W
0032h		EP5TXR	EP 5 Transmission Register	00h	R/W
0033h		CNT5TXR	EP 5 Transmission Counter Register	00h	R/W
0034h		ERRSR	Error Status Register	00h	R/W
0035h	TBU	TBUCV	Timer counter value	00h	R/W
0036h		TBUCSR	Timer control status	00h	R/W
0037h	ITC	ITSPR0	Interrupt Software Priority Register 0	FFh	R/W
0038h		ITSPR1	Interrupt Software Priority Register 1	FFh	R/W
0039h		ITSPR2	Interrupt Software Priority Register 2	FFh	R/W
003Ah		ITSPR3	Interrupt Software Priority Register 3	FFh	R/W
003Eh		LED_CTRL	LED Control Register	00h	R/W

4 Flash program memory

4.1 Introduction

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a Byte-by-Byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (In-Circuit Programming) or IAP (In-Application Programming).

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- Three Flash programming modes:
 - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
 - ICP (In-Circuit Programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
 - IAP (In-Application Programming). In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (In-Circuit Testing) for downloading and executing user application test patterns in RAM
- Read-out protection
- Register Access Security System (RASS) to prevent accidental programming or erasing

4.3 Structure

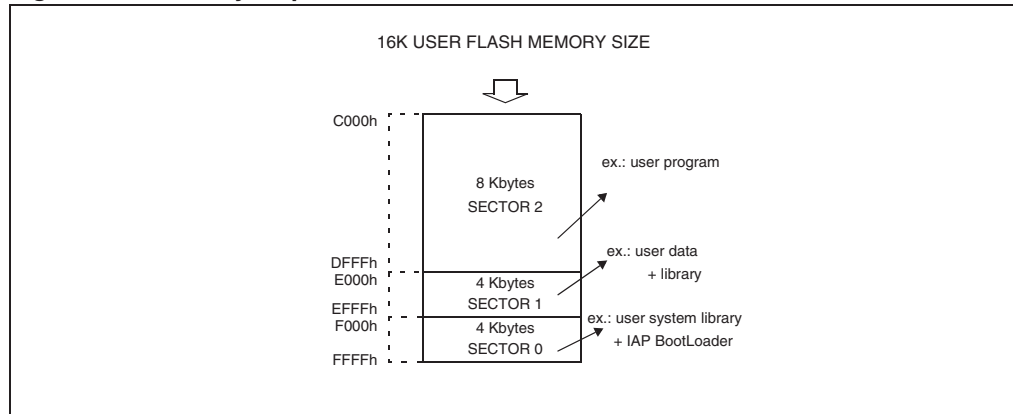
The Flash memory is organized in sectors and can be used for both code and data storage.

Depending on the overall FLASH memory size in the microcontroller device, there are up to three user sectors (see [Table 5](#)). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see [Figure 8](#)). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 5. Sectors available in FLASH devices

Flash Memory Size (bytes)	Available Sectors
4K	Sector 0
8K	Sectors 0,1
> 8K	Sectors 0,1, 2

Figure 8. Memory map and sector address

4.4 ICP (In-circuit programming)

To perform ICP the microcontroller must be switched to ICC (In-Circuit Communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see [Figure 9](#)). For more details on the pin locations, refer to the device pinout description.

ICP needs six signals to be connected to the programming tool. These signals are:

- V_{SS} : device power supply ground
- V_{DD} : for reset by LVD
- OSCIN: to force the clock during power-up
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input serial data pin
- V_{PP} : ICC mode selection and programming voltage.

If ICCCLK or ICCDATA are used for other purposes in the application, a serial resistor has to be implemented to avoid a conflict in case one of the other devices forces the signal level.

Note: To develop a custom programming tool, refer to the ST7 FLASH Programming and ICC Reference Manual which gives full details on the ICC protocol hardware and software.

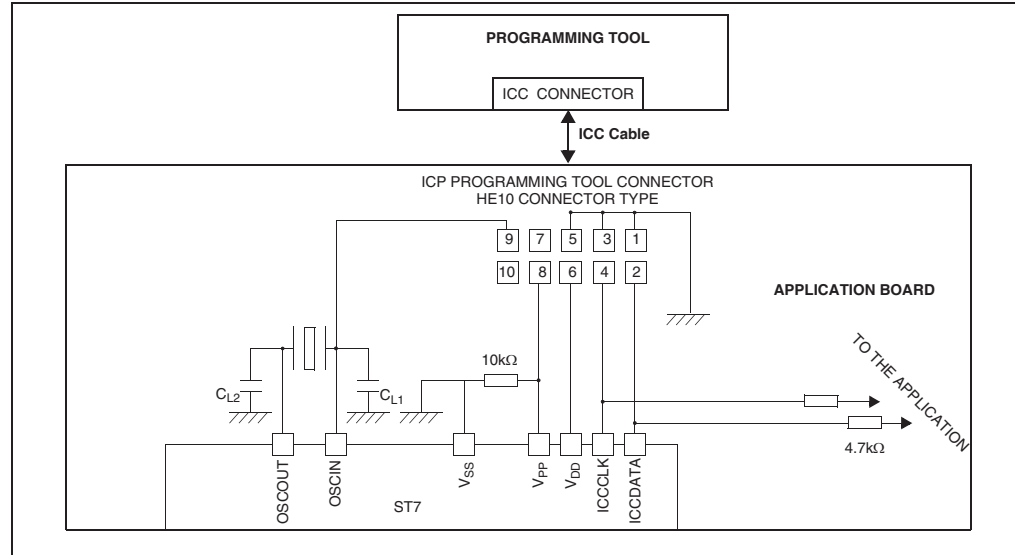
4.5 IAP (In-application programming)

This mode uses a BootLoader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored, etc.). For example, it is

possible to download code from the USB interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

Figure 9. Typical ICP interface



Note: *If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.*

4.6 Program memory read-out protection

The read-out protection is enabled through an option bit.

For Flash devices, when this option is selected, the program and data stored in the Flash memory are protected against read-out (including a re-write protection). When this protection is removed by reprogramming the Option Byte, the entire Flash program memory is first automatically erased and the device can be reprogrammed.

Refer to the Option Byte description for more details.

4.7 Related documentation

For details on Flash programming and ICC protocol, refer to the ST7 Flash Programming Reference Manual and to the ST7 ICC Protocol Reference Manual.

4.8 Register description

FLASH control/status register (FCSR)

Read/Write

Reset Value: 0000 0000 (00h)

7				0			
0	0	0	0	0	0	0	0

This register is reserved for use by Programming Tool software. It controls the FLASH programming and erasing operations. For details on customizing FLASH programming methods and In-Circuit Testing, refer to the ST7 FLASH Programming and ICC Reference Manual.



5 Central processing unit

5.1 Introduction

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

5.2 Main features

- Enable executing 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes (with indirect addressing mode)
- Two 8-bit index registers
- 16-bit stack pointer
- Low power HALT and WAIT modes
- Priority maskable hardware interrupts
- Non-maskable software/hardware interrupts

5.3 CPU registers

The 6 CPU registers shown in [Figure 10](#) are not present in the memory mapping and are accessed by specific instructions.

Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

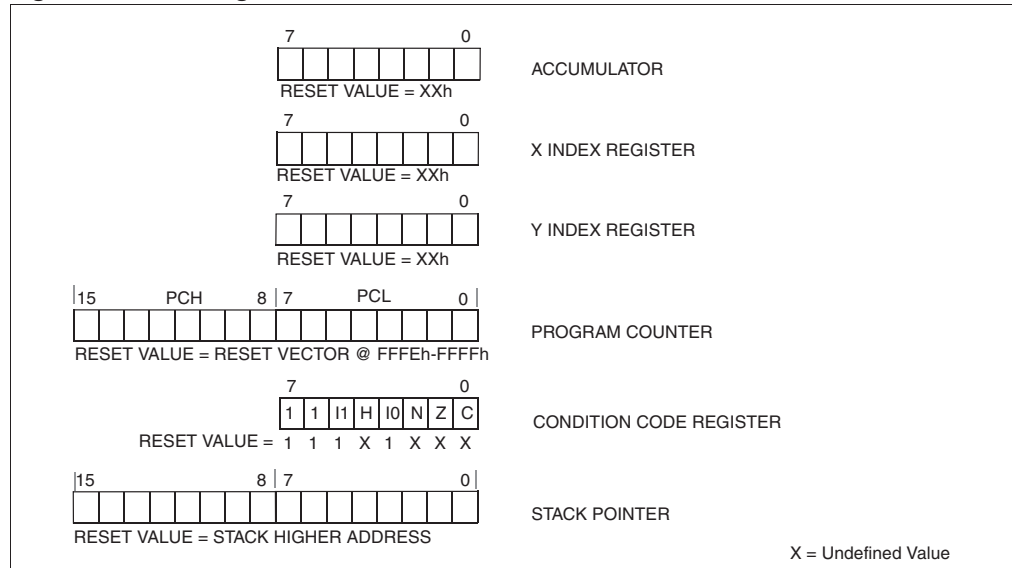
Index registers (X and Y)

These 8-bit registers are used to create effective addresses or as temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures.

Program counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (Program Counter Low which is the LSB) and PCH (Program Counter High which is the MSB).

Figure 10. CPU registers**Condition code register (CC)**

Read/Write

Reset Value: 111x1xxx

7							0
1	1	I1	H	I0	N	Z	C

The 8-bit Condition Code register contains the interrupt masks and four flags representative of the result of the instruction just executed. This register can also be handled by the PUSH and POP instructions.

These bits can be individually tested and/or controlled by specific instructions.

Arithmetic management bitsBit 4 = **H** *Half carry*.

This bit is set by hardware when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instructions. It is reset by hardware during the same instructions.

0: No half carry has occurred.

1: A half carry has occurred.

This bit is tested using the JRH or JRNH instruction. The H bit is useful in BCD arithmetic subroutines.

Bit 2 = **N** *Negative*.

This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It's a copy of the result 7th bit.

0: The result of the last operation is positive or null.

1: The result of the last operation is negative (i.e. the most significant bit is a logic 1).

This bit is accessed by the JRMI and JRPL instructions.

Bit 1 = **Z** Zero.

This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

0: The result of the last operation is different from zero.

1: The result of the last operation is zero.

This bit is accessed by the JREQ and JRNE test instructions.

Bit 0 = **C** Carry/borrow.

This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.

0: No overflow or underflow has occurred.

1: An overflow or underflow has occurred.

This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the “bit test and branch”, shift and rotate instructions.

Interrupt Management Bits

Bit 5,3 = **I1, I0** Interrupt

The combination of the I1 and I0 bits gives the current interrupt software priority.

Interrupt Software Priority	I1	I0
Level 0 (main)	1	0
Level 1	0	1
Level 2	0	0
Level 3 (= interrupt disable)	1	1

These two bits are set/cleared by hardware when entering in interrupt. The loaded value is given by the corresponding bits in the interrupt software priority registers (IxSPR). They can be also set/cleared by software with the RIM, SIM, IRET, HALT, WFI and PUSH/POP instructions.

See the interrupt management chapter for more details.

Stack Pointer (SP)

Read/Write

Reset Value: 017Fh

15							8
0	0	0	0	0	0	0	1
7							0
SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The Stack Pointer is a 16-bit register which is always pointing to the next free location in the stack. It is then decremented after data has been pushed onto the stack and incremented before data is popped from the stack (see [Figure 11](#)).