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ST802RT1A
ST802RT1B

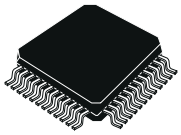
10/100 real-time Ethernet 3.3 V transceiver

Features

- IEEE802.3 10Base-T and IEEE802.3u 100Base-TX, 100Base-FX (ST802RT1B only) transceiver
- Support for IEEE802.3x flow control
- Provides full-duplex operation in both 100 Mbps and 10 Mbps modes
- Register bit strap during HW reset
- Auto MDI-X for 10/100 Mb/s
- Auto-negotiation
- Provides loop-back mode for diagnostics
- Programmable LED display for operating mode and functionality signaling
- MII / RMII interface
- MDC / MDIO serial management interface
- Optimized deterministic latency for real-time Ethernet operation
- Supports external transformer with turn ratio 1.414:1 on Tx/Rx side
- Self-termination transceiver for external components and power saving
- Operation from single 3.3 V supply
- High ESD tolerance
- 48-pin LQFP 7 x 7 package
- Extended temp. range: -40 °C to +105 °C
- Power dissipation < 315 mW (typ)

Applications

- Industrial control
- Factory automation
- High-end peripherals



LQFP48

- Building automation
- Telecom infrastructure

Description

The ST802RT1x is a high-performance fast Ethernet physical layer interface for 10Base-T, 100Base-TX and 100Base-FX applications. It is designed using advanced CMOS technology to provide MII and RMII interfaces for easy attachment to 10/100 media access controllers (MAC). The ST802RT1x supports the 100Base-TX of IEEE802.3u and 10Base-T of IEEE802.3i and 100Base FX of IEEE 802.3u (B version only). The ST802RT1x supports both half-duplex and full-duplex operation at 10 and 100 Mbps operation. Its operating mode can be set using auto-negotiation, parallel detection or manual control. It allows for the support of auto-negotiation functions for speed and duplex detection. The automatic MDI / MDIX feature compensates for the use of a crossover cable. With auto MDIX, the ST802RT1x automatically detects what is on the other end of the network cable and switches the TX & RX pin functionality accordingly.

Table 1. Device summary

Order codes	Temperature range	Package
ST802RT1AFR	- 40 to 105 °C	LQFP48
ST802RT1BFR	- 40 to 105 °C	LQFP48

Contents

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List of figures

1 Features

1.1 Physical layer

- The ST802RT1x integrates the entire physical layer functions of 100Base-TX, 10Base-T and 100Base-FX (B version only)
- Optimized deterministic latency for real-time Ethernet operation
- Provides full-duplex operation in both 100 Mbps and 10 Mbps modes
- Provides auto-negotiation (NWAY) function of full/half-duplex operation for both 10 and 100 Mbps
- Provides MLT-3 transceiver with DC restoration for base-line wander compensation
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides loop-back modes for diagnostics
- Built-in stream cipher scrambler/ de-scrambler and 4B/5B encoder/decoder
- Supports external transformer with a turn ratio of 1.414:1

1.2 LED display

The ST802RT1x supports three configurable light emitting diode (LED) pins. The three supported LED configurations are: link, speed, activity and collision. Functions are multiplexed among the LEDs according to the LED mode selected through bit 9 of the Auxiliary mode 2 register (RN1B[9]). Since these LED pins are also used as strap options, the polarity of the LED is dependent on whether the pin is pulled up or down.

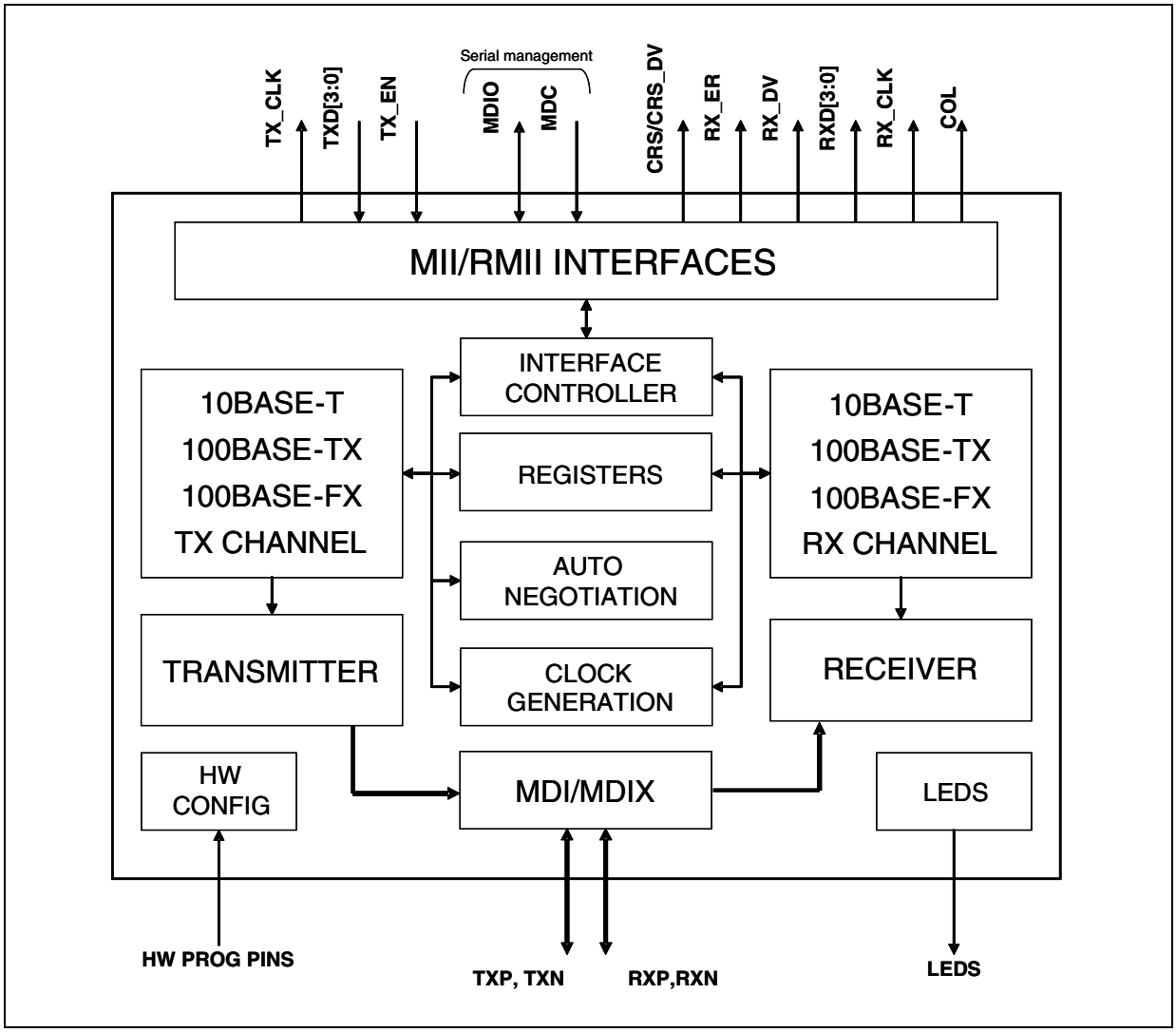
See *Table 26* and paragraph *7.11* for more details of LED mode selection.

1.3 Package

- 48-pin LQFP (7 x 7 mm.).

2 Device block diagram

Figure 1. ST802RT1x block diagram



3 System and block diagrams

Figure 2. System diagram of the ST802RT1A/B

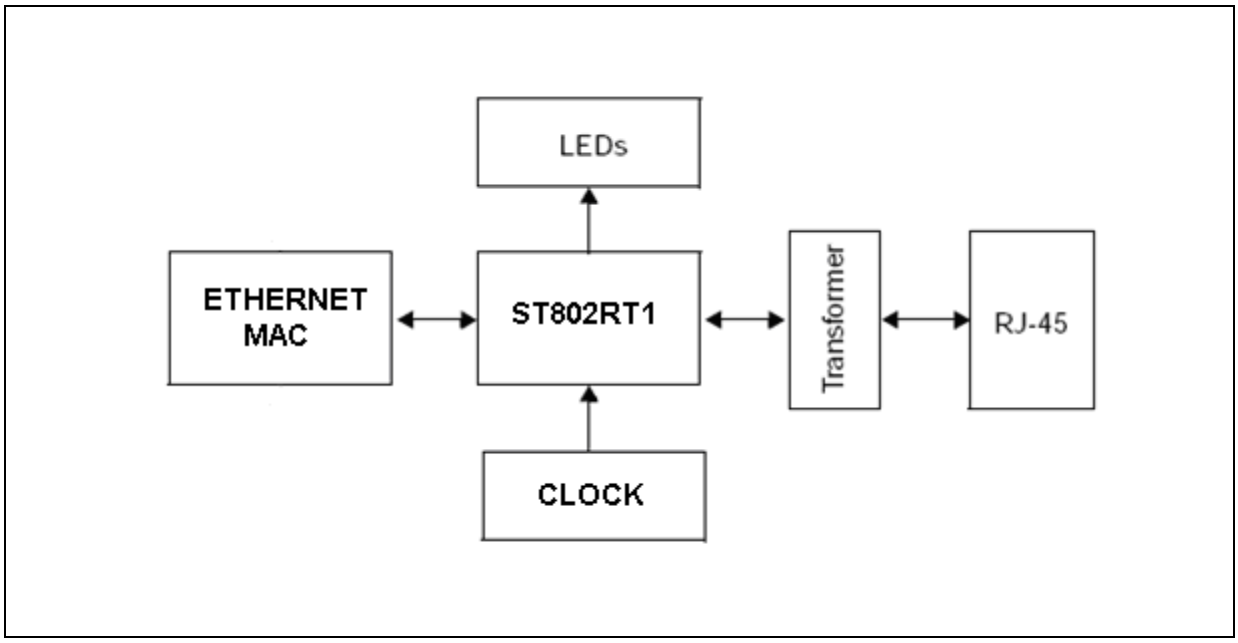
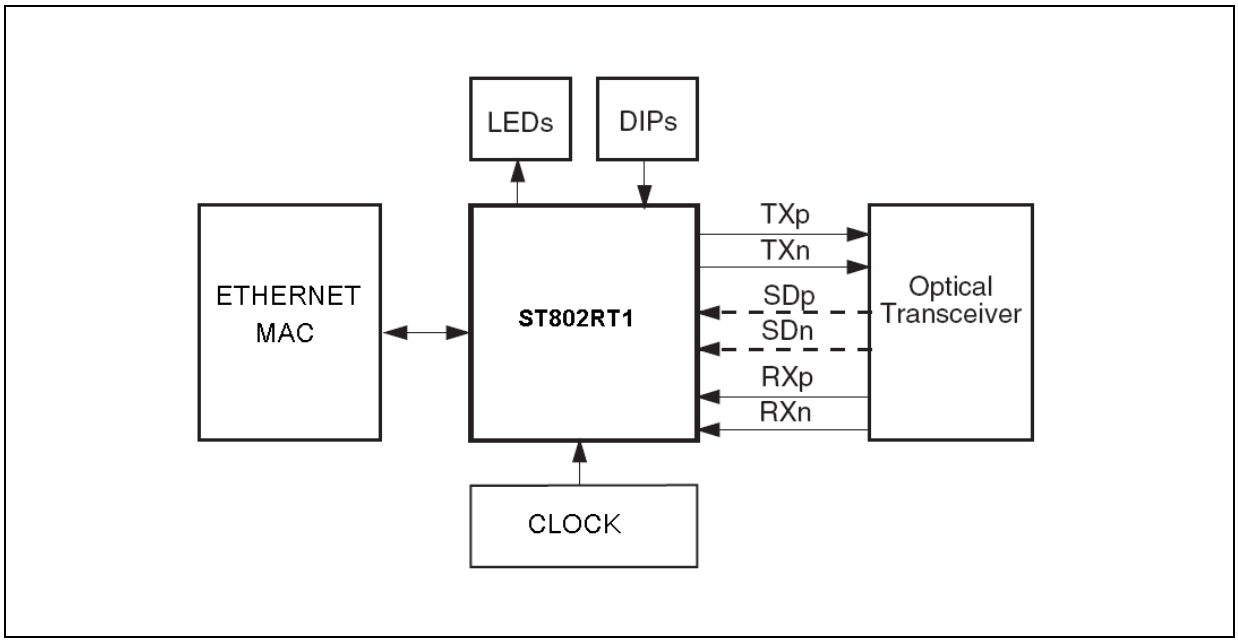


Figure 3. System diagram of the ST802RT1B in FX mode



4 Pin configuration

Figure 4. Pin configuration - ST802RT1A

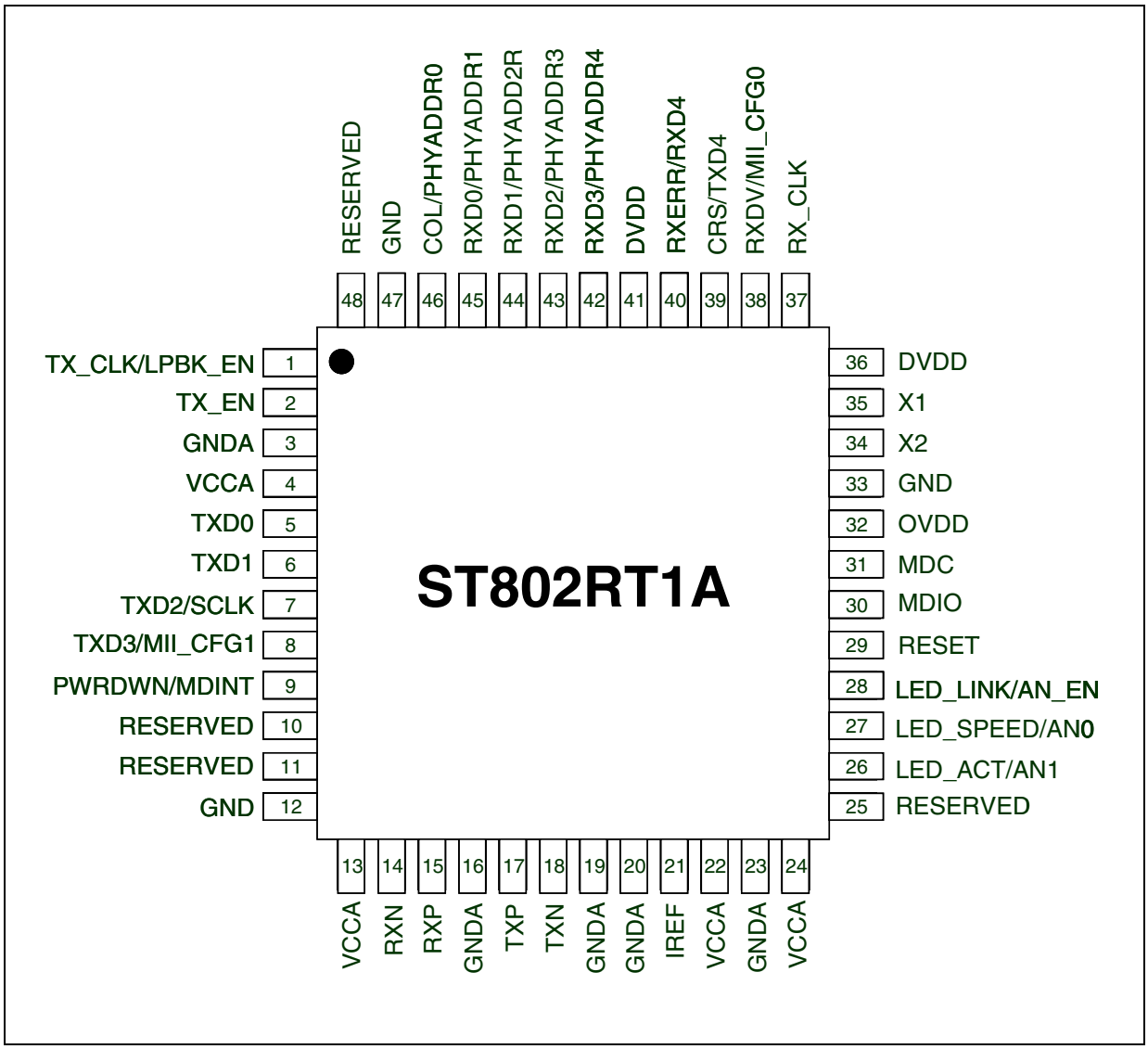
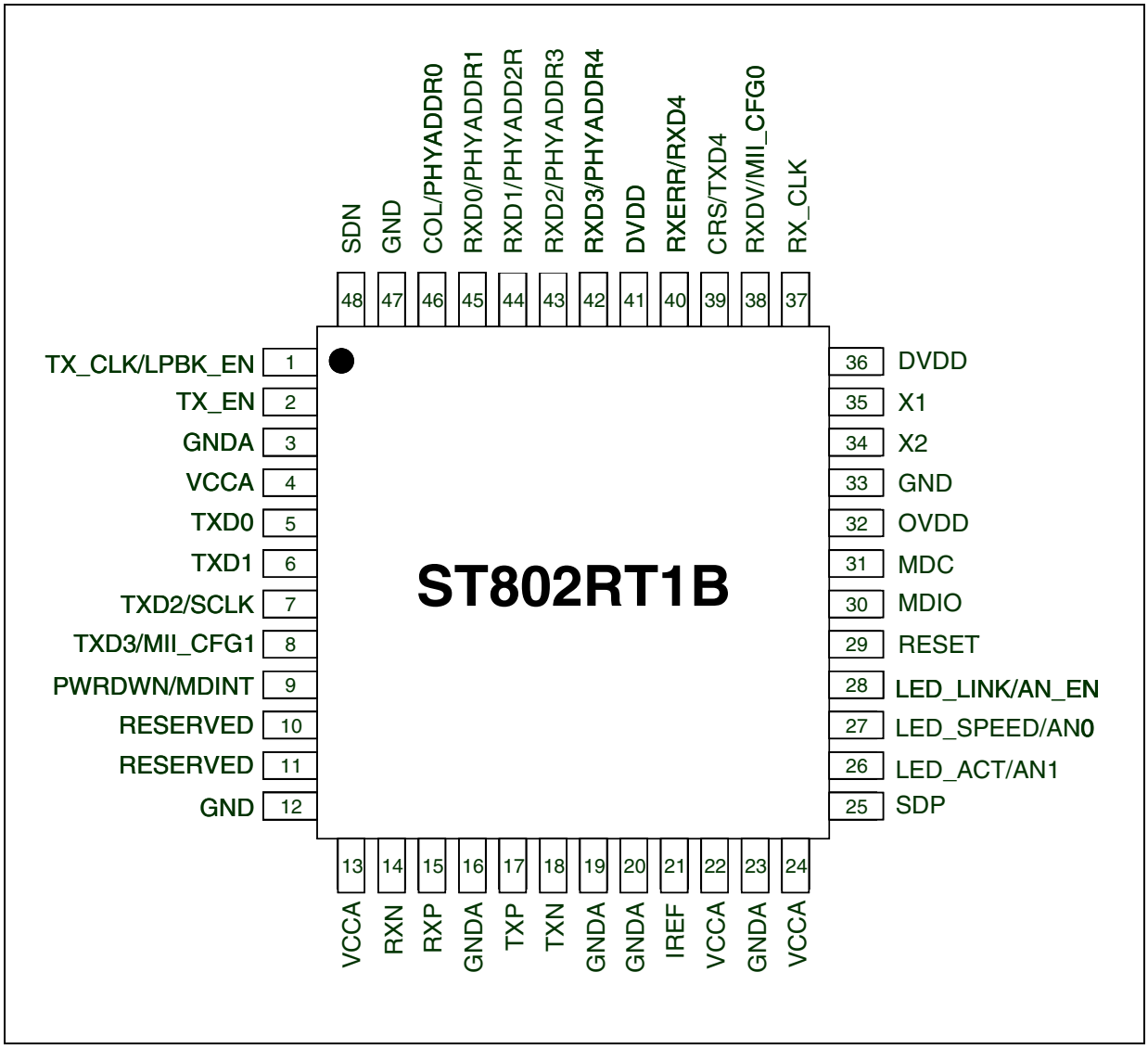


Figure 5. Pin configuration - ST802RT1B



5 Pin description

Table 2. Pin description of the ST802RT1x

Pin n° ST802RT1x	Name	Type	Description
1	TX_CLK/LPBK_EN	O, S, PD	MII transmit clock
2	TX_EN	I, PD	MII transmit enable
3	GNDA	Ground	Analog ground
4	VCCA	Supply	Analog power supply
5	TXD0	I	Transmit data (MII/RMII)
6	TXD1	I	Transmit data (MII/RMII)
7	TXD2/SCLK	I	Transmit data (MII), RMII clock (50 Mhz)
8	TXD3/MII_CFG1	I, S, PD	Transmit data (MII) / multi-function pin
9	PWRDWN/MDINT	I, PU, OD	Power-down/management data interrupt
10	RESERVED	I, PD	To be set to digital ground
11	RESERVED	I, PD	To be set to digital ground
12	GND	Ground	Digital ground
13	VCCA	Supply	Analog power supply
14	RXN	I, O	Differential receive inputs
15	RXP	I, O	Differential receive inputs
16	GNDA	Ground	Analog ground
17	TXP	I, O	Differential transmit outputs
18	TXN	I, O	Differential transmit outputs
19	GNDA	Ground	Analog ground
20	GNDA	Ground	Analog ground
21	IREF	I/O	Reference resistor/ DC regulator output (bias resistor)
22	VCCA	Supply	Analog power supply
23	GNDA	Ground	Analog ground
24	VCCA	Supply	Analog power supply
25	RESERVED	-	Not used in the ST802RT1A
	SDP	I	Positive signal detect for 100Base-FX operation (ST802RT1B only)
26	LED_ACT/AN_1	O, S, PU	Activity/full-duplex/collision led
27	LED_SPEED/AN_0	O, S, PU	Speed LED
28	LED_LINK/AN_EN	O, S, PU	Link LED
29	RESET	I	Reset (active-low)
30	MDIO	I/O, PU	Management data input/output
31	MDC	I	Management data clock

Table 2. Pin description of the ST802RT1x (continued)

Pin n° ST802RT1x	Name	Type	Description
32	OVDD	Supply	IO ring power supply (3.3 V)
33	GND	Ground	Analog ground
34	X2	O	Xtal out
35	X1	I	Xtal in (25 MHz)
36	DVDD	Supply	Digital power (3.3 V)
37	RX_CLK	O	MII receive clock
38	RXDV/MII_CFG0	O, S, PD	Receive data valid (MII: RXDV, RMII: CRSDV) / multi-function pin
39	CRS_TXD4	O	MII carrier sense / transmit data 4
40	RXER_RXD4	O	Receive error / receive data 4
41	DVDD	Supply	Digital power (3.3 V)
42	RXD3/PHYADDR4	O, S, PD	Receive data (MII)/Phy4
43	RXD2/PHYADDR3	O, S, PD	Receive data (MII)/Phy3
44	RXD1/PHYADDR2	O, S, PD	Receive data (MII/RMII)/Phy2
45	RXD0/PHYADDR1	O, S, PD	Receive data (MII/RMII)/Phy1
46	COL/PHYADDR0	O, S, PU	MII collision detection/Phy0
47	GND	Ground	Ground
48	RESERVED	-	Not used in the ST802RT1A
	SDN	I	Negative signal detect (100Base-FX only)

Table 3. Abbreviations

Legend	Description
I	Input
O	Output
I/O	Input/output
S	Strap option
OD	Open drain
PD	Pull-down
PU	Pull-up

Table 4. Pin functions of the ST802RT1x

Pin n°	Name	Type	Function
Data interface			
5 6 7 8	TXD0 TXD1 TXD2 TXD3	I	**Transmit data.** The media access controller (MAC) drives data to the ST802RT1x using these inputs. txd0 = MII/RMII tx data txd1 = MII/RMII tx data txd2/txd3 = MII tx data
7	SCLK	I	**RMII clock** (50 Mhz)
2	TX_EN	I, PD	**MII transmit enable**. The MAC asserts this signal when it drives valid data on the txd inputs.
1	TX_CLK	O, PD	**MII transmit clock**. Normally the ST802RT1x drives tx_clk. 25 MHz for 100 Mbps operation 2.5 MHz for 10 Mbps operation
40	RXER	O	**Receive error.** The ST802RT1x asserts this output when it receives invalid symbols from the network.
42 43 44 45	RXD3 RXD2 RXD1 RXD0	O, PD	**Receive data**. The ST802RT1x drives received data on these outputs. rxd0 = MII/RMII rx data rxd1 = MII/RMII rx data rxd2/rxd3 = MII rx data
38	RXDV / CRSDV	O, PD	**Receive data valid.** (MII = RXDV, RMII = CRSDV). The ST802RT1x asserts this signal when it drives valid data on rxd.
37	RX_CLK	O	**MII receive clock**. This continuous clock provides reference for rxd, rx_dv, and rx_er signals. 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation.
46	COL	O	**MII collision detection.** The ST802RT1x asserts this output when detecting a collision. This output remains high for the duration of the collision. This signal is asynchronous and inactive during full-duplex operation.
39	CRS	O	**MII carrier sense**. During half-duplex operation (RN00[8]=0), the ST802RT1x asserts this output when either transmit or receive medium is non idle. During full-duplex operation (RN00[8]=1), crs is asserted only when the receive medium is non-idle.
MII control interface			
31	MDC	I	**Management data clock**. Clock for the MDIO serial data channel. One MDC transition is also required to complete a device reset. Maximum frequency is 2.5 MHz.
30	MDIO	I/O, PU	**Management data input/output**. Bi-directional serial data channel for PHY communication.
9	MDINT	OD	**Management data interrupt**.
Physical (twisted pair) interface			
35	X1	I	**Xtal in** (25 Mhz). 25 MHz reference clock input. When an external 25 MHz crystal is used, this pin must be connected to one of its terminals. If an external 25 MHz oscillator clock source is used, then this pin will be its input pin.

Table 4. Pin functions of the ST802RT1x (continued)

Pin n°	Name	Type	Description
34	X2	O	**Xtal out**. 25 MHz reference clock output. When an external 25 MHz crystal is used, this pin is connected to one of its terminals. If an external clock source is used, then this pin should be left open.
17 18	TXP TXN	I/O	**Differential transmit outputs** (100Base-TX, 10Base-T). These pins output directly to the transformer. When MDIX is enabled, they can work as RXP/RXN
25 48	SDP SDN	I	Signal detect (ST802RT1B version only) see *Table 5*. Connect a 100 Ω resistor between TXn and VCCA and between TXp and VCCA to achieve the pseudo-emitter coupled logic (PECL) levels for the optical transmitter. The PECL logical low level ($PECL_{LOW}$) is approximately VCC-1.7 V, the PECL logical middle level ($PECL_{MID}$) is approximately VCC-1.32 V and the PECL logical high level ($PECL_{HIGH}$) is approximately VCC-0.9 V. RESERVED in ST802RT1A the pins must be grounded through a 1.2 kΩ resistor
15 14	RXP RXN	I/O	**Differential receive inputs** (100Base-TX, 10Base-T). These pins directly output to the transformer. When MDIX is enabled they can work as TXP/TXN
21	IREF	O	**Reference resistor/DC regulator output**. Reference resistor connecting pin for reference current, directly connect a 5.25 kΩ ± 1% resistor to V_{SS}.
28	LED_LINK	O, PU	**Link LED**. In Mode 1 and Mode 2 this pin indicates the status of the link. The LED is ON when the link is good.
27	LED_SPEED	O, PU	**Speed LED**. This pin is driven on continually when 10Mb/s or 100Mb/s network operating speed is detected.(All modes -> ON: 100Mb/s, OFF: 10Mb/s)
26	LED_ACT	O, PU	**Activity/collision LED**. This pin is driven on continually when a full-duplex configuration is detected. This pin is driven on at a 20 Hz blinking frequency when a collision status is detected in the half-duplex configuration. (Mode 2 -> BLINK: activity - Mode 1 -> ON: full-duplex, BLINK: collision)
29	RESET	I	**Reset (active-low)**. This input must be held low for a minimum of 1 ms to reset the ST802RT1x. During power-up, the ST802RT1x is reset regardless of the state of this pin. Reset is not complete before 1 ms plus an MDC transition.
9	PWRDWN	I, PU, OD	**Power-down**. This pin is an active low input in this mode and should be asserted low to put the device in a power-down mode. During power-down mode, TXP/TXN outputs and all LED outputs are 3-stated, and the MII interface is isolated. The power-down functionality is achievable by software by asserting bit 11 of register RN00.
10, 11	RESERVED	PD	(No connection) - Should be pulled low for normal operation through an external resistor of 2.2 kΩ
Digital power pins			
32	OVDD	Supply	**IO ring power supply** (3.3 V)
36, 41	DVDD	Supply	**Digital power** (3.3 V)
12, 33, 47	GND	Ground	Digital ground
Analog power pins			
4, 13, 22, 24	VCCA	Supply	Analog power supply

Table 4. Pin functions of the ST802RT1x (continued)

Pin n°	Name	Type	Description
3, 16, 19, 20, 23	GNDA	Ground	Analog ground
Strap pins The ST802RT1x uses many of the functional pins as strap options. The values of these pins are sampled during reset hardware or power-up and used to strap the device into specific modes of operation. The ST802RT1x provides simple strap options to automatically configure some device modes with no device register configuration necessary. All strap pins have a weak internal pull-up or pull-down. If the default strap value is needed to be changed, they should not be connected directly to V_{CC} or GND and an external 2.2 kΩ resistor should be used. The software reset and the power down through the PD pin cannot be used to change the strap configuration			
1	LPBK_EN	S, PD	Loop-back enable
38 8	MII_CFG0 MII_CFG1	S, PD	MII Mode Select: This strapping option pair determines the operating mode of the MAC Data Interface. Default operation (No pull-ups) enables normal MII mode of operation. Strapping mii_cfg0 high causes the device to be in RMII mode of operation, determined by the status of the mii_cfg1 strap. Since the pins include internal pull-downs, the default values are 0. See *Table 6* for details and configurations
28 27 26	AN_EN AN_0 AN_1	S, PU	Auto-negotiation enable: When high, this enables auto-negotiation with the capability set by the an_0 and an_1 pins. When low, this puts the part into Forced Mode with the capability set by the an_0 and an_1 pins. an_0 / an_1: These input pins control the forced or advertised operating mode of the ST802RT1x according to *Table 7*. The value on these pins is set by connecting the input pins to GND (0) or VCC (1) through 2.2 kΩ resistors. These pins should NEVER be connected directly to GND or V_{CC}. The value set at this input is latched into the ST802RT1x at Hardware-Reset. The float/pull-down statuses of these pins are latched into the basic mode control register and the auto-negotiation advertisement register during hardware-reset. The default is 111 since these pins have internal pull-up (see *Table 7*).
46 45 44 43 42	PHYADDR0 PHYADDR1 PHYADDR2 PHYADDR3 PHYADDR4	S, PU S, PD	PHY address [4:0]. These pins are used to provide the address which is latched into the internal receive mode control register RN14 (0x14h) after the reset. PHYADDR0 pin has weak internal pull-up resistor. PHYADDR[4:1] pins have weak internal pull-down resistors. An external 2.2 kΩ resistor should be used for pull-up/down the pins

Table 5. Signal detect

SDN	SDP	Mode
Ground	Ground	TX mode
Ground	A positive voltage	Undefined state
Voltage > 0.6 V	Voltage > 0.6 V	Undefined state
$PECL_{LOW}$ ($PECL_{MID}$)	$PECL_{LOW}$	FX mode asserted, but no data valid on the line
$PECL_{HIGH}$ ($PECL_{MID}$)	$PECL_{LOW}$	FX mode asserted, but no data valid on the line
$PECL_{HIGH}$	$PECL_{HIGH}$	Undefined state
$PECL_{LOW}$ ($PECL_{MID}$)	$PECL_{HIGH}$	FX mode asserted, link OK, and data valid

Table 6. MII_CFG0, MII_CFG1 configuration

	mii_cfg0	mii_cfg1
MII mode	0	X
RMII mode	1	0
Reserved	1	1

Table 7. Auto-negotiation advertisement register

Forced mode	an_en	an_0	an_1
10M, Half-duplex	0	0	0
10M, Full-duplex	0	0	1
100M, Half-duplex	0	1	0
100M, Full-duplex	0	1	1
Advertised mode	an_en	an_0	an_1
10M, Half/full-duplex	1	0	0
100M, Half/full-duplex	1	0	1
10M, Half-duplex 100M, Half-duplex	1	1	0
10M, Half/Full-duplex 100M, Half/Full-duplex	1	1	1

6 Registers and descriptors description

All of the management data control and status registers in the ST802RT1x's register set are accessed via a Write or Read operation on the serial MDIO port. This access requires a protocol described in the MII management interface section.

6.1 Register list

Table 8. List of registers

Address	Reg. Index	Name	Default value	Register description
00h – 0d	RN00	CNTRL	0x0000	Control register
01h – 1d	RN01	STATS	0x7849	Status register
02h – 2d	RN02	PHYID1	0x0203	PHY identifier register Hi
03h – 3d	RN03	PHYID2	0x8461	PHY identifier register Lo
04h – 4d	RN04	LDADV	0x05E1	Auto-negotiation advertisement register
05h – 5d	RN05	LPADV	0x0000	Auto-negotiation link partner ability register
06h – 6d	RN06	ANEGX	0x0004	Auto-negotiation expansion register
07h – 7d	RN07	LDNPG	0x2001	Auto-negotiation next page transmit register
08h – 8d	RN08	LPNPG	0x0000	Auto-negotiation link partner received next page register
Extended registers				
10h – 16d	RN10	XCNTL	0x1200	RMII-TEST control register
11h – 17d	RN11	XSTAT	0x0000	Receiver configuration information and interrupt status register
12h – 18d	RN12	XRCNT	0x0100	Receiver event interrupts register
13h – 19d	RN13	XCCNT	0x0140	100Base-TX control register
14h – 20d	RN14	XDCNT	0x000A	Receiver mode control register
18h – 24d	RN18	AUXCS	0x0027	Auxiliary control register
19h – 25d	RN19	AUXSS	0x0000	Auxiliary status register
1Bh – 27d	RN1B	AUXM2	0x000A	Auxiliary mode 2 register
1Ch – 28d	RN1C	TSTAT	0x0820	10Base-T error and general status register
1Eh – 30d	RN1E	AMPHY	0x0000	Auxiliary PHY register
Shadow registers				
1Fh - 31d	RN1F	BTEST	0x0000	Shadow Registers enable register
1Bh - 27d	RS1B	AUXS2	0x0000	MISC/status/error/test shadow register

6.2 Register description

Table 9. Abbreviations

Legend	Description
RW	Read/write
RO	Read only
SC	Self-clearing
P	Constant
STRAP	Bit with strap value
LH	Latched high
LL	Latched low

Table 10. RN00 [0d00, 0x00]: Control register

Bit	Bit name	Description	Default	RW type	Type
15	Soft reset	1 -> software reset, reset in process 0 -> normal operation This bit, which is self-clearing, returns 1 until the reset process is complete. After this reset the configuration is not re-strapped.	0	RW	SC
14	Local loop-back	1 -> Loop-back enabled 0 -> Normal operation Local loop-back passes data from transmitting to receiving serial conversion analog logic.	Strap	RW	-
13	Speed selection	1 -> 100 Mb/s 0 -> 10 Mb/s Ignored if auto-negotiation is enabled	Strap	RW	-
12	Auto-negotiation enable	1 -> Auto-negotiation is enabled 0 -> Auto-negotiation is disabled Bits 8 and 13 of this register are ignored if this bit is set high. Not available in FX-mode (auto-negotiation always disabled)	Strap	RW	-
11	Power-down	1 -> Power down 0 -> Normal operation	0	RW	-
10	Isolate	1 -> Isolates the core from the MII, with the exception of the serial management 0 -> Normal operation. When this bit is set to ‘1’, related pad outputs are forced to tri-state, inputs are ignored. MII isolate mode can be activated at initialization by strapping 00000 on physical address.	Strap	RW	-
9	Auto-negotiation restart	1 -> Restarts Auto-negotiation process (ignored if Auto-negotiation is disabled) 0 -> Normal operation	0	RW	SC
8	Duplex mode	1 -> full-duplex operation 0 -> Half-duplex operation Ignored if auto-negotiation is enabled	Strap	RW	-

Table 10. RN00 [0d00, 0x00]: Control register (continued)

Bit	Bit name	Description	Default	RW type	Type
7	Collision test	1 -> Collision test enabled 0 -> Normal operation Active only in loop-back mode (RN00[14]=1)	0	RW	-
6	RESERVED	Not used	0	RO	P
5	RESERVED	Not used	0	RO	P
4	RESERVED	Not used	0	RO	P
3	RESERVED	Not used	0	RO	P
2	RESERVED	Not used	0	RO	P
1	RESERVED	Not used	0	RO	P
0	RESERVED	Not used	0	RO	P

Soft reset: In order to reset the ST802RT1x by software control, a **"1"** must be written to bit 15 of the control register using a serial management interface write operation. The bit clears itself after the reset process is complete, and does not need to be cleared using a second MII write. Writes to other control register bits have no effect until the reset process is completed, which requires approximately 1 millisecond. Writing a "0" to this bit has no effect. Since this bit is self-clearing, after a few cycles from a write operation, it returns a "0" when read.

Local loop-back: The ST802RT1x may be placed into loop-back mode by writing a **"1"** to bit 14 of the control register. The loop-back mode may be cleared by writing a "0" to bit 14 of the control register, or by resetting the chip. When this bit is read, it returns a "1" when the chip is in software-controlled loop-back mode; otherwise it returns a "0".

Speed selection: If auto-negotiation is enabled, this bit has no effect on the speed selection. However, if auto-negotiation is disabled by software control, the operating speed of the ST802RT1x can be forced by writing the appropriate value to bit 13 of the control register. Writing a "1" to this bit forces 100BASETX operation, while writing a "0" forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only.

Auto-negotiation enable: Auto-negotiation can be disabled by one of two methods: hardware or software control. If the AN_EN input pin is driven to "0", auto-negotiation is disabled by hardware control. If bit 12 of the control register is written with a value of "0", auto-negotiation is disabled by software control. When auto-negotiation is disabled in this manner, writing a "1" to the same bit of the control register re-enables auto-negotiation. If auto-negotiation is disabled in this manner and the chip is reset the auto-negotiation follows the strap configuration. Writing to this bit has no effect when auto-negotiation has been disabled by hardware control. When read, this bit returns the value most recently written to this location, or "1" if it has not been written since the last chip reset.

Power-down: If set to '1', the channel is powered down. If this bit is set for all channels, then the IO pad directions are forced and the device is in power-down state. Refer to *Section 7.9* for a more detailed explanation of the power-down operation.

Isolate: The PHY may be isolated from its media independent interface (MII) by writing a **"1"** to bit 10 of the control register. All MII outputs are tri-stated, except tx_clk, and all MII inputs are ignored. Since the MII management interface is still active, the isolate mode may

be cleared by writing a “0” to bit 10 of the control register, or by resetting the chip. When this bit is read, it returns a “1” when the chip is in isolate mode; otherwise it returns a “0”.

Restart auto-negotiation: Bit 9 of the control register is a self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the auto-negotiation state machine. In order for this bit to have an effect, auto-negotiation must be enabled. Writing a “1” to this bit restarts the auto-negotiation, while writing a “0” to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a “0” when read.

Full-duplex: By default, the ST802RT1x powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a “1” to bit 8 of the control register while auto-negotiation is disabled. Half-duplex mode can be resumed by writing a “0” to bit 8 of the control register, or by resetting the chip.

Collision test: The COL pin may be tested during loop-back by activating the collision test mode. While in this mode, asserting TXEN causes the COL output to go high within 512 bit times. De-asserting TXEN causes the COL output to go low within 4 bit times. Writing a “1” to bit 7 of the control register enables the collision test mode. Writing a “0” to this bit or resetting the chip disables the collision test mode. When this bit is read, it returns a “1” when the collision test mode has been enabled; otherwise it returns a “0”. This bit should only be set while in loop-back test mode.

Reserved bits: Write ignored, read as 0.

Table 11. RN01 [0d01, 0x01]: Status register

Bit	Bit name	Description	Default	RW type	Type
15	100BASE-T4 ABILITY	0 -> PHY not able to perform 100BASE-T4 Fixed to 0	0	RO	P
14	100BASE-X Full Duplex	1 -> PHY able to perform full-duplex 100BASE-X Fixed to 1, internally not used	1	RO	P
13	100BASE-X Half Duplex	1 -> PHY able to perform half-duplex 100BASE-X Fixed to 1	1	RO	P
12	10BASE-T Full Duplex	1 -> PHY able to perform full-duplex 10BASE-T Fixed to 1, internally not used	1	RO	P
11	10BASE-T Half Duplex	1 -> PHY able to perform half-duplex 10BASE-T Fixed to 1	1	RO	P
10	RESERVED	Not used	0	RO	P
9	RESERVED	Not used	0	RO	P
8	RESERVED	Not used	0	RO	P
7	RESERVED	Not used	0	RO	P
6	MF Preamble Suppression	1 -> Accepts management frames with preamble suppressed 0 -> Doesn't accept management frames without preamble Controlled by RN14 [1].	1	RO	-
5	Auto-Negotiation complete	1 -> Auto-negotiation process completed, registers 4, 5, 6 are now valid 0 -> Auto-negotiation process not completed Active only if auto-negotiation is enabled, else 0	0	RO	-
4	Remote Fault	1 -> Remote fault condition detected 0 -> No remote fault condition detected Set when link partner signals a remote fault condition (RN05 - bit 13) or a far-end-fault indicator was asserted. Latched, so the occurrence of a remote fault causes the remote fault bit to become set and remain set until it is cleared (by register read, if no more fault is present).	0	RO	LH
3	Auto-Negotiation Ability	1 -> PHY is able to perform auto-negotiation Fixed to 1	1	RO	P
2	Link Status	1 -> Link is valid and established (either for 10 and 100 Mb/s) 0 -> Link is down This bit is cleared at link failure and set after a register read if a valid link is established	0	RO	LL
1	Jabber Detect	1 -> Jabber condition detected: transmission exceeded max number of bytes 0 -> No jabber condition detected. Set at jabber condition detection, cleared only after register read (if no more jabber condition is present). Working on 10Base-T only. Fixed to 0 in 100Base-X modes	0	RO	LH
0	Extended Capability	1 -> extended register capabilities Fixed to 1	1	RO	P

Reserved bits: Ignore ST802RT1x output when these bits are read.

Preamble suppression: This bit is a read-only bit and can be set by bit 1 of the RN14 register. When read as a logic “1”, the ST802RT1x is able to accept MII management frames with or without the standard preamble pattern. When preamble suppression is enabled (RN14[1]=1), only 2 preamble bits are required between successive management commands, instead of the normal 32.

Auto-negotiation complete: Bit 5 of the status register returns a **“1”** if the auto-negotiation process has been completed, and the contents of registers 4, 5, and 6 are valid.

Link status: The ST802RT1x returns a **“1”** on bit 2 of the status register when the link state machine is in link pass, indicating that a valid link has been established. Otherwise, it returns a “0”. When a link failure occurs after the link pass state has been entered, the link status bit is latched at “0” and remains so until the bit is read. After the bit is read, it becomes “1” if the link pass state has been entered again.

Jabber detect: 10BASE-T operation only. The ST802RT1x returns a **“1”** on bit 1 of the status register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to “0”.

Extended register ability: Because the ST802RT1x supports extended register capability, this read-only bit is always “1”. The ST802RT1x extended registers with their bit functions are described in later sections of this document.

The PHY identifier registers #1 and #2 consist of a sum of the organizationally unique identifier (OUI), the vendor's model number and the model revision number. ST's IEEE assigned OUI is 0x0080E1.

Table 12. RN02 [0d02, 0x02]: PHY identifier register Hi

Bit	Bit name	Description	Default	RW type	Type
15:0	OUI MSBs	Organizationally unique identifier (OUI), bits 3..18 OUI bits 1 and 2 are fixed to 0 by standard; ST OUI = 0080E1	0203h	RO	P

Table 13. RN03 [0d03, 0x03]: PHY identifier register Lo

Bit	Bit name	Description	Default	RW type	Type
15:10	OUI LSBs	Organizationally unique identifier (OUI), bits 19..24	100001b	RO	P
9:4	MODEL NUMBER	Manufacturer’s model number	000110b	RO	P
3:0	REVISION NUMBER	Allows identification of the revision of the device via software reading of the register	0001b	RO	P

Table 14. RN04 [0d04, 0x04]: Auto-negotiation advertisement register

Bit	Bit name	Description	Default	RW type	Type
15	Next Page	1 -> Next page transfer supported 0 -> Next page transfer not supported	0	RW	-
14	RESERVED	---	0		P
13	Remote Fault	1 -> Advertises that this device has detected a remote fault during auto-negotiation 0 -> No remote fault detected.	0	RW	-
12	RESERVED	---	0		-
11	Asymmetric Pause (full-duplex)	1 -> Asymmetric pause supported (MAC level) 0 -> No MAC based full-duplex flow control.	0	RW	-
10	Pause (full-duplex)	1 -> Symmetric pause supported (MAC level) 0 -> No MAC based full-duplex flow control.	1	RW	-
9	100BASE-T4	0 -> 100BASE-T4 not supported	0	RW	-
8	100BASE-TX full duplex	1 -> 100BASE-TX Full-duplex is supported by the local device 0 -> 100BASE-TX Full-duplex is not supported	Strap	RW	-
7	100BASE-TX	1 -> 100BASE-TX is supported by the local device 0 -> 100BASE-TX is not supported	Strap	RW	-
6	10BASE-T full duplex	1 -> 10BASE-T Full-duplex is supported by the local device 0 -> 10BASE-T Full-duplex is not supported	Strap	RW	-
5	10BASE-T	1 -> 10BASE-T is supported by the local device 0 -> 10BASE-T is not supported	Strap	RW	-
4:0	Selector	00001 -> IEEE802.3u	00001b	RW	-

Next page: The ST802RT1x supports next page capability.

Reserved: Ignore output when read.

Remote fault: Writing a **“1”** to bit 13 of the advertisement register causes a remote fault indicator to be sent to the link partner during auto-negotiation. Writing a “0” to this bit or resetting the chip clears the remote fault transmission bit. This bit returns the value last written to it, or else “0” if no write has been completed since the last chip reset.

Asymmetric pause: write '1' if asymmetric pause is supported by MAC when full-duplex link is available. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sub layer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = No MAC based full-duplex flow control.

Pause: The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate symmetric pause capability to its link partner, and has no effect on PHY operation.

Advertisement bits: Bits 9:5 of the advertisement register allow the user to customize the ability information transmitted to the link partner. The default value for each bit reflects the abilities of the ST802RT1x. By writing a “1” to any of the bits, the corresponding ability is transmitted to the link partner. Writing a “0” to any bit causes the corresponding ability to be

suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset. Even though bit 9 (advertise 100BASE-T4) is writable, it should never be set since the ST802RT1x does not support T4 operation.

Advertised selector: Bits 4:0 of the advertisement register contain the fixed value “00001”, indicating that the chip belongs to the 802.3 class of PHY transceivers

Table 15. RN05 [0d05, 0x05]: Auto-negotiation link partner ability register

Bit	Bit name	Description	Default	RW type	Type
15	LP Next Page	1 -> Link partner desires next page transfer 0 -> Link partner does not desire next page transfer	0	RO	-
14	LP Acknowledge	1 -> Link partner acknowledges reception of the ability data word 0 -> Acknowledge not yet received	0	RO	-
13	LP Remote Fault	1 -> Remote fault indicated by link partner 0 -> No remote fault indicated by link partner	0	RO	-
12	RESERVED	--	0	RO	-
11	Asymmetric Pause (full-duplex)	1 -> LP supports asymmetric pause (MAC level: clause 31, annex 31B of 802.3u) 0 -> LP has no MAC-based full-duplex flow control.	0	RO	-
10	LP pause (full-duplex)	1 -> LP supports symmetric pause (MAC level: clause 31, annex 31B of 802.3u) 0 -> LP has no MAC-based full-duplex flow control.	0	RO	-
9	100BASE-T4	1 -> LP supports 100BASE-T4 0 -> LP does not support 100BASE-T4	0	RO	-
8	100BASE-TX full duplex	1 -> LP supports 100BASE-TX full-duplex 0 -> LP does not support 100BASE-TX full-duplex	0	RO	-
7	100BASE-TX	1 -> LP supports 100BASE-TX 0 -> LP does not support 100BASE-TX	0	RO	-
6	10BASE-T full duplex	1 -> LP supports 10BASE-T full-duplex 0 -> LP does not support 10BASE-T full-duplex	0	RO	-
5	10BASE-T	1 -> LP supports 10BASE-T 0 -> LP does not support 10BASE-T	0	RO	-
4:0	LP selector field	LP's binary encoded protocol selector	00000b	RO	-

LP next page: Bit 15 of the link partner ability register returns a value of “1” when the link partner implements the next page function and has next page information that it wants to transmit.

LP ack: Bit 14 of the link partner ability register is used by auto-negotiation to indicate that a device has successfully received its link partner's link code word.

LP remote fault: Bit 13 of the link partner ability register returns a value of “1” when the link partner signals that a remote fault has occurred. The ST802RT1x simply copies the value to this register and does not act upon it.

Reserved: Ignore when read.

LP pause: Indicates that the link partner pause bit is set.

LP selector field: Bits 4:0 of the link partner ability register reflect the value of the Link partner's selector field. These bits are cleared any time auto-negotiation is restarted or the chip is reset.

Advertisement bits: Bits 9: 5 of the link partner ability register reflect the abilities of the Link partner. A “1” on any of these bits indicates that the link partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time auto-negotiation is restarted or the ST802RT1x is reset.

Table 16. RN06 [0d06, 0x06]: Auto-negotiation expansion register

Bit	Bit name	Description	Default	RW type	Type
15:5	RESERVED	--	00000000000	RO	P
4	Parallel Detection Fault	1 -> A fault has been detected via the parallel detection function (updated on read) 0 -> A fault has not been detected	0	RO	LH
3	Link Partner Next Page Able	1 -> LP is next-page able 0 -> LP does not support next pages	0	RO	-
2	Next Page Able	1 -> Local device is next-page able Fixed to 1	1	RO	P
1	Page Received	1 -> Link code word received (updated on read) 0 -> Link code word not yet received	0	RO	LH
0	Link Partner Auto-Negotiation Able	1 -> LP supports auto-negotiation (updated on read) 0 -> LP does not support auto-negotiation	0	RO	LH

Reserved: Ignore when read.

Parallel detection fault: Bit 4 of the auto-negotiation expansion register is a read-only bit that gets latched high when a parallel detection fault occurs in the auto-negotiation state machine. For further details, please consult the IEEE standard. The bit is reset to “0” after the register is read, or when the chip is reset.

LP next page able: Bit 3 of the auto-negotiation expansion register returns a **“1”** when the link partner has next page capabilities. It has the same value as bit 15 of the link partner ability register.

Page received: Bit 1 of the auto-negotiation expansion register is latched high when a new link code word is received from the link partner, checked, and acknowledged. It remains high until the chip is reset.

LP auto-negotiation able: Bit 0 of the auto-negotiation expansion register returns a **“1”** when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged, or if the link partner does not comply with IEEE auto-negotiation, the bit returns a value of “0”.